Interconnection Networks for Massively Parallel Computer on 3D Stacked Implementation

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1 Introduction

A massively parallel computer was implemented in wafer scale integration(WSI). However the number of processing elements(PEs) implemented on a wafer is limited. The three dimensional(3D) stacked implementation has been proposed as a new technology for massively parallel computers. Since the area of vertical links between wafers amount to hundreds μm^2, it requires far fewer number of vertical links than almost all known massively parallel computer networks. A restriction of vertical links increases the diameter of networks and makes network feature worse. Thus, a new interconnection needs reducing the number of vertical links for 3D stacked implementation with keeping good network feature.

This paper discusses network feature such as diameter, the maximum number of vertical links and chip area conventional networks on 3D stacked implementation. After the investigation of 3D stacked implementation, we propose the two types of network, 3D hierarchical mesh networks and 3D hierarchical torus network. The primitive applications;sorting and FFTs are mapped on two networks and the performances are discussed by comparing those on the conventional networks.

2 The network feature on 3D stacked implementation

This section discuss networks for 3D stacked implementation. We examine the conventional networks feature on 3D stacked implementation and show the issues of 3D stacked implementation. We use the conventional networks such as 2Dtorus, 3Dtorus, Hypercube, TESH and the network features such as diameter, the vertical links between wafers, chip area.

The low degree 2Dtorus have a few vertical wires and keep chip area narrow. But the diameter of 2Dtorus is large.Therefore communication delay of 2Dtorus is large.The diameter of Hypercube is small, but to implement Hypercube on 3D stacked implementation is hard because of vertical links. TESH and 3Dtorus realize small diameter and few vertical links. In particular, hierarchical interconnection networks, TESH can realize smaller diameter and fewer vertical links. Therefore, hierarchical interconnection networks is suited for 3D stacked implementation.

3 3D hierarchical interconnection networks

For the 3D stacked implementation, it requires interconnection networks which have fewer vertical links and keep diameter at the same. This chapter propose two 3D hierarchical interconnection networks(3Dh-network) having good feature.

The 3Dh-networks do hierarchical interconnection between basic modules and realize smaller vertical links.This paper propose 3Dh-torus and 3Dh-mesh. The 3Dh-torus have smallest vertical links. 3Dh-mesh increase the number of links between basic modules for decreasing communication concentration at links between basic modules.

We calculate the 3Dh-networks features and compare the conventional network. The 3Dh-torus have fewer vertical wires than 2Dtorus having smaller vertical links. The chip area of 3Dh-torus is 60 percent that of 2Dtorus. The 3Dh-mesh have many links between basic modules, therefore 3Dh-mesh have more vertical wires than 3Dh-torus. But 3Dh-mesh have fewer vertical links than 3Dtorus. So, chip area of 3Dh-torus is 60 percent that of 3Dtorus.

4 Application

This chapter consider mapping the basic applications, such as sort, FFT, maximum to 3Dh-networks and evaluate with communication steps. The 3Dh-networks is built by many 3Dtorus and 3Dmesh or 3Dtorus and 2Dmesh and can use conventional mapping method. This paper adopt divide&conquer scheme for mapping primitive applications. The divide&conquer scheme iteravely divide a problem into subproblems and finally combines the results of the subproblems by executing operations on corresponding pair of sub-results. Because of wire-limiting, 3Dh-torus can't get good feature. But 3Dh-mesh can operate applications fewer communication steps than 2Dtorus. 3D-hnetworks can

operate the problem of maximum which require a few data communication with a few steps.

5 Conclusion

This paper examine conventional network feature on 3D stacked implementation and propose 3Dh-networks. We show that 3Dh-networks can realize small diameter and few links on 3D stacked implementation at the same time. we show being able to map applications to 3Dh-networks easily. Future research is to discuss hierarchical redundance mapping and mapping advanced application.