Selective area molecular beam epitaxy of InAs on GaAs (110) masked substrates for direct fabrication of planar nanowire field-effect transistors

M. Akabori*, T. Murakami, S. Yamada

Center for Nano Materials and Technology (CNMT). Japan Advanced Institute of Science and Technology (JAIST), 1-1 Asahidai, Nomi, Ishikawa 923-1292, Japan

*Corresponding author, e-mail: akabori@jaist.ac.jp; Tel: +81-761-51-1477; Fax: +81-761-51-1049.

Abstract

We have synthesized InAs nanowires (NWs) by selective area molecular beam epitaxy (SA-MBE) on GaAs masked substrates. In particular, we have obtained in-plane-oriented NWs on the (110) plane, and then directly applied the NWs to planar nanowire field-effect transistors (NWFETs) by using conventional electron beam lithography without a NW dispersion process. We have measured output and transfer characteristics of the NWFETs at room temperature, and obtained a current swing but no turning off, and a field-effect mobility peak of 150 cm^2/V-s. We have also observed almost no temperature influence on field-effect mobility between 2 K and 300 K, suggesting a high-dense surface accumulation layer even at low temperatures.

Keywords

A1. Nanostructures; A3. Molecular beam epitaxy; A3. Selective epitaxy; B2. Semiconducting III-V materials; B3. Field effect transistors

1. Introduction

III-V compound semiconductor nanowires (NWs) have received much attention as base components of novel nanodevices, e.g. nanowire field-effect transistors (NWFETs). Especially, InAs NWs are very promising to realize high-performance NWFETs [1-3], spintronic NWFETs [4, 5], and single-electron spin-qubit quantum dots with multi-gates [6]. This is because InAs has a narrow gap, a surface accumulation layer, i.e. conductivity, a high mobility and a large spin-splitting. For the NWFET applications, it is desirable that NWs are synthesized by controlling their positions as well as orientations. A catalyst-free selective area epitaxy on partially masked substrates is one of the appropriate methods to synthesize controlled NWs; in fact, vertically-oriented and position-controlled InAs NWs have been realized on III-V (111)B or Si (111) [7-9]. The vertical-oriented NWs are applicable to vertical NWFETs by a using complex three-dimensional fabrication process [1-2] or to planar NWFETs by using a NW dispersion process [3-5]. However, both processes cannot be suitable for NWFET integration. On the other hand, in-plane-oriented NWs toward substrate surfaces have been realized by using vapor-liquid-solid growth [10], which is one of the major methods of NW synthesis. If such in-plane-oriented NW formation is performed with position-controlling, it will be possible to carry out direct fabrication of planar NWFETs by using conventional lithography, and then to develop the NWFET integration techniques.

To this end, in this paper, we have chosen selective area molecular beam epitaxy (SA-MBE) on GaAs (110) masked substrates as a synthesis method of in-plane-oriented InAs NWs. In-plane-oriented NWs obtained by selective area epitaxy are also expected to show high-quality, because this method can confine misfit dislocations due to lattice mismatch between NW and substrate materials around opening area like microchannel epitaxy [11]. Thus, it can provide high-quality InAs NWs except around InAs/GaAs interfaces when the length of NWs becomes much longer than the opening diameter. In order to confirm growth selectivity between opening and mask areas, we have first performed SA-MBE of InAs on GaAs (001) plane at various growth temperatures. Next, we have compared the SA-MBE morphology on GaAs (001), (111)B and (110) planes. Then, we have directly fabricated InAs planar NWFETs on GaAs (110) plane by SA-MBE and conventional electron-beam lithography (EBL) without any NW dispersion process. Finally, we have measured the electrical characteristics of the NWFETs.

2. Selective area molecular beam epitaxy of InAs on GaAs (001), (111)B and (110) masked substrates

We first coated GaAs (001), (111)B and (110) low-index substrates with hydrogen slisesquioxane (HSQ) after a conventional surface treatment. Next, we patterned HSQ/GaAs with a hole array by using EBL with a positive-type resist and reactive ion etching with CHF_3. The initial opening holes were designed with an almost circular shape, and the diameter and the pitch were about 100-300 and 500-1000 nm, respectively. After resist removal, we treated the substrates using H_2SO_4 and de-ionized water, and then loaded them into a conventional solid-source MBE system. In the growth chamber, the substrates were heated up to 590-600°C once under As ambient for the thermal cleaning, and then they were cooled down to 460-540°C for growth. The beam equivalent pressure (BEP) of As was fixed to $1x10^{-6}$ Torr. It should be noted that we did not employ any intentional doping into InAs. However, SA-MBE grown InAs were expected to be conductive, because InAs grown on GaAs has electron accumulation layers at the surface and the interface of InAs/GaAs [12]. In fact, 1-μm-thick InAs grown on GaAs(001) in our MBE system shows sheet electron concentration of $3x10^{12}$ cm^{-2} and electron mobility of 10000 cm^2/V-s, which seem typical values in un-doped InAs/GaAs(001) [12].

Figure 1 shows scanning electron microscope (SEM) images of SA-MBE grown InAs on HSQ/GaAs(001) at various temperatures with two different In BEPs ($0.5x10^{-7}$ and $1x10^{-7}$ Torr). The growth time for all samples shown in this figure was 1 hour. The tilt angle was 45° for all images. At 460°C, low and high In BEPs result in a few and many polycrystalline depositions on HSQ masks, respectively. Additionally, in the case of low In BEP, position-controlled pyramids were clearly observed. At 480°C, the pyramid growth as well as the polycrystalline deposition was no longer observed in the case of low In BEP, which indicates less nucleation for the growth due to re-evaporation of In adatoms. In contrast, in the case of high In BEP, position-controlled pyramid-like structures with the polycrystalline depositions were still observed at 480°C, which indicates still less selectivity between opening and mask areas. At 510°C, the position-controlled pyramids with several NWs over the pyramids were observed without polycrystalline deposition, which suggests a better growth condition. At 540°C, the pyramid structures became irregular, which can correspond to lower nucleation for growth. These results indicate that precise control of In flux and growth temperature is important for InAs NW formation by SA-MBE with suppression of the polycrystalline deposition.

Figure 2 shows comparison of SA-MBE grown InAs on (001), (111)B, and (110) planes. The In BEP and the growth temperature were $1 x10^{-7}$ Torr and 510°C, respectively. Figures 2(a)-(c) correspond to a growth time of 1 hour and a pitch of 500 nm, and Figs. 2(d)-(f)

correspond to a growth time of 3 hours and a pitch of 1000 nm. The tilt angle was 45° for all images. Similarly to the discussion in the previous paragraph, no polycrystalline depositions on HSQ masks were observed in the 1-hour-grown samples. The result indicates that the growth condition with certain selectivity is almost independent of the substrate orientation. In the 3-hour-grown samples, a few polycrystalline depositions were observed on the mask, however, most growth started from the openings, i.e. controlled the position. On the (001) plane, several NWs along [-111] or [1-11] directions over position-controlled pyramids were observed. Also on the (111)B plane, tetrahedrons as well as several vertical NWs over the tetrahedrons were observed. Since the top shape of the NWs was hexagonal, the side facets of the NWs could be {-110} surfaces similar to typical NWs obtained by selective area epitaxy [7-9]. Additionally, since the NWs were formed over pyramidal or tetrahedral structures, the diameter of the NWs did not seem to be determined by the diameter of initial opening holes. On the (110) plane, not only trigonal pyramids and several NWs along the out-of-plane [11-1] direction but also a few NWs along the in-plane [-111] or [1-11] directions were observed.

Figure 3(a) shows the size of NWs for a growth time of 3 hours. The length of the NWs indicates a dependency on the substrate orientation; the longest is on the (111)B plane, and the shortest is on the (110) plane. The result may be related to the number of equivalent <111>B orientations nearby the substrate surface. On the other hand, the diameter of NWs does not strongly depend on the substrate orientation. The diameter is about 300 nm. The NW size on the (111)B plane seems to be similar to that in a previous report on InAs NW SA-MBE on Si (111) [9]. Therefore, the present growth mode can be a diffusion limited growth regime, where growth is limited by the surface diffusion length of In adatoms on the HSQ mask. Figure 3(b) shows the yield of NWs, which also does not depend on the substrate orientation, and is about 10-20 %. The yield is quite lower than that in the Ref. 9. We think that this is not attributed to substrate materials, because GaAs and InAs are the same zincblende structure and different to the diamond structure like Si used in the Ref. 9. Thus, InAs growth on GaAs substrates should be controlled well rather than that on Si substrates. Actually, we employed relatively larger opening diameters and lower V/III ratio compared to the Ref. 9. In addition, in the Ref. 9, it is pointed out that NW yield can depend on accurate pattern processing. Therefore, we must tune the pattern processing and growth conditions in the future to improve the yield as well as to obtain longer and thinner NWs. However, our result also indicates the possibility of in-plane-oriented NW formation with position-controlling by using SA-MBE and (110) masked substrates, which means that it is possible to fabricate a planar NWFET without a NW dispersion process.

3. Direct fabrication of nanowire field effect transistors by selective area molecular beam epitaxy on GaAs (110) masked substrates and their characterization

According to the results discussed in the previous section, we fabricated InAs planar NWFETs on HSQ/GaAs (110) masked substrates. The pattern was different from the morphological investigation, and was one-dimensional hole-array across [1-11] with markers to obtain a parallel-NW multi-channel. The growth sequence and condition were the same as in the morphological investigation, and the growth time was 3 hours. After the growth, we formed drain and source electrodes with the lift-off process using EBL and Ti/Au evaporation. Then, we formed 35-nm-thick Al_2O_3 on the surface by atomic layer deposition with trimethylaluminum and water. Finally, we formed Ti/Au top-gate electrodes by lift-off process again. We note that there is no NW dispersion process, and we just utilize conventional device process techniques. Figures 4(a) and (b) show an SEM image of a part of a fabricated planar NWFET and a schematic illustration of its cross section, respectively. We note that the top-gate electrodes overlap with the drain and source electrodes. The typical NW diameter D and the drain-source distance L are about 300 and 700 nm, respectively. The number of bridged NWs between the drain and source N is 8-21 for 100 opening holes at present. The order is almost the same as in the morphological investigation.

Figure 5(a) shows room temperature transfer characteristics at V_D = 0.1 V of a planar NWFET (N = 17) with the inset of its output characteristics. In the output characteristics, the drain current I_D at V_G = 0 V and V_D = 1 V is about 12 mA, which corresponds to 2.3 A/mm when assuming a channel width $W = ND$ of 5.1 μm. In the transfer characteristics, there is no I_D turning off even at V_G = -20 V. We note that there is also low gate current I_G (< 0.5 nA), not shown in the figure. This no-turning-off behavior can be attributed to the thick NW diameter, for which it should be difficult to obtain full depletion of a cylindrical surface accumulation layer on InAs NW side facets and an interface accumulation layer on GaAs opening, especially on the substrate (bottom) side far from the top-gate. Furthermore, in the case of Al_2O_3/p-InAs wafers, similar no-turning-off behavior has been observed, which has been interpreted as influence of a leakage current by thermal generation or band-to-band tunneling [13]. Similar situation could take place in the present NWFETs having thick diameters. With thinner NWs, we believe that it can be possible to obtain InAs planar NWFETs with high current drivability and turning-off behavior. The transconductance g_m shows a maximum value of 25 μS around V_G = -10 V, which corresponds to 4.9 mS/mm. From the maximum g_m, we estimated the field-effect mobility μ_{FE} to be 150 cm^2/V-s using the

gradual-channel approximation: $\mu_{FE} = g_m \frac{t_{Al_2O_3}}{ND\varepsilon_{Al_2O_3}} \frac{L}{V_D}$, where $t_{Al_2O_3}$ and $\varepsilon_{Al_2O_3}$ are the Al_2O_3 thickness (35 nm) and permittivity for Al_2O_3 (8.0×10^{-11} F/m), respectively. This mobility seems quite low compared in the bulk InAs value (~ 33,000 cm^2/V-s). The low μ_{FE} and g_m can be associated with (a) contact resistance, (b) interface states between Al_2O_3 and InAs, and/or (c) the crystallographic quality of InAs NWs. Concerning (a), even the product of g_m (25 μS) and a drain-source resistance R_{DS} (110 Ω) is estimated to be 0.0028, therefore the g_m correction by the contact resistance is negligible currently. Concerning (b), the ratio between the accumulation layer capacitance C_{ac} and the interface state capacitance C_{it} is important [2-3]. Since a high C_{it} / C_{ac} ratio results in a low measured g_m, the g_m correction by C_{ac} and C_{it} can provide a high μ_{FE}. From this point of view, we need further fabrication and characterization to perform an accurate analysis. Concerning (c), the InAs/GaAs system is a lattice-mismatch system. Therefore, there are many dislocations around the interface, which can deteriorate transport properties. Furthermore, in selective area epitaxial InAs NWs, there is a possibility of stacking faults, e.g. twinning or mixing of zincblende and wrutzite [9, 14], which can also deteriorate transport properties. From this point of view, we need additional structural characterization, e.g. transmission electron microscopy. As an additional information, Fig. 5(b) shows the temperature dependence of μ_{FE} as well as the g_m maximum at V_D = 100 mV in another NWFET (N = 19). Since μ_{FE} in the measurement range is about 150-200 cm^2/V-s, we conclude that there is almost no temperature influence on μ_{FE} in the present NWFETs. We also note that there is no turning off in all the temperature range. The results suggest that there is a high-dense surface accumulation layer even at low temperatures, and then there may be high-dense interface states near the Fermi level.

4. Summary

We performed SA-MBE of InAs on GaAs (001), (111)B, and (110) HSQ-masked substrates, and investigated their morphology. We successfully demonstrated the existence of in-plane-oriented InAs NWs on GaAs (110) in certain conditions. Moreover, we directly fabricated InAs planar NWFETs on the (110) plane by SA-MBE and conventional EBL, and measured their output and transfer characteristics. The NWFETs at room temperature show I_D swing but no turning off due to the thick diameter, and a maximum μ_{FE} = 150 cm^2/V-s. Additionally, the NWFETs showed almost no temperature influence on μ_{FE} between 2 K and 300 K. The results suggest that there is a high-dense surface accumulation layer even at low temperatures.

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Figure captions

FIG. 1. SEM images showing the morphology of InAs grown on HSQ/GaAs(001) at various temperatures.

FIG. 2. SEM images showing the morphology of InAs NWs. (a)-(c) correspond to a growth time of 1 hour and a pitch of 500 nm, and (d)-(f) correspond to a growth time of 3 hours and a pitch of 1000 nm. The magnification and tilt angle are the same for all the images.

FIG. 3. (a) Size of NWs for a growth time of 3 hours, and (b) yield of NWs.

FIG. 4. (a) SEM image and (b) cross-sectional schematic illustration of a planar NWFET.

FIG. 5. (a) Transfer characteristics of a planar NWFET with the inset of its output characteristics measured at room temperature. (b) Temperature dependence of field-effect mobility (transconductance) in another planar NWFET.

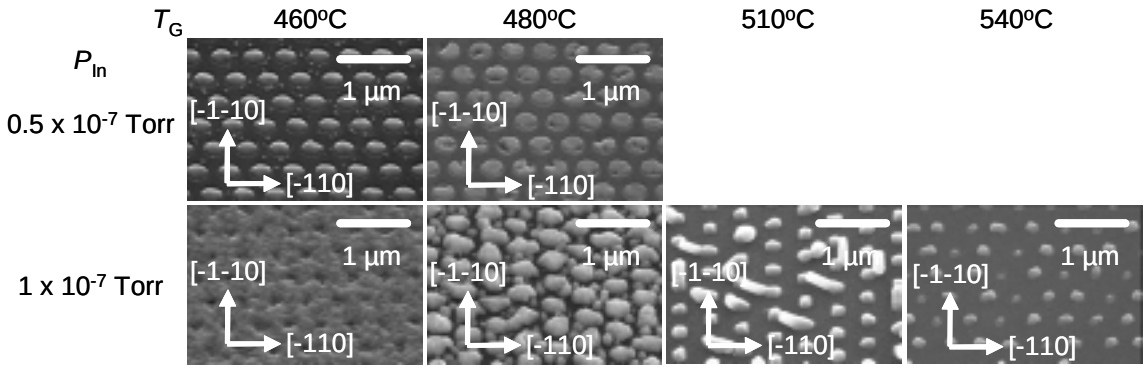

FIG. 1.

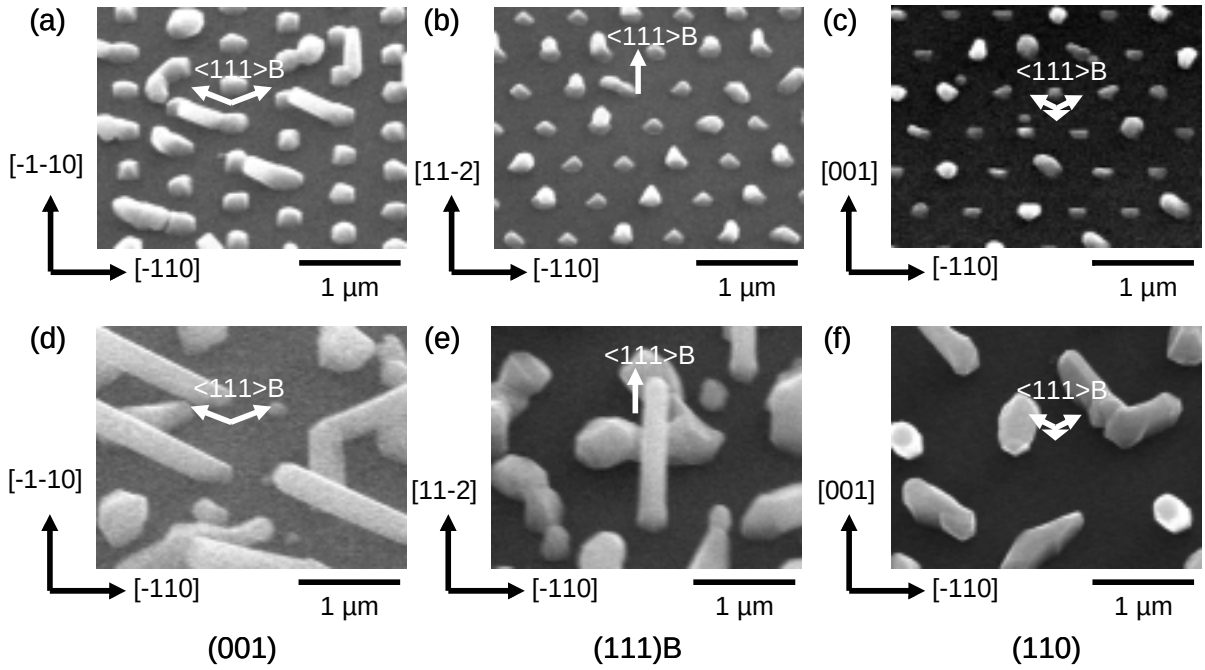
(a)
<111>B
[-1-10]
[-110]
1 µm
(b)
<111>B
[11-2]
[-110]
1 µm
(c)
<111>B
[001]
[-110]
1 µm
(d)
<111>B
[-1-10]
[-110]
1 µm
(e)
<111>B
[11-2]
[-110]
1 µm
(f)
<111>B
[001]
[-110]
1 µm
(001)
(111)B
(110)

FIG. 2.

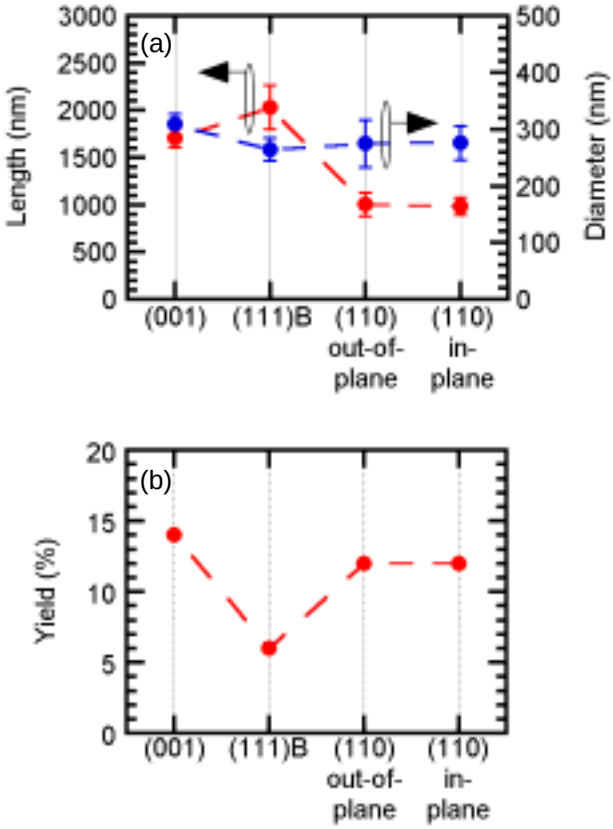
(a)
Length (nm)
Diameter (nm)
3000
2500
2000
1500
1000
500
0
500
400
300
200
100
0
(001)
(111)B
(110) out-of-plane
(110) in-plane
(b)
Yield (%)
20
15
10
5
0
(001)
(111)B
(110) out-of-plane
(110) in-plane

FIG. 3.

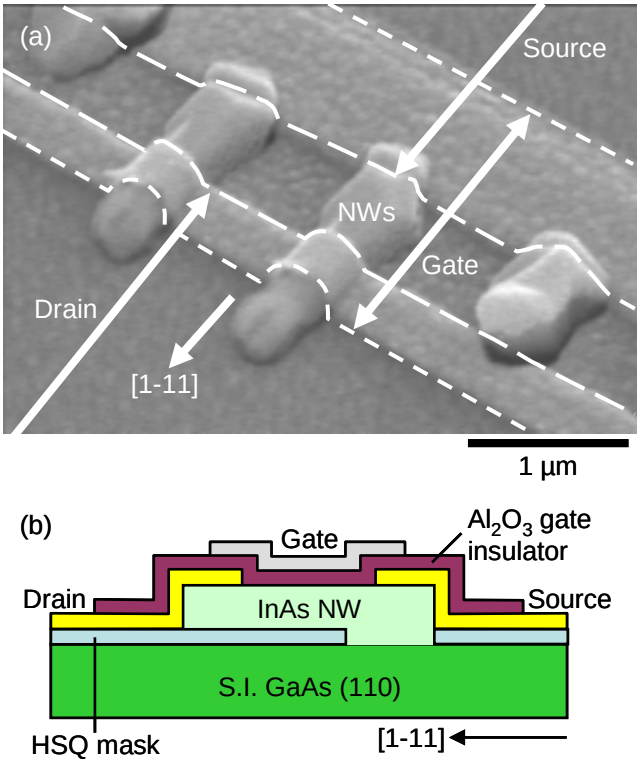
(a)
Source
NWs
Gate
Drain
[1-11]
1 µm
(b)
Gate
Al_2O_3 gate
insulator
Drain
InAs NW
Source
S.I. GaAs (110)
HSQ mask
[1-11]

FIG. 4.

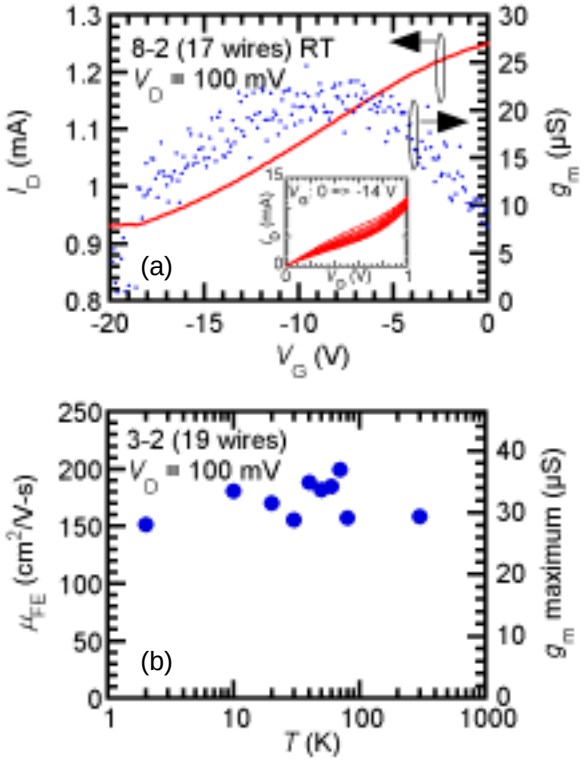
8-2 (17 wires) RT
V_D = 100 mV
I_D (mA)
g_m (μS)
V_G (V)
(a)
V_G: 0 => -14 V
I_D (mA)
V_D (V)
3-2 (19 wires)
V_D = 100 mV
μ_{FE} (cm^2/V-s)
g_m maximum (μS)
T (K)
(b)

FIG. 5.