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Area Minimization for Module Placement Including a Novel Type of Soft-module

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VLSI technology has matured to the extent that millions of transistors can be integrated within a single chip, and VLSIs are now the key to the design of electronic systems for communications, signal and information processing, etc. It follows that the complexity and difficulty of designing VLSIs are becoming larger and are now beyond manual design. Hence, the success of VLSI design relies deeply on the performance of available CAD/DA systems.

VLSI design consists of three major processes, high–level design, logic–design and layout design, and the layout design can further be separated into two tasks; placement and routing. Placement is the problem to determine absolute locations of all components within a layout region. Since the hierarchical design is widely adopted in common, subjects to be placed can be elementary devices such as transistors and resistors, gate cells such as NAND gate cell and NOR gate cell or functional blocks such as ALU, memory block and controller.

In spite of the difference of subjects to be placed and the difference of the objectives of the placement, the core problem of the placement is a rectangle packing problem; for a given set of modules $\mathcal{M}$, find a non–overlapping placement of all the modules within a bounding rectangle(chip) of minimum area. In many cases, every module in $\mathcal{M}$ is given as a rectangle with a fixed width and height, but in some cases, all of the modules or some modules among $\mathcal{M}$ are given as rectangles without fixed width nor fixed height but as ones only whose areas are specified. Latter type of module is called a soft–module.

This paper treats a module placement with soft–modules. In the previous works treating soft–modules, the widths and heights of the soft–modules are determined to minimize the chip area, subject to preserve the area of each soft–module as which is specified. However, the area of each soft–module is not always necessarily preserved as

far as the total sum of the areas of soft–modules is maintained. For example, a random logic is usually allowed to be divided into a number of modules, and such division may possibly result in a smaller chip area. In this paper, a new floorplan area minimization problem which includes such type of soft–modules is formulated and an analytical solution of it is obtained.

A floorplan is the representation of geometrical relation between rooms onto each of which at most one module is assigned. A horizontal constraint graph G_h and a vertical constraint graph G_v represent horizontal partial order and vertical partial order, respectively, of rooms(modules) of a floorplan. Each directed edge of $G_h(G_v)$ has own weight which corresponds to the width(height) of a module, and the width(height) of a chip is evaluated as the length of a longest path in $G_h(G_v)$. Floorplan area minimization considered here is the problem (*FAM*); given $m-n$ modules of fixed dimensions, n soft–modules whose total sum of areas is fixed to S, a horizontal constraint graph G_h and a vertical constraint graph G_v, find the width and the height of each soft–modules to minimize the chip area.

Since the width and the height of each soft–module are not fixed and are treated as variables, we can not find a longest path of $G_h(G_v)$ and we can only make a list of candidates for the longest path, each of which contains different set of soft–modules(the number of candidates is between $n+1$ and 2^n, which depends on the structure of $G_h(G_v)$). A candidate which does not include any soft–module is also in the list and its length is denoted as $\mathcal{W}^c_{\{\}}$ ($\mathcal{H}^c_{\{\}}$). One of the contributions of this paper is to show that, in the case which an optimum chip area is greater than $\mathcal{W}^c_{\{\}} \times \mathcal{H}^c_{\{\}}$, there exists an optimum solution(situation) in which at least n candidates for the longest path are the exact longest paths in each of G_h and G_v. On the other hand, in the case which the optimum chip area is $\mathcal{W}^c_{\{\}} \times \mathcal{H}^c_{\{\}}$ (minimum possible chip area), we can consider an alternative problem to maximize the total area of soft–modules under the chip size $\mathcal{W}^c_{\{\}} \times \mathcal{H}^c_{\{\}}$, and it is shown that the above property is held also in this problem. Note that the conversion of an optimum solution for latter problem into the one for the original problem is straightforward.

Based on the above theorem, an analytic solution of *FAM* is derived. The method utilizes the algebraic solution for every possible choice of n candidates of the longest path for each G_h and G_v. The key of this approach is that, once n candidates are selected as the longest path for $G_h(G_v)$, the width(the height) of every soft–module can be solved as a linear function of the width(the height) of the chip, and as a result we can get a second order rational function of a single variable to be minimized and the domain of the variable.

A software system for module placement with soft–modules is developed and its performance is examined. The entire system is the combination of the solver of *FAM*(proposed) and the floorplan generator. The generation of floorplans is navigated by the simulated annealing method. The experimental results show us the distinct feature that the chip area is decreasing as the number of soft–modules increases(the total area is unchanged).