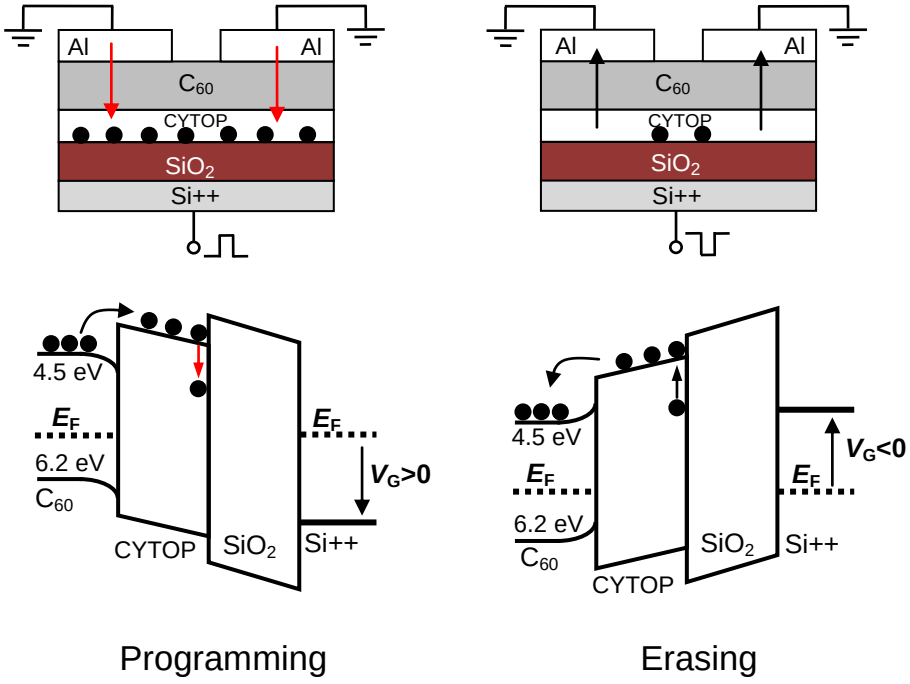
Highlights

- We report for the first time organic *n*-type nonvolatile memory transistors based on a fullerene (C_{60}) semiconductor and an electron-trapping polymer.
- The memory transistor can be programmed/erased by applying relatively low gate voltage pulses of 50/−45 V.
- The memory transistor shows a memory window of 10 V, a memory on/off ratio of 10^5, and a retention time over 10^5 s.
- The memory effect originates from trapping and detrapping electrons at a CYTOP/SiO_2 interface.

Graphical Abstract



Programming Erasing

Organic nonvolatile memory transistors based on fullerene and an electron-trapping polymer

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ABSTRACT

We report for the first time organic *n*-type nonvolatile memory transistors based on a fullerene (C_{60}) semiconductor and an electron-trapping polymer, poly(perfluoroalkenyl vinyl ether) (CYTOP). The transistors with a Si++/SiO_2/CYTOP/C_{60}/Al structure show good *n*-type transistor performance with a threshold voltage (V_{th}) of 2.8 V and an electron mobility of 0.4 $cm^2\ V^{-1}\ s^{-1}$. Applying gate voltages of 50 or –45 V for about 0.1 s to the devices induces the reversible shifts in their transfer characteristics, which results in a large memory window (ΔV_{th}) of 10 V. A memory on/off ratio of 10^5 at a small reading voltage below 5 V and a retention time greater than 10^5 s are achieved. The memory effect in the transistor is ascribed to trapped electrons at the CYTOP/SiO_2 interface. Because of the use of high-electron-mobility C_{60}, the switching voltages of our memory transistors become significantly lower than those of conventional memory transistors based on pentacene.

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Keywords:

Fullerene transistor

Nonvolatile memory transistor

Floating-gate effect

Electron-trapping polymer

1. Introduction

Electronics using organic materials has rapidly grown due to their unique and attractive features including mechanical flexiblility, low-cost and low temperature manufacturing, which are suitable for large area fabrication [1–10]. Various types of organic electronic device, such as organic solar cells [1,2], organic light-emitting diodes [3,4], organic field-effect transistors (OFETs) [5,6], and organic integrated circuits [7,8], have been fabricated. Memory devices have received considerable attention because they can be used for data/code storage in electronic circuits and as radiofrequency identification tags and microprocessors [9,10]. Memory effects can be observed in capacitor [11], resistor [12], and transistor [13] structures. Among these organic memories, transistor memories have gained considerable attention in recent years because they require the use of a single transistor structure, without loss of reading behavior; moreover, these memories can be easily embedded in integrated circuits [14–16]. The memory effects can be realized by using ferroelectric polymers such as poly(vinylidenefluoride/trifluoroethylene) [17,18]. Polarization/depolarization of the gate dielectrics would induce/deplete carriers in the transistor channel, corresponding to the logic states. However, it is hard to obtain long retention time from the devices reported thus far because of the rough surface and high leakage current of the gate ferroelectric film [15,17–19]. Another approach for constructing the organic memory transistors is to employ metals [19,20] or nanoparticles (NPs) [20,21] as floating gates. Under an external field, charges are injected and stored into the floating gate that is isolated by two insulators. Information can be presented via charge storage in the floating gate. However, fabrication of the inorganic floating gates requires vacuum

evaporation of metals or other complicated processes [19–21], which are not compatible for low cost manufacturing of organic memories.

Recently, electron-trapping polymers were demonstrated as substituted candidates for charge storage media. The memory transistors fabricated based on these materials exhibited high stability of data storage [23,24]. Moreover, because of the solution processability of these polymers, the memory devices based on them can be prepared by low-temperature fabrication; hence, the electron-trapping polymers offer promising applications in future electronic nonvolatile memory technologies. Structurally, an electron-trapping polymer is embedded as a second dielectric in a conventional pentacene transistor. Under the influence of an external field, mobile electrons are injected and captured in a thin layer of the electron-trapping polymer or at the interface between the two dielectrics [15]. The captured electrons are stable even after the electric field is removed, and this phenomenon is referred to as the nonvolatile memory effect. To release the trapped electrons, a reverse voltage must be applied to the device. Similar to the case of a floating-gate memory, charge trapping and detrapping at the trap sites modulate the conductivity of the transistor channel, resulting in different current levels. Therefore, the digital information can be encoded by the channel current levels. Baeg *et al.* fabricated a poly(α-methylstyrene) (PαMS)-based pentacene memory transistor with program/erase voltages of 200/−100 V [24]. Gue *et al.* fabricated polystyrene- or polymethylmethacrylate (PMMA)-based memory devices in which light-assisted programming and erasing processes were triggered at voltages of >40 V and −150 V, respectively [25]. Feng *et al.* observed a memory effect in transistors fabricated by dispersing nanostructured poly(9,9-dioctylfluorene) (PFO) in PMMA. However, a high voltage of 200 V and light illumination were required to switch their memory transistors

[26]. In such reported memory transistors, either pentacene [24–26] or copper phthalocyanine (CuPc) [25] has been used as an electron-transport layer (ETL) for the programming or erasing processes. Obviously, the common drawback of these structures is that electrons must move through the pentacene and CuPc films with very low electron mobility, which results in very large switching voltages [23–26]. For example, in pentacene-based OFETs, a field-effect electron mobility (0.005 $cm^2\ V^{-1}\ s^{-1}$) is much lower than a field-effect hole mobility (0.1 $cm^2\ V^{-1}\ s^{-1}$) [27]. For practical applications, the working voltages should be scaled down to the level as small as possible. Furthermore, the operation mechanism of the memory transistors has not yet been clarified, for example, the memory effect is attributed to charge trapping in the PαMS bulk or at the interface between PαMS and SiO_2 [15]. To further understand the operation mechanism, the roles of the bulk and the interface in the memory effect must be clarified.

Fullerene (C_{60}) has been widely used as a *n*-type semiconductor in OFETs [28] and as an ETL in organic electronics [29,30] due to its high electron mobility. An Al electrode is suitable for injecting electrons into C_{60} because the work function of Al (4.3 eV) [12] is close to the lowest unoccupied molecular orbital (LUMO) level of C_{60} (4.5 eV) [28,29]. Thus, the combination of Al and C_{60} is ideal for reducing the working voltage and enhancing the performance of the memory devices with an electron-trapping polymer. However, an organic memory transistor using C_{60} has never been reported.

In this article, we demonstrate *n*-type organic memory transistors based on the floating-gate-like effect that originates from electron trapping at the interface between a poly(perfluoroalkenyl vinyl ether) (CYTOP) thin film and SiO_2. In contrast to

conventional approaches where a *p*-type semiconductor is used as the ETL, the present approach involves the use of C_{60} as the active layer and the CYTOP/SiO_2 interface as the electron-trapping site, and hence, the working voltages of the memory devices can be significantly reduced. A shift in transfer characteristics of the transistors could be reversibly controlled by the applications of the external gate fields. Programming/erasing processes were realized by applying gate pulse voltages of 50/–45 V. These switching voltages were much lower than those mentioned in previous reports [24–26]. The devices had a large memory window of 10 V (ΔV_{th}, defined as a difference in threshold voltage (V_{th}) between the programmed and erased states), a memory on/off ratio of 10^5, and a retention time of $>10^5$ s, indicating stable information storage in the memory devices. Additionally, analysis of the roles of the bulk and the interface revealed that the memory mechanism was ascribed to trapping/detrapping of electrons at the CYTOP/SiO_2 interface.

2. Experimental

Figure 1 shows a cross section and an optical image of the top view of the C_{60} OFETs with a bottom-gate top-source/drain contact geometry as well as the chemical structures of C_{60} and CYTOP. The memory transistor devices were fabricated on a heavily doped Si gate electrode (n^+Si, resistivity: 1–100 Ω-cm) coated with a 50 nm SiO_2 dielectric layer. The silicon wafer was cleaned by ultrasonication (in acetone for 5 min, in detergent for 10 min, twice in pure water for 5 min, and in isopropanol for 10 min) and subjected to UV-O_3 treatment. A CYTOP electron-trapping layer (CTL-809 M, Asahi Glass) was spin-coated onto the gate dielectric at 2000 rpm for 60 s using a 0.5 wt% CYTOP solution (CT-Solv. 180) and dried at 100 °C for 2 h. All spin-coating and

heating processes were carried out in a class 100 clean room environment. The thickness of the CYTOP layer was estimated to be ~10 nm by an atomic force microscope (AFM) (VN-8000, KEYENCE). A 50-nm-thick C_{60} layer (Nanom purple SUH with purity of 99.9%, Frontier Carbon Corp., Japan) was thermally deposited onto the CYTOP layer through a shadow mask at a base pressure of 2×10^{-6} torr and a deposition rate of 0.1 nm s^{-1}. Al source-drain electrodes were formed by thermal evaporation at a deposition rate of 3 nm s^{-1} through a shadow mask under a pressure of 7×10^{-6} torr. The thickness of the Al electrodes was 70 nm. For comparison, the transistor devices without the CYTOP layer were also prepared. The channel length (L) and width (W) of all the devices were set at 75 and 5000 μm, respectively.

In order to examine current transport characteristics through the CYTOP thin film, a multilayer device with the structure of glass substrate/ITO (150 nm)/C_{60} (50 nm)/CYTOP (10 nm)/C_{60} (50 nm)/Al (70 nm) and a device without CYTOP were fabricated. All fabrication processes of the devices were set to be similar to those used for the organic memory transistors. The active area of the multilayer devices was 4 mm^2.

Electrical measurements of the devices were performed using a Keithley 4200 semiconductor characterization system in a dry nitrogen atmosphere at room temperature in a dark probe station.

3. Results and Discussion

Figure 2 shows the typical electrical characteristics of the organic transistors. For the output behavior, the drain current (I_D) of the transistors increased at a positive gate voltage (V_G). In the linear region of the graph, I_D showed a linear increase at a low drain voltage (V_D), implying efficient electron injection at the C_{60}/Al interface. Then, I_D

saturated at a high V_D because the conducting channel was pinched off. These curves indicated that the transistor devices showed standard *n*-channel field-effect operation. The gate current (I_G) measured during the transfer characterization was very small, indicating negligible leakage current (Fig. 2b).

The field-effect electron mobility (μ) was calculated by fitting the $I_D^{0.5}$ versus V_G curves using the saturation-regime equation [31]:

$$I_{D,sat} = \frac{WC_i}{2L}\mu(V_G - V_{th})^2, \quad (1)$$

where $I_{D,sat}$ is the saturation drain current and C_i is the capacitance per unit area of the gate dielectric. C_i was estimated to be 50 nF cm^{-2} from the dielectric constants of the SiO_2 (3.9) and CYTOP (2.1) and their film thickness. The V_{th} value was determined from the intercept at $I_D^{0.5}$=0 in the plot of $I_D^{0.5}$ versus V_G (Fig. 2b). The estimated V_{th}, μ, and on/off current ratio were found to be 2.8 V, 0.4 cm^2 V^{-1} s^{-1}, and 6×10^4, respectively, which were reasonable values for C_{60} OFETs [32,33]. The experimental results suggested that the presence of the electron-trapping polymer CYTOP does not affect the C_{60} OFET characteristics.

The programming and erasing characteristics of the memory transistors are shown in Figs. 3a and 3b. The transfer curve significantly shifted to a positive V_G region when a V_G of 50 V was applied for about 0.1 s, causing an increase in V_{th} from 2.8 to 12.8 V (programmed state). Subsequently, upon applying a reverse V_G of −45 V for about 0.1 s, the transfer curve returned to the initial position (erased state). In both cases, the source-drain electrodes were grounded. The direction of the transfer curve shift corresponding to the polarity of the applied voltages indicated trapping/detrapping of electrons in the devices. The programming/erasing operation was repeatable many times. In addition,

the I_G values observed during the programmed and erased states were not changed significantly (Fig. 2b), suggesting that there was no dielectric breakdown during the programming/erasing processes. The estimated ΔV_{th} was as large as 10 V (Fig. 3b), clearly indicating that the memory effect was pronounced in our memory transistors [22,24].

In our memory transistors, five possible mechanisms can be considered for the memory effect: (1) charge trapping at grain boundaries of C_{60} [34], (2) slow alignment of permanent dipole in the CYTOP bulk film, (3) charge trapping in the CYTOP bulk, (4) charge trapping at the CYTOP/C_{60} interface, and (5) charge trapping at the CYTOP/SiO_2 interface [35]. By analyzing of the AFM topographic images of C_{60} films on SiO_2 and CYTOP, we confirmed that contribution of the charges trapping caused by grain boundaries of C_{60} was not dominant in our devices (see Fig. S1 for the AFM images, Supporting Information). Notably, under the same experimental conditions, the change in the transfer curves for the device without CYTOP was small and not reproducible (see Fig. S2 for the transfer curves, Supporting Information). The large shift in ΔV_{th} observed for the memory transistors is thus due to the presence of CYTOP. The function of CYTOP might be similar to that of PαMS demonstrated by Baeg *et al.* (charge trapping in the PαMS bulk or at the interface of PαMS is proposed to be responsible for the memory effect [15,24]). Kalb *et al.* reported that there was no change in transfer curves for a transistor with a ITO/CYTOP/pentacene/Au structure even after application of gate bias stress for 2 h at $V_G = \pm 70$ V [36]. If slow dipole polarization or charge trapping in the CYTOP bulk takes place, a hysteresis of the transfer curves should be observed in the reported device. Jang *et al.* [33] demonstrated that there is no hysteresis in transfer characteristics of a Si/CYTOP/C_{60}/Au transistor,

i.e., no charge trapping occurs at the CYTOP/C_{60} interface. Thus, we assume that the charge trapping at the CYTOP/SiO_2 interface is convincingly attributed to the memory effect.

This mechanism is valid only if electrons can be injected from C_{60} to CYTOP and they reach the CYTOP/SiO_2 interface. To obtain the evidence for electron injection into CYTOP, the current density–voltage (*J*–*V*) characteristics of the ITO (150 nm) bottom anode/C_{60} (50 nm)/CYTOP (10 nm)/C_{60} (50 nm)/Al (70 nm) top cathode device were measured and compared with the device without CYTOP. As shown in Fig. 4, a current flows through the multilayer devices, i.e., electrons can pass through the 10-nm-thick CYTOP layer. The memory effect due to the charge trapping at the CYTOP/SiO_2 interface was also confirmed by analyzing the capacitance-voltage (*C*−*V*) curves of the metal-insulator-semiconductor capacitor (see Fig. S3 for the *C*−*V* curve, Supporting Information). The clear hysteresis in the *C*−*V* curves was observed and the shift direction of the *C*−*V* curves in the MIS capacitor was consistent with that of I_D-V_G curves of the respective memory transistor. The origin of the electron trapping site at the CYTOP/SiO_2 interface is not clearly understood yet. However, if no SiO_2 is used, such trapped electrons may be released very fast and neutralized at the gate electrode because the use of SiO_2 can reduce I_G. The presence of the double insulating layers of CYTOP and SiO_2 is indispensable to obtain the memory effect.

Based on these results, the proposed operation mechanism of the memory transistors is presented in Fig. 5. When a positive pulse is applied to the Si^{++} gate electrode, electrons are injected from Al through C_{60} and CYTOP and then trapped at the CYTOP/SiO_2 interface (Fig. 5a). This causes the depletion of intrinsic carriers in the C_{60} channel, thus inducing the shift in V_{th} to a positive value. In contrast, the trapped

electrons are removed from the interface under a negative gate pulse voltage. Consequently, the memory transistor reverts to the initial condition (Fig. 5b). The trap site at the interface between the CYTOP and SiO_2 insulators behaves as like a floating gate.

The changes in the transfer curves of the memory transistors at various gate pulse voltages are presented in Fig. S4 (Supporting Information). Figures 6a and 6b show the dependence of V_{th}, μ, and ΔV_{th} on the gate pulse voltages. During programming, V_{th} remained constant up to 30 V and then increased beyond 40 V. The shift in V_{th} nearly saturated at the gate pulse voltages higher than 50 V, presumably because all trap sites at the interface are filled with electrons. Meanwhile, during erasing, V_{th} gradually decreased with the increase in the negative voltage. Since the application of the negative voltage of −45 V causes complete removal of the trapped electrons from the interface, V_{th} reverts to its initial value. The estimated μ of the transistors remained almost constant upon the application of these gate pulse voltages.

From Fig. 6a, the programming/erasing operation can be completed by 50/−45 V, respectively. These values are about 50 V lower than those reported for polymer-based devices [24–26] and also 30 V lower than those of memory transistors fabricated using Au NPs [21,22]. We suggest that the switching voltages can be further reduced by using a thinner SiO_2 layer or by replacing the insulating layer with a high-k dielectric.

The total number of trapped electrons at the interface can be estimated by using the equation:

$$\Delta N = \frac{C_i \Delta V_{th}}{e}, \qquad (2)$$

where e is the elementary charge. The value of ΔN is calculated to be 3.1×10^{12} cm^{-2}. This ΔN is equal to that for an Au NP floating gate in the memory transistors [22].

The changes in the ΔV_{th} of the memory transistors as a function of pulse width were investigated and shown in Fig. 7. The devices were programmed/erased by applying the optimized gate pulse voltages of 50 and −45 V, respectively, for different applied time while the source-drain electrodes were grounded. At the programming stage, ΔV_{th} was unchanged up to 1 ms and then increased beyond 0.05 s. The pulse duration of 0.1 s is the critical time to reach maximum ΔV_{th}. On the other hand, at the erasing stage, ΔV_{th} gradually decreased with the increase of the applied time. Slightly shorter pulse width of 0.09 s can erase the memory window.

In our devices, electrons must pass through the CYTOP layer. Therefore, the thickness of the CYTOP film is a key factor for the device performance. To address this, we fabricated and evaluated the memory transistors with the different thickness of the CYTOP layer. The gate pulse voltages of 50 and −45 V were utilized to program and erase the devices. As shown in Fig. 8a, the ΔV_{th} strongly decreased with increasing the thickness of the CYTOP layer. The memory effect was clearly observed with the CYTOP thickness smaller than 30 nm. This is because electron injection can take place in the case of the smaller CYTOP thickness. When using the CYTOP thickness larger than 50 nm, the ΔV_{th} did not change because it is very difficult to inject electrons across the thick CYTOP layer.

Figure 8b shows the dependence of ΔV_{th} on the calculated electric fields, which were calculated by simply dividing the gate voltages (50 and −45 V) by the total thickness by the layers of C_{60}, SiO_2 and CYTOP. Figure 8b indicates that the applied

electric fields of 4.5 and 4.1 $MVcm^{-1}$ are required to program and erase the memory transistors to obtain the ΔV_{th} of 10 V.

In order to demonstrate the long-term stability of the memory transistors, the retention time measurement was conducted. The memory transistors were programmed/erased by applying the gate pulse voltages of 50/−45 V, and then I_D under the programmed and erased states was continuously measured for 10^5 s at a V_D of 4 V and a V_G of 5 V (Fig. 9). The logical values of "1" and "0" are defined by the low and high I_D states, respectively. The initial memory on/off ratio was ~10^5, which was equal to that of the PαMS-based device [24]. In our devices, the CYTOP and SiO_2 insulators prevent detrapping of electrons stored at the interface. As the result, the memory on/off ratio remained 6.2×10^4 even after 10^5 s, which is one of the largest values ever reported [13,17–19,24–26]. The obtained large memory on/off ratio enables the "1" and "0" values to be clearly distinguished in the reading circuit. Moreover, it is interesting to note that the reading voltages of our devices are much lower than those of the reported organic memory transistors [21, 22, 24–26] and consistent with the transistor-transistor logic (TTL) level (5 V).

4. Conclusions

In summary, we have demonstrated low-working-voltage and long-lifetime *n*-type memory transistors based on C_{60} and CYTOP. The transistors showed very good *n*-type performance with a V_{th} of 2.8 V and a μ of 0.4 $cm^2\ V^{-1}\ s^{-1}$, respectively. The I_D of the transistors was modulated by trapping/detrapping of electrons at the CYTOP/SiO_2 interface (a floating-gate-like memory effect). The required program/erase voltages

were 50/−45 V, which resulted in a large ΔV_{th} of 10 V. An on/off ratio of 10^5 was obtained at a V_D of 4 V and a V_G of 5 V. The memory transistors showed very long retention time characteristics with a retention time longer than 10^5 s. The reading voltages were adaptable to the available TTL level. From the experimental results, we suggest that C_{60} can be substituted for the conventional pentacene semiconductor for memory transistor fabrication. The memory transistors based on C_{60} and CYTOP have a variety of applications such as nonvolatile memories, controllable V_{th} transistors for organic integrated circuit manufacturing [37], and combination with the *p*-type memory transistors to build tunable complementary inverter circuits [38].

Acknowledgement

The authors thank Prof. Heisuke Sakai (Waseda University) for fruitful discussion. This work was partially supported by a Grant-in-Aid (Grant No. 20241034) and Scientific Research on Innovative Areas “pi-Space” (Grant No. 20108012) from the Ministry of Education, Culture, Sports, Science, and Technology, Japan. D. T. T. gratefully acknowledges financial support by a 322 Scholarship (doctoral course) of the Vietnamese Government.

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Figure captions

Fig. 1. (Color online) Schematic illustration of cross section (left) and optical microscope image of top view (right) of memory transistors and chemical structures of C_{60} and CYTOP.

Fig. 2. (Color online) (a) Output and (b) I_D–V_G, I_G–V_G, and $(I_D)^{0.5}$–V_G curves of memory transistors.

Fig. 3. (Color online) (a) I_D–V_G, I_G–V_G, and (b) $(I_D)^{0.5}$–V_G curves of memory transistors in programmed and erased states. Programming and erasing operations were performed by applying gate pulse voltages of 50 and –45 V, respectively, while source-drain electrodes were grounded.

Fig. 4. (Color online) J–V curves of multilayer devices. Observation of current flow through devices suggests that electrons can pass through 10-nm-thick CYTOP layer under high electric field.

Fig. 5. (Color online) Operation model for memory transistors: (a) programming and (b) erasing processes. Top figures show schematic representations of programming/erasing operations, and bottom figures show corresponding energy diagrams. (•) stands for electron. Arrows indicate directions of electron movement. E_F implies Fermi level.

Fig. 6. (Color online) Change in (a) V_{th} and μ and (b) ΔV_{th} of memory transistors as function of gate pulse voltages. Devices were programmed/erased by changing magnitude of gate pulse voltage while source-drain electrodes were grounded. Width of each pulse was about 0.1 s.

Fig. 7. (Color online) Change in ΔV_{th} of memory transistors as function of pulse width. Devices were programmed/erased by applying gate pulse voltages of 50 and −45 V, respectively, for different applied time while source-drain electrodes were grounded.

Fig. 8. (Color online) (a) CYTOP thickness dependence of ΔV_{th}. Gate pulse voltages of 50 and −45 V were used to program or erase devices while source-drain electrodes were grounded. (b) Dependence of ΔV_{th} of memory transistors on applied electric field.

Fig. 9. (Color online) Retention time characteristics of I_D in programmed and erased states. Programming/erasing processes were carried out by applying gate pulse voltages of 50 and −45 V, respectively, while source-drain electrodes were grounded. I_D was continuously measured at a V_D of 4 V and a V_G of 5 V.

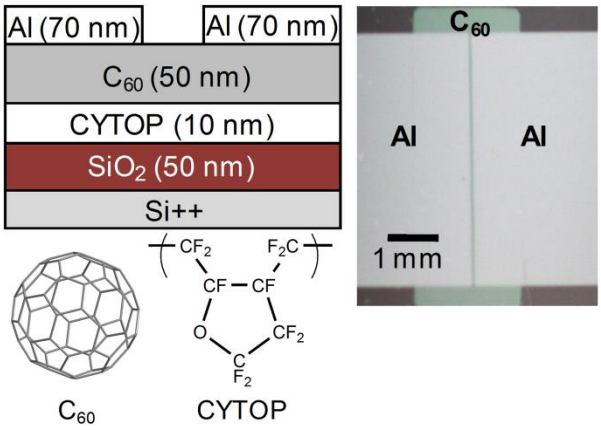

Fig. 1.

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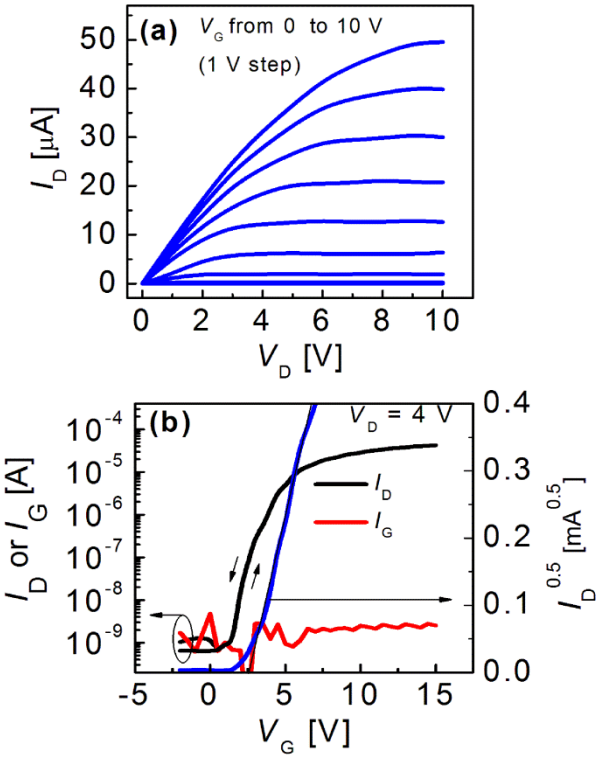

Fig. 2.

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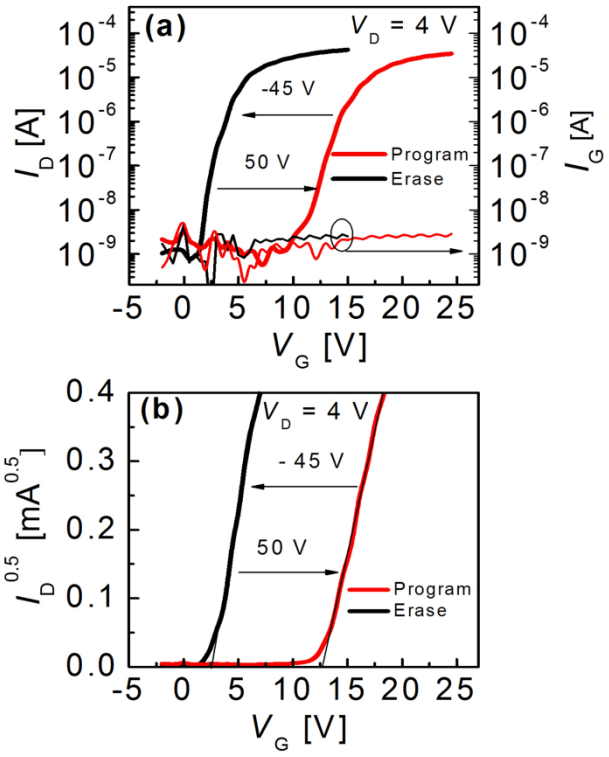

Fig. 3.

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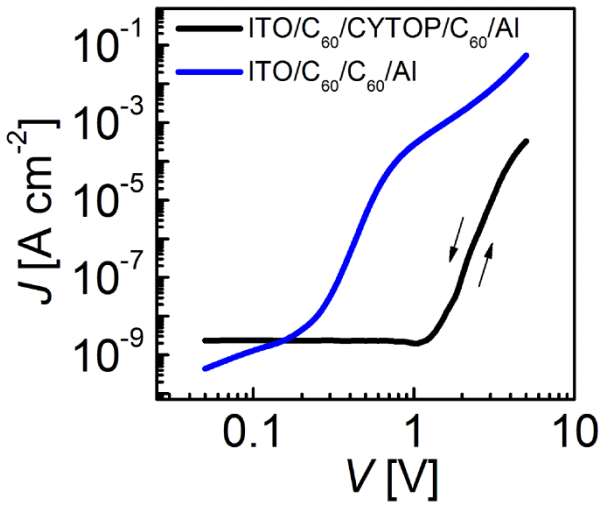

Fig. 4.

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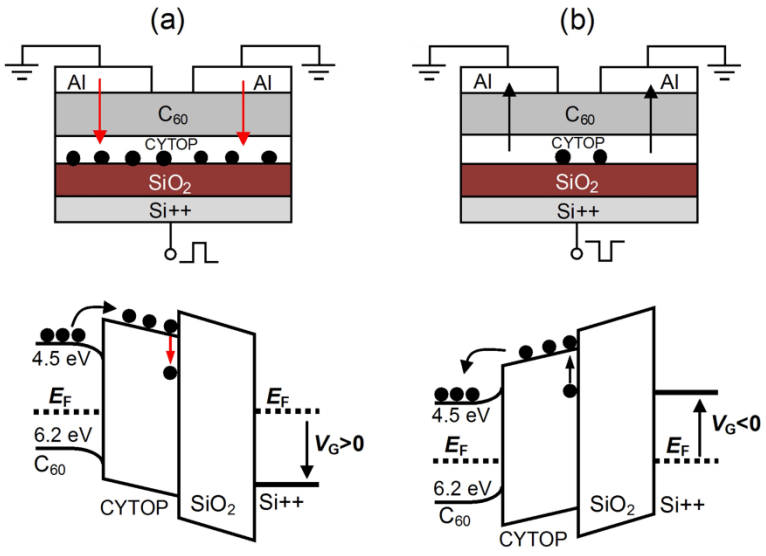

Fig. 5.

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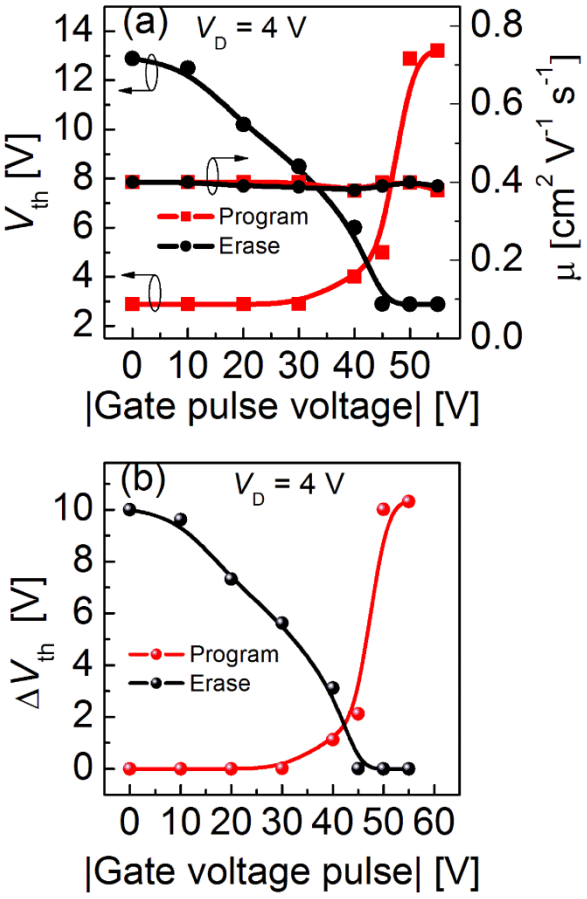

Fig. 6.

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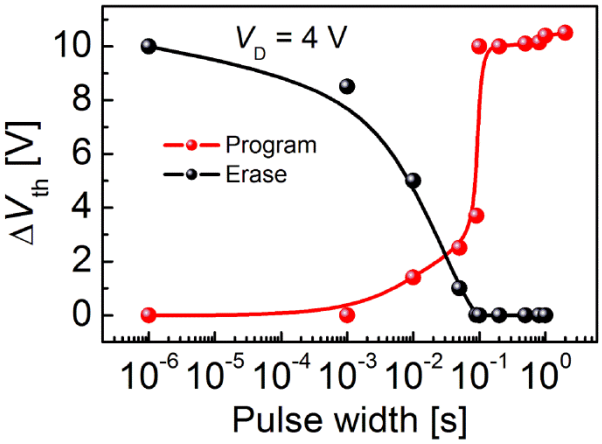

Fig. 7.

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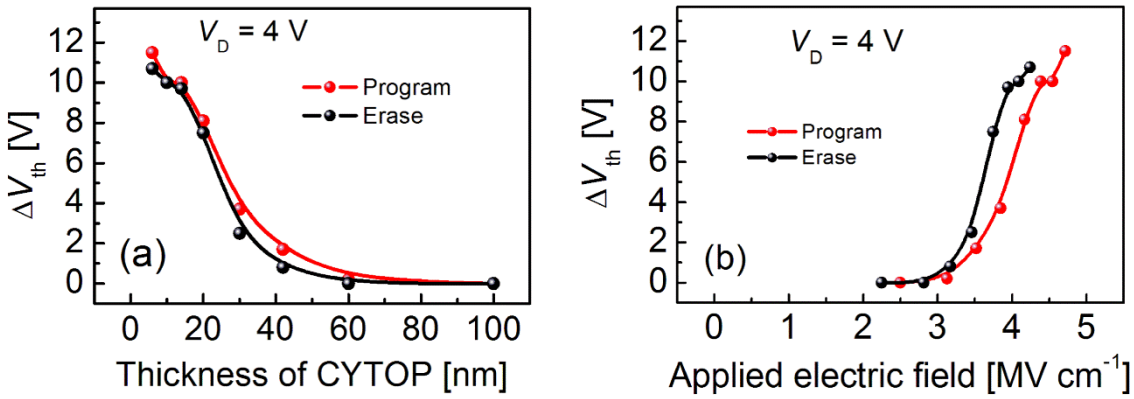

Fig. 8.

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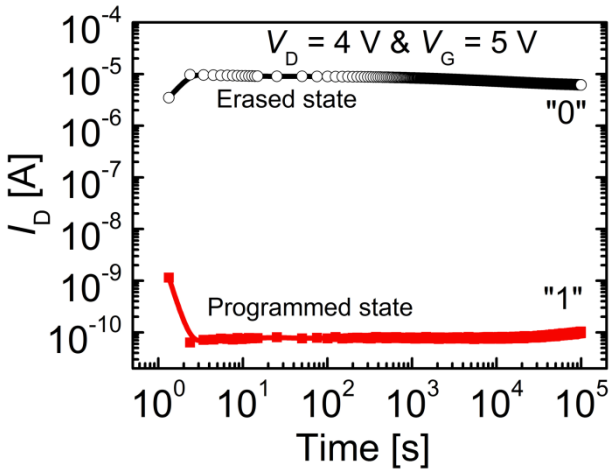

Fig. 9.

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