A Design Method of Mixed Synchronous-Asynchronous Circuit

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Most of the digital circuits are categorized into the synchronous circuit which uses a clock signal to alter its internal state such that a digital signal is latched by a flip-flop in the timing specified by a clock signal. Therefore, even if a digital signal suffers from "hazard" in between two consecutive raising edges of a clock signal, a correct signal is successfully latched if the signal reaches its final value before the raising edge arrives. In addition, it is also a good point of a synchronous circuit that the behavior of a circuit is easily verified by a cycle-based verifier/simulator. However, as the device size shrinks further and the system size becomes lager, delay variation becomes larger due to the variations of device parameters during fabrication process, the change of operating environment, etc. As a result, a synchronous circuit which is controlled by a global clock fails easily in timing of latching signal. On the other hand, an asynchronous circuit doesn't use a clock signal, but uses handshake signals between components. Hence, an asynchronous circuit can realize a highly reliable system in which delay variation never causes timing error. However, since the handshake protocol becomes a time overhead, it is hard to improve a speed performance. Also, the area overhead of an asynchronous circuit tends to be large since the arrival of a signal is recognized with the change of signal value during the handshake protocol and hence a hazard-free circuit design is mandatory.

As a conclusion, it is expected that a synchronous circuit has an advantage against an asynchronous circuit in case we will design a small-size circuit having relatively small signal delays in it, and the opposite in other cases including a large-size circuit having relatively large signal delays, and a circuit having signal delays which very vastly depending on input data.

In this research, we have studied the mixture of synchronous and asynchronous circuits for realizing a high performance digital circuit under delay variation environment by bringing out the strengths of each circuit. Globally Asynchronous Locally Synchronous system (GALS) is known as one possible configuration of the mixture of synchronous and asynchronous circuits. We have studied a more general configuration including GALS, and provided an important basis for future discussions on the deep optimization of the mixture of synchronous and asynchronous circuits.

Usually, a synchronous data path circuit is controlled by a finite state machine (FSM), while an asynchronous data path circuit in controlled by a network of so-called Q-elements (Q-network), where Q-element is a macro circuit which manages the handshake between two registers. We followed these schemes to control a mixed synchronous-asynchronous circuit, and introduced additional control structures between FSM and Q-network in order to establish the collaboration between them. "Controller Behavior Graph (CBG)" has been introduced for representing whole structure of a controller for a mixed synchronous-asynchronous circuit. Next, we have designed a novel register which can realize data sharing between a synchronous part and an asynchronous part. The register can latch both data in a synchronous part(it was one line per bit, and the latch operation is triggered by a clock signal) and data in a asynchronous part (it uses two lines per bit, and the latch operation is trigged by an asynchronous handshake signal), and provide the latched data to both synchronous and asynchronous parts. It makes data sharing and register sharing between synchronous and asynchronous parts possible.

On the other hand, if asynchronous operations are going to share the signal path with synchronous operations, the signal path used by synchronous operations should be initialized before asynchronous operations use this path. However any proper way to initialize such signal path is not found. Hence we limited our design so that synchronous operations

use distinct sets of functional units. The proposed design procedure of a mixed synchronous-asynchronous circuit is summarized as follows. (1)For a given application algorithm to be implemented, each operation is assigned to either synchronous operation or asynchronous operations. (2)Schedule synchronous operations into control steps, (3)generate the initial CBG, (4)determine resource assignment (FU binding and register binding) and append extra control structures to the CBG for resolving timing problems induced by resource sharing. Finally, data path net list is generated based on the input application algorithm and resource assignment, and the controller which contains FSM, Q-network and interconnection between them is configured based on the CBG.

Moreover, we have developed a macro-timing simulator for checking the behavior and evaluating the speed performance of a mixed synchronous-asynchronous circuit. It enables us to verify all events which occur during the execution of an application algorithm under the specified delay value in each component. The simulator can be combined with Monte Carlo simulation to compute the statistical distribution of the execution time of a given application. Finally, we have demonstrated a design example and applied our simulator to the designed circuit. we have set different average delay to a synchronous FU and an asynchronous FU, and carried out Monte Carlo simulations (10000 trials per one set of average delay assignment to FF). Through this simulation, we have found several characteristics of a mixed synchronous-asynchronous circuit, and the difference of the execution time of the input application caused by the difference of the average delay between synchronous and asynchronous operations.

The future problems include the development of a clear criterion for separating operations in an application into synchronous operations and asynchronous operations, and a design optimization method in the high-level synthesis framework. Also it is necessary to contrive more efficient control structure because the connection and the handshake between the synchronous and the asynchronous controllers become unnegligible overhead for the whole circuit.