AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors using BN and AlTiO high-k gate insulators

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Doctoral Dissertation

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Abstract

GaN-based metal-insulator-semiconductor heterojunction field-effect transistors (MIS-HFETs) have been investigated owing to the merits of gate leakage reduction and passivation to suppress the current collapse. Gate insulators, such as Al_2O_3, HfO_2, TiO_2, or AlN, have been studied. Further developments of the MIS-HFETs using novel gate insulators suitable according to applications are important. A desired gate insulator should have:

- wide energy gap E_g and high breakdown field F_{br} for high voltage operation,
- high dielectric constant k for high transconductance, and
- high thermal conductivity κ for good heat release suitable for high power operation

In particular, boron nitride (BN) and aluminum titanium oxide (AlTiO: an alloy of TiO_2 and Al_2O_3) are promising candidates owing to their advantageous properties, as shown below.

In this work, we characterized physical properties of amorphous BN thin films obtained by RF magnetron sputtering, which have $E_g \sim 5.7$ eV, $F_{br} \sim 5.5$ MV/cm, and $k \sim 7$. Using the BN films, we fabricated BN/AlGaN/GaN MIS-HFETs (BN MIS-HFETs), which exhibit very low gate leakage, indicating good insulating properties of BN. We obtain high maximum drain current I_D and no negative conductance, suggesting good thermal release properties owing to the excellent κ of BN. We elucidated temperature-dependent channel conduction, where I_D decreases with increase in temperature. In the linear region, the decrease in I_D is attributed to decrease in the electron mobility, while the sheet electron concentration is constant. In the saturation region, the decreased I_D is proportional to the average electron velocity, whose temperature dependence is in-between those of the low- and high-field velocities. Furthermore, we elucidated the temperature-dependent gate leakage, attributed to a mechanism with temperature-independent tunneling, dominant at low temperatures, and temperature-enhanced tunneling, dominant at high temperatures, from which we estimated the BN/AlGaN interface state density, which is $\gg 10^{12}$ $cm^{-2}eV^{-1}$. High-density BN/AlGaN interface states lead to the weak gate controllability for the BN MIS-HFETs.

We also characterized physical properties of Al_xTi_yO thin films obtained by atomic layer deposition, for several Al compositions $x/(x+y)$. We observe increasing E_g and F_{br}, and decreasing k with increase in the Al composition. Considering the trade-off between k and F_{br}, we applied Al_xTi_yO with $x : y = 0.73 : 0.27$, where $E_g \sim 6$ eV, $F_{br} \sim 6.5$ MV/cm, and $k \sim 24$, to fabrication of AlTiO/AlGaN/GaN MIS-HFETs (AlTiO MIS-HFETs). In comparison with Al_2O_3/AlGaN/GaN MIS-HFETs, the AlTiO MIS-HFETs exhibit higher maximum I_D, higher peak and better linearity of transconductance, shallower threshold voltage, and higher gate leakage (but still very low), suggesting that AlTiO is more favorable

than Al_2O_3 for applications to AlGaN/GaN MIS-HFETs. We investigated temperature-dependent channel conduction of the AlTiO MIS-HFETs, where I_D decreases with increase in temperature. In the linear region, the decrease in I_D is mainly due to decrease in the electron mobility, while the contact resistance and the sheet electron concentration are almost constant. In the saturation region, the decreased I_D is proportional to the average electron velocity, whose temperature dependence is in-between those of the low- and high-field velocities. Temperature-dependent channel conduction of the AlTiO MIS-HFETs is similar to that of the BN MIS-HFETs. Moreover, we observe bumps in gate current for high drain-source voltages and high I_D, indicating increase in channel temperature due to self-heating effects at high power consumption. This suggests low κ of AlTiO due to random effects in alloy materials. In addition, we elucidated the temperature-dependent gate leakage, attributed to a mechanism with two terms. One is temperature-independent tunneling, dominant at low temperatures. The other exhibits Poole-Frenkel mechanism, dominant at high temperatures, from which we estimated AlTiO/AlGaN interface state density, which is $\sim 2 \times 10^{12}$ $cm^{-2}eV^{-1}$. Low-density AlTiO/AlGaN interface states lead to the strong gate controllability for the AlTiO MIS-HFETs.

Finally, we concluded that AlTiO films have low thermal conductivity, but low interface state density in comparison with those of BN films.

Keywords: AlGaN/GaN, MIS-HFET, BN, AlTiO, channel conduction, gate leakage, interface state

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Chapter 1

Introduction

1.1 Trends of semiconductor industry

After the statement of Gordon Moore about the increasing rate of device packing, the number of components per integrated circuit or the density of transistors on a chip has doubled every two years since 1970s [1]. Figure 1.1 shows the evolution of transistor gate length (minimum feature size) and the density of the transistors in microprocessors over time [2]. The reducing the size of the transistors allows an increase in their density on a chip, which will increase the functionality of the circuit for a constant chip size. This has resulted in a reduction of the relative manufacturing cost per function, enabling the production of more complex circuits on a single substrate. However, there are other reasons for making the transistors smaller. Doubling the density of transistors on the same chip area indicates that the transistor sizes are scaled down. The benefits of the device size scaling was first introduced by Dennard *et al.* in 1974 [3]. Based on the assumption of maintaining a constant electric field, they exhibited scaling results for circuit performance as the device scaled down by a factor of β shown in Tab. 1.1. The trend of miniaturization based on the reduction of the device sizes is called "More Moore", described in Fig. 1.2.

Table 1.1: Scaling results for circuit performance [R. Dennard *et al.*].

Device or circuit parameter	Scaling factor
Device dimension d, L, W	$1/\beta$
Doping concentration N_{a}	β
Voltage V	$1/\beta$
Current I	$1/\beta$
Capacitance $\varepsilon A/d$	$1/\beta$
Delay time/circuit VC/I	$1/\beta$
Power dissipation/circuit VI	β^2
Power density VI/A	1

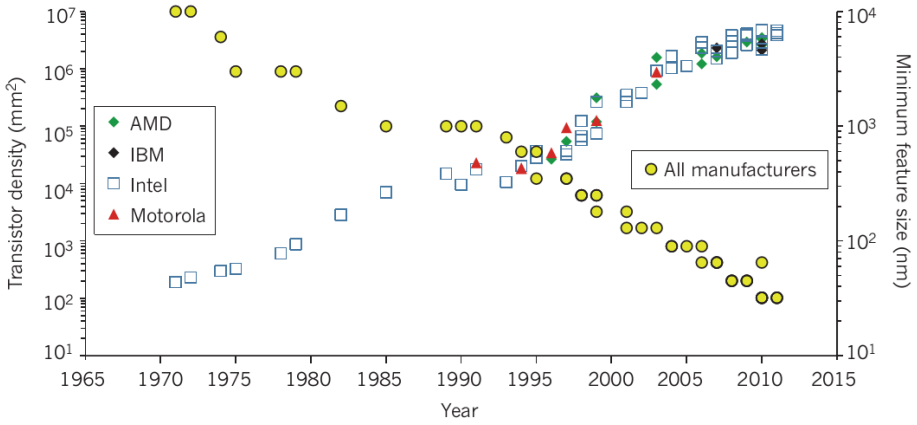


Figure 1.1: The evolution of transistor gate length (minimum feature size) and the density of transistors in microprocessors over time. Diamonds, triangles and squares show data for the four main microprocessor manufacturers: Advanced Micro Devices (AMD), International Business Machines (IBM), Intel, and Motorola [I. Ferain *et al.*].

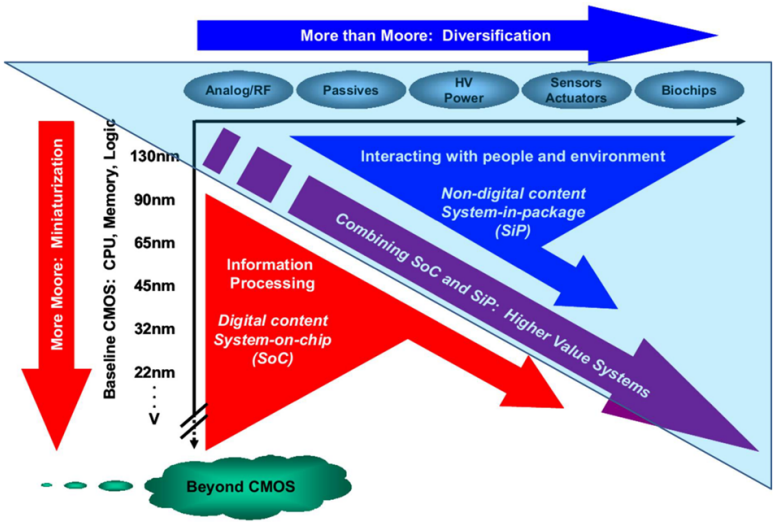


Figure 1.2: The dual trend in the International Technology Roadmap for Semiconductors (ITRS): miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore") [ITRS 2011].

Unfortunately, the scale down to "More Moore" trend will soon face its limitation at very small device sizes. By reducing the device size, we can obtain higher operation speed. However, driving voltage and power should be also decreased to maintain electric field lower than breakdown value. For analog devices in some fields, especially in telecommunication or automobile, where high voltage and high power are important requirements, the voltage and power can not be lower than a minimum value. For example, to transmit a power of 1 W through transmission lines with $\sim 50\ \Omega$ characteristic impedance in wireless communication, the voltage swing is determined ~ 10 V [4]. This exceeds the breakdown voltage of 0.1-μm FETs on silicon or GaAs, the channel length needed for millimeter wavelength applications. Therefore, in order to increase the performance for devices, new technologies have to be developed.

In order to enhance device performance without following of scaling requirements, the other trend of the semiconductor industry, called "More than Moore" (MtM), has been investigated, as shown in Fig. 1.2 [1]. This trend is characterized by functional diversification of semiconductor-based devices. The MtM contributes to the miniaturization of electronic systems by provide additional value into the systems and allow for the non-digital functionalities to migrate from the system board-level into the package (SiP) or onto the chip (SoC).

MtM trend is much more important for several applications employed active devices, such as analog/RF, e.g., wireless communication, and HV power, e.g. power switching, which are required to operate at high speed and high power. High-speed operation increases the communication rate, which is effective usage of frequency resources. In addition, high-power operation enhances long-range communication, high-efficiency, and miniaturization of the systems [5]. Therefore, to enhance the performance of the wireless communication systems, high-speed and high-power semiconductor active devices are important. Figure 1.3(a) exhibits a relation of RF power and frequency (speed) for several wireless-communication applications [6]. Similarly, the requirements are also hold for HV power applications. Fig. 1.3(b) shows relation of RF power and frequency for several power-switching applications [7]. From these figures, we can see that the devices which are required to operate at high speed can not transfer high power. On the other hand, the devices which are required to transfer high power can not operate at high speed. Although there is a trade-off between speed (frequency) and power for both applications, wide-gap semiconductor devices, such as GaN-based devices, have potentials to overcome the trade-off.

We discuss in details the trade-off between speed and power from material points of view. For high speed, high electron mobility and saturation velocity are preferred, in which electron mobility μ is given by

$$\mu = \frac{e\tau}{m^*},$$

and saturation velocity v_{sat} is given by

$$v_{\mathrm{sat}} \sim \sqrt{\frac{\hbar\omega_{\mathrm{op}}}{m^*}},$$

with electron charge e, relaxation time τ, optical phonon energy $\hbar\omega_{\mathrm{op}}$, and electron effective mass m^* [8]. In this sense, small m^* is advantageous. On the other hand, for high power,

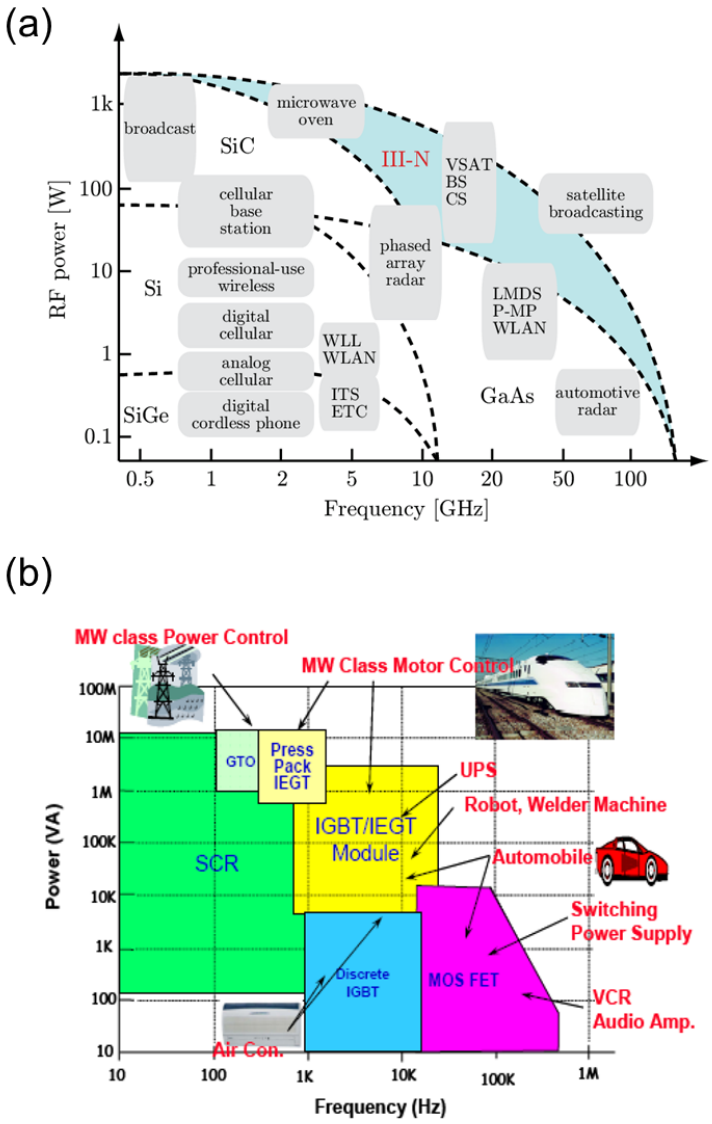


Figure 1.3: Relation of RF power and frequency for (a) several wireless-communication applications [J.-Y. Duboz], and (b) several power-switching applications [H. Wang]. There is a trade-off between power and speed (frequency) for both device applications.

i.e., high voltage, high breakdown field $F_{\rm br}$ is desired, in which

$$F_{\rm br} \propto E_{\rm g}^{\alpha},$$

with energy gap $E_{\rm g}$ and $\alpha \simeq$ 1-3 [5, 9]. This indicates that wide $E_{\rm g}$ is advantageous. However, a trend of proportional relation $m^* \propto E_{\rm g}$, as shown in Fig. 1.4, exists in general cases. This leads to the trade-off between speed and power. Fortunately, wide-gap semiconductor GaN has possibilities to overcome the trade-off.

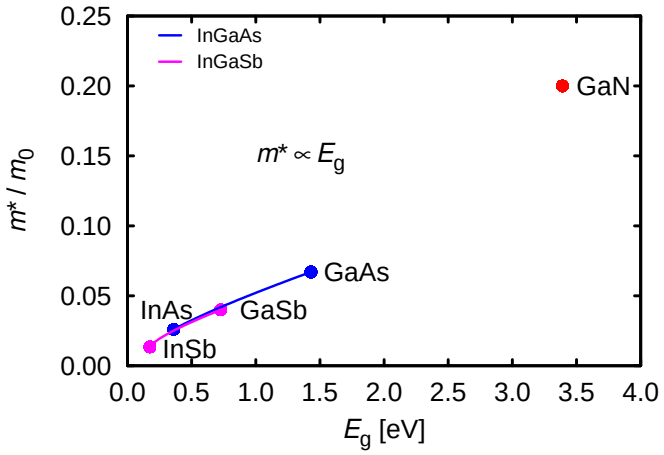


Figure 1.4: Electron effective mass m^* at Γ point as a function of energy gap $E_{\rm g}$ for several III-V compound semiconductors.

1.2 GaN-based materials and devices

1.2.1 Advantageous properties of GaN-based materials

Wide-gap compound semiconductor GaN

Figure 1.5 shows relation between lattice constant in a-axis and energy gap E_g and corresponding emission wavelength for several wurtzite-nitride materials [10], in which GaN exhibits a wide E_g of 3.39 eV [11]. This leads to a high $F_{br} \sim 3.3$ MV/cm, an advantageous for high power, but also a large m^*, shown in Fig. 1.4. This is disadvantageous. However, GaN has a large optical-phonon energy $\hbar\omega_{op} \simeq 90$ meV [12] and a large valley-separation energy, as depicted in Fig. 1.6 [13]. From this, we carried out Monte-Carlo simulation and obtained electron transport in GaN, depicted in Fig. 1.7, in which GaN shows not very high electron mobility, but high peak and saturation velocity, which are advantageous for high speed. Therefore, GaN is anticipated to overcome the trade-off between speed and power in semiconductor devices.

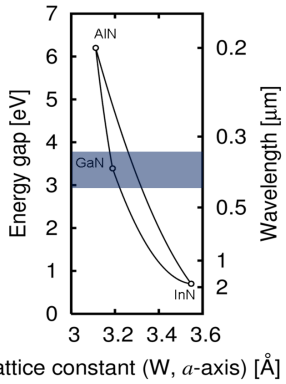


Figure 1.5: Relation between energy gap and lattice constant in a-axis for several wurtzite-nitride materials [I. Vurgaftman *et al.*].

Table 1.2: Advantageous properties of GaN in comparison with other semiconductors.

Mater.	Bandgap [eV]	Electron mobility [cm^2/Vs]	Electron saturation velocity [cm/s]	Breakdown field [V/cm]
Si	1.12	1500	1.0×10^7	3.0×10^5
GaAs	1.42	8500	2.0×10^7	4.0×10^5
InAs	0.36	33000	$\sim 4.0 \times 10^7$	4.0×10^4
SiC	3.33	900	2.0×10^7	3.0×10^6
GaN	**3.39**	**1100**	$\mathbf{2.7 \times 10^7}$	$\mathbf{3.3 \times 10^6}$

Table 1.2 shows advantageous properties of GaN at 300 K in comparison with other

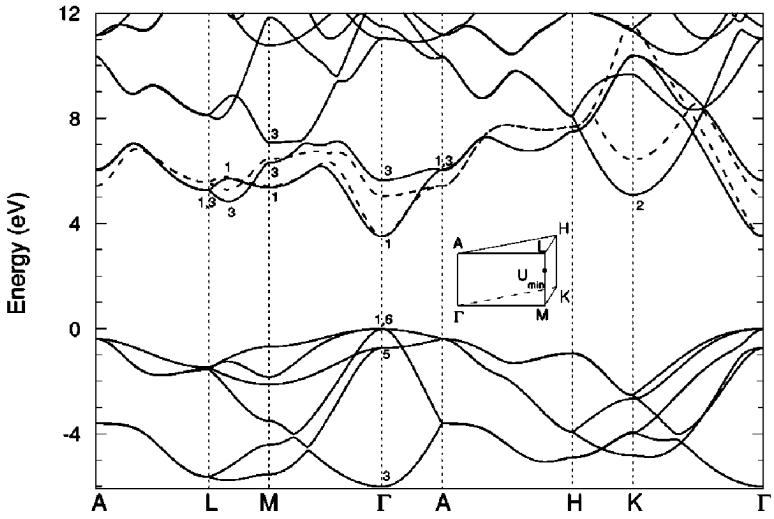


Figure 1.6: Energy band structure for wurtzite GaN [C. Bulutay *et al.*].

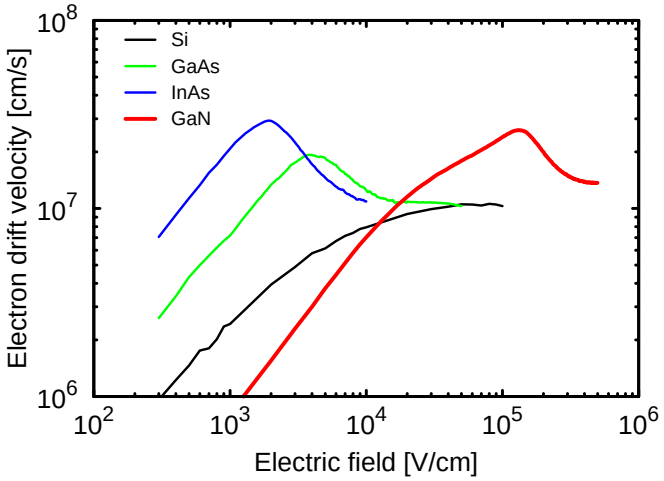


Figure 1.7: Relation between electron drift velocity and electric field obtained by Monte Carlo simulation for several semiconductor materials.

semiconductors [5]. Using the table, we plotted Johnson figure of merit, given by

$$f_{\mathrm{T}} V_{\mathrm{br}} \leqslant \frac{F_{\mathrm{br}} v_{\mathrm{sat}}}{2\pi}, \tag{1.1}$$

where f_{T} is cut-off frequency and V_{br} is breakdown voltage [14], showing products of the maximum cut-off frequencies and the maximum breakdown voltages V_{br}, as depicted in Fig. 1.8. We also plotted Baliga figure of merit, given by

$$R_{\mathrm{on}} \geqslant \frac{4V_{\mathrm{br}}^2}{\varepsilon_0 k \mu F_{\mathrm{br}}^3} \tag{1.2}$$

or

$$\frac{V_{\mathrm{br}}^2}{R_{\mathrm{on}}} \leqslant \frac{\varepsilon_0 k \mu F_{\mathrm{br}}^3}{4}, \tag{1.3}$$

with vacuum dielectric constant ε_0 [15], showing relation between the maximum V_{br} and the minimum on-resistances R_{on}, as depicted in Fig. 1.9. From these figures, we can see that GaN is more superior than other semiconductors.

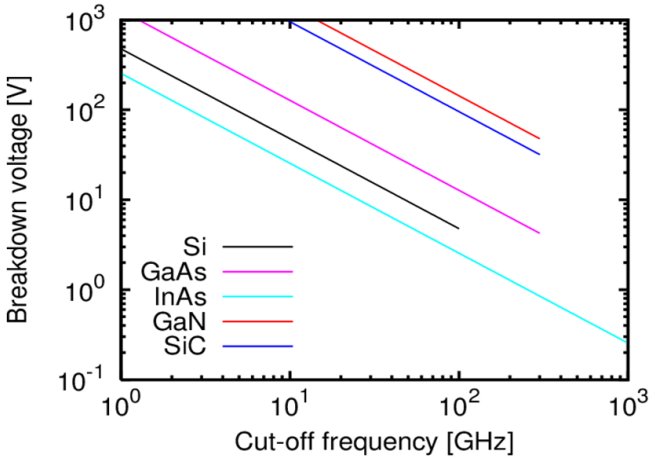


Figure 1.8: Johnson figure of merit showing relation between maximum breakdown voltage V_{br} and maximum cut-off frequency f_{T} for several semiconductors [E. O. Johnson *et al.*].

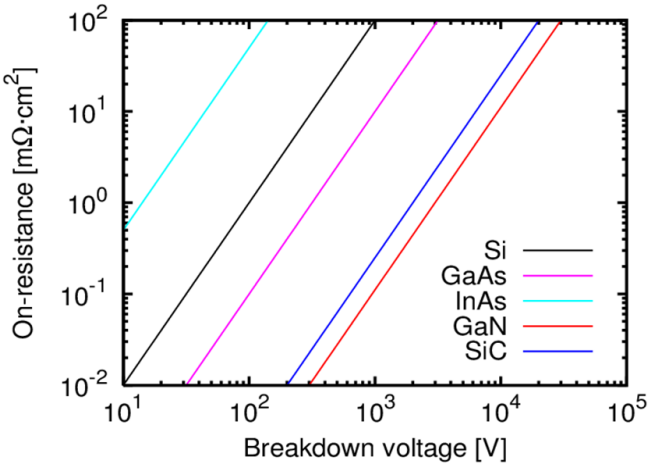


Figure 1.9: Baliga figure of merit showing relation between minimum on-resistance R_{on} and maximum breakdown voltage V_{br} for several semiconductors [B. J. Baliga].

Two-dimensional electron gas in AlGaN/GaN heterostructure

The formation of two dimensional electron gases (2DEG) in AlGaN/GaN heterostructures relies on both spontaneous and piezoelectric polarization induced effects [16, 17]. The spontaneous polarization is due to an intrinsic asymmetry of the bonding in equilibrium wurtzite crystal structures of AlN and GaN. Piezoelectric polarization comes from mechanical stress, or tensile (compressive) strain of AlGaN and GaN layers. The details of these mechanisms are discussed as follows.

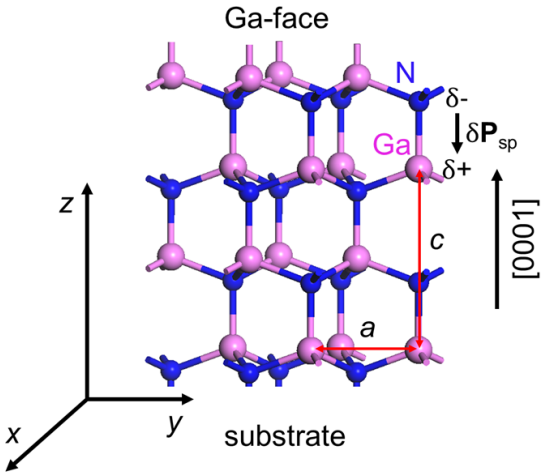


Figure 1.10: Wurtzite crystal structure of GaN with Ga-face. The growth direction is [0001].

Figure 1.10 shows a wurtzite crystal structure of GaN (or AlN), in which a_0 is the edge length of the basal hexagon, c_0 the height of the hexagonal prism at equilibrium. Structure parameters of the GaN and AlN are listed in the table 1.3 [17], in which, the parameter u is defined as the ratio of bonding length b_0 and the height c_0 at equilibrium.

In the absence of external electric field and strain, the polarization inside the material is spontaneous. We consider the polarization along the [0001] direction (z-direction), since this

Table 1.3: Lattice constants $a_0, c_0, c_0/a_0$, bonding length b_0, and parameter $u = b_0/c_0$ at equilibrium of GaN and AlN.

	a_0 [Å]	c_0 [Å]	c_0/a_0	b_0 [Å]	$u = b_0/c_0$
AlN	3.11	4.98	1.60	1.91	0.380
GaN	3.19	5.19	1.63	1.95	0.376

is the direction using for film growth. The spontaneous polarization along the direction is

$$\mathbf{P}_{\text{sp}} = P_{\text{sp}}\hat{\mathbf{z}}. \tag{1.4}$$

Because of the sensitive dependence of the spontaneous polarization on the structure parameters, there are some quantitative differences in the polarization for GaN and AlN. The electronegativity number of Al ~ 1.6 and Ga ~ 1.8 are smaller than that of N ~ 3.0, which create a dipole, i.e., polarization, in Ga-N and Al-N bonds, whose direction is from N to Ga or Al. Table 1.4 shows the spontaneous polarization of GaN and AlN, which are negative. [16]. This indicates that for Ga(Al)-face heterostructures the spontaneous polarization is pointing towards the substrate as shown in Fig. 1.11.

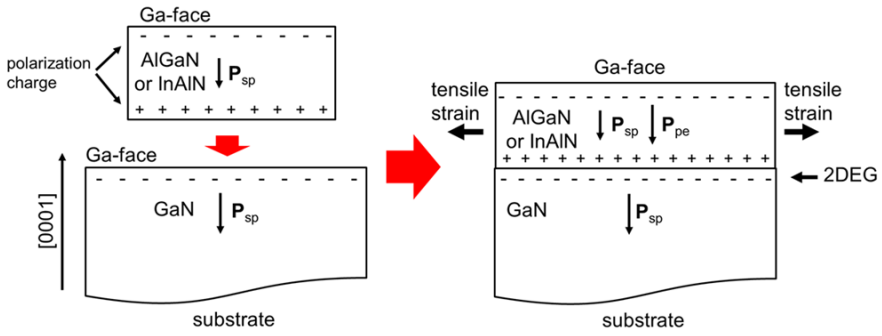


Figure 1.11: Two-dimensional electron gas (2DEG) with high sheet carrier concentration formed by spontaneous and piezoelectric polarizations at the AlGaN/GaN (InAlN/GaN) heterointerface

Piezoelectric or strain-induced polarization P_{pe} is defined from piezoelectric coefficient tensor e_{il} and strain tensor ε_{hk} [16]

$$P_{\text{pe}} = e_{il}\varepsilon_{hk}. \tag{1.5}$$

For wurtzite structure, the piezoelectric coefficient tensor e_{il} has form

$$e_{il} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix}, \tag{1.6}$$

and the strain tensor ε_{hk} has form

$$\varepsilon_{hk} = \begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{pmatrix}, \tag{1.7}$$

in which $\varepsilon_{xx}, \varepsilon_{yy}, \varepsilon_{zz}$ are stress strains and $\varepsilon_{yz}, \varepsilon_{zx}, \varepsilon_{xy}$ are shear strains. In the case of without external force, stress strain is dominant. Therefore, P_{pe} can be calculated as

$$P_{\text{pe}} = e_{31}(\varepsilon_{xx} + \varepsilon_{yy}) + e_{33}\varepsilon_{zz}, \tag{1.8}$$

where $\varepsilon_{zz} = (c - c_0)/c_0$ is the strain along the z-axis and $\varepsilon_{xx} = \varepsilon_{yy} = (a - a_0)/a_0$ are the in-plane strain, in which a_0 and c_0 are the equilibrium values of the lattice parameters. In the case of no force acting on z-axis, we have the relation

$$C_{33}e_{zz} = -2C_{13}e_{xx}, \tag{1.9}$$

where C_{33} and C_{13} are elastic constants. Using Eq. (1.8) and (1.9), the amount of the piezoelectric polarization in the direction of the z-axis can be determined by

$$P_{\text{pe}} = -2\varepsilon_{xx}(e_{31} - e_{33}\frac{C_{13}}{C_{33}})$$

or

$$P_{\text{pe}} = -2\frac{(a - a_0)}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}). \tag{1.10}$$

Table 1.4: Calculated the spontaneous polarization and piezoelectric constants of AlN and GaN wurtzites.

	P_{sp} [C/m^2]	e_{33} [C/m^2]	e_{31} [C/m^2]
AlN	-0.081	1.46	-0.60
GaN	-0.29	0.73	-0.49

Table 1.4 shows calculated values of e_{33} and e_{31} [16]. From eq. (1.10), we can say that $\mathbf{P}_{\text{pe}}$ is negative for tensile and positive for compressive strain. For AlGaN growth on GaN, the strain is tensile, depicted in Fig. 1.11, indicating that $\mathbf{P}_{\text{pe}}$ is in the same direction with $\mathbf{P}_{\text{sp}}$.

The gradient of polarization of in space generates induced charges. At an abrupt interface of AlGaN/GaN heterostructure the polarization can decrease or increase, causing a polarization sheet charge density. For AlGaN growth on GaN with Ga-face, the total polarization $\mathbf{P}$, the sum of the spontaneous polarization $\mathbf{P}_{\text{sp}}$ and the piezoelectric polarization $\mathbf{P}_{\text{pe}}$, is negative, which induces electrons accumulating near the AlGaN/GaN interface. Owing to the strong $\mathbf{P}$, the density of the accumulating electrons is large, which form a two-dimensional electron gas (2DEG) near the interface of the AlGaN/GaN heterostructures. Figure 1.12

shows calculated sheet charge density caused by spontaneous and piezoelectric polarization at the lower interface of a Ga-face GaN/AlGaN/GaN heterostructure v.s. alloy composition of the barrier, obtained by O. Ambacher *et al.* [18], indicating the high electron density of the 2DEG. As a result, the 2DEG can be utilized as the channel for GaN-based heterojunction field-effect transistors (HFETs). [19].

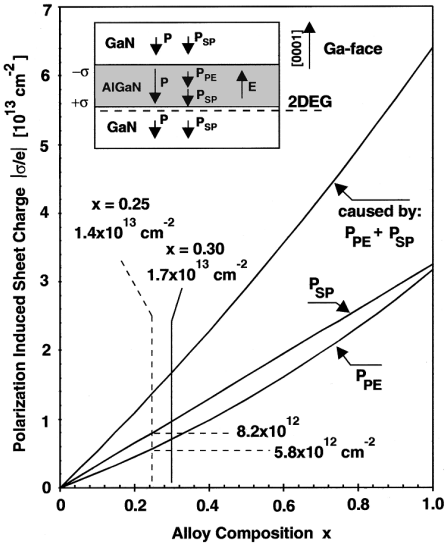


Figure 1.12: Calculated sheet charge density caused by spontaneous and piezoelectric polarization at the lower interface of a Ga-face GaN/AlGaN/GaN heterostructure v.s. alloy composition of the barrier [O. Ambacher *et al.*].

1.2.2 GaN-based Schottky-HFETs and MIS-HFETs

Using the 2DEG as a channel, GaN-based Schottky-HFETs have been intensively investigated for high-speed, high-power, and high-temperature device applications [19–24]. High drain current, high transconductance, especially high cut-off frequency f_T and maximum frequency f_{max} were obtained. For example, G. J. Sullivan *et al.* fabricated a AlGaN/GaN Schottky-HFET with a gate length of 0.7 μm on SiC substrate which showed a high current of $\sim$ 1100 mA/mm, a transconductance of $\sim$ 270 mS/mm, $f_T \sim$ 15 GHz and $f_{max} \sim$ 42 GHz [23]. However, AlGaN/GaN Schottky-HFETs exhibit high gate leakage current in spite of large energy gap [21, 25–27] and serious current collapse due to due to surface electron trapping [28–30], as depicted in Fig. 1.13(a). As a result, the reliability and life time of the devices are reduced.

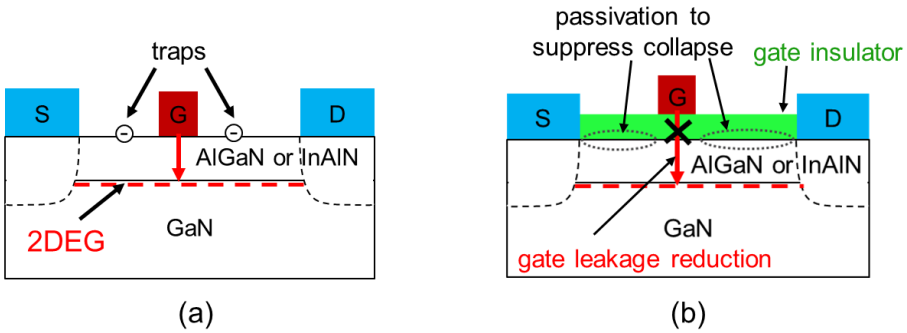


Figure 1.13: Schematic cross section of GaN-based (a) Schottky-HFETs and (b) Metal-insulator-semiconductor (MIS)-HFETs.

In order to solve the problems, GaN-based metal-insulator-semiconductor (MIS)-HFETs, where a gate insulator is inserted between the metal and semiconductor, as depicted in Fig. 1.13(b), have been investigated owing to the merits of gate leakage reduction [27, 31–37] and passivation to suppress the current collapse [28–30], as shown in Fig. 1.13(b). Gate insulators, such as Al_2O_3 ($E_g \sim$ 6.8 eV, $k \sim$ 9 [38]) [34, 35, 39–42], HfO_2 ($E_g \sim$ 5.8 eV, $k \sim$ 25 [43]) [32, 33, 44], TaON ($E_g \sim$ 4.3 eV, $k \sim$ 24) [37], and TiO_2 ($E_g \sim$ 3.1 eV [45], $k \sim$ 60 [43]) [46–48]. and high-k nitrides, such as SiN ($E_g \sim$ 5.0 eV, $k \sim$ 7.5 [49]) [46, 47, 50, 51] and AlN ($E_g \sim$ 6.2 eV [52], $k \sim$ 9 [53]) [28–30, 36, 51, 54–56] have been intensively investigated. However, further developments of the MIS-HFETs using novel gate insulators suitable according to applications are important. A desired gate insulator should have:

- wide energy gap and high breakdown field F_{br} for high voltage operation
- high dielectric constant k for high transconductance
- high thermal conductivity κ for good heat release suitable to high power operation

In particular, boron nitride (BN) and aluminum titanium oxide (AlTiO: an alloy of TiO_2 and Al_2O_3) are promising candidates.

1.3 BN and AlTiO as a high-dielectric-constant (high-k) insulator

1.3.1 Boron nitride (BN)

Boron nitride (BN) has been the subject of numerous theoretical and experimental studies. It can occur in multiple polytypes, including white-graphite BN (h-BN), wurtzite BN (w-BN), and zincblende BN (c-BN) [57–63]. Similar to graphite, the h-BN has a white-graphite structure with sp^2-hybridized B-N bonds [59, 64, 65] shown in Fig. 1.14(a). In contrast to graphite with C-C bondings showing strong covalent character, which exhibits semimetallic behavior, h-BN with B-N bonds showing ionic character, is insulating with an indirect energy gap E_g. It is in a range from 3.6 to 6.0 eV for theoretical calculations [57, 58, 60–63] and $\sim$ 5 eV for experimental measurements [64, 66–70]. The wide E_g and the ability to synthesize single layers of the h phase make it attractive for two-dimensional electronics and as a substrate for growth or bonding of graphene [71]. In addition, the h-BN possesses a high thermal conductivity $\kappa \sim 600$ $WK^{-1}m^{-1}$ and high heat capacity [72].

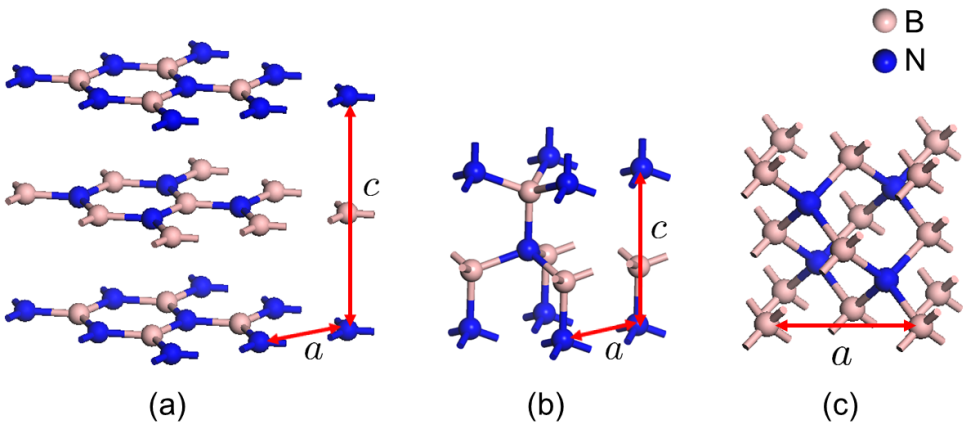


Figure 1.14: Crystal structures of BN polymorphs: (a) zincblende, (b) wurtzite, and (c) white-graphite, obtained by Materials Studio.

On the other hand, the w-BN has a wurtzite structure with sp^3-hybridized B-N bonds, as shown in Fig. 1.14(b), [59, 64]. Theoretical calculations show its indirect E_g in a rang from 4.4 to 6.5 eV [57, 60–63]. The w-BN is metastable at all temperatures, and a large volume expansion occurs on conversion of the wurtzitic form to the other forms [73]. Therefore, E_g of w-BN is difficult to be determined by experimental methods.

In contrast, the c-BN, which is stable and ultra-hard, has a zincblende structure with sp^3-hybridized B-N bonds [59, 64, 65, 74], as shown in Fig. 1.14(c). The c-BN has an indirect E_g, which is in a range from 4.2 to 7.2 eV for theoretical calculations [57, 58, 60–63] and $\sim$ 6.4 eV for experimental measurements [75]. The wide E_g of the c-BN leads to its high breakdown field $\sim$ 10 MV/cm [52]. In addition, the c-BN has a high melting point $\sim$ 3000 °C [76], high dielectric constant $k \sim 7$ [77], and very high $\kappa \sim 1300$ $WK^{-1}m^{-1}$ [78, 79]. This is $\sim$ 4 and $\sim$ 40 times higher than that of AlN and Al_2O_3, respectively. Table 1.5 lists physical

properties of BN polymorphs in comparison with other insulators. Figure 1.15 draws band lineup of BN polymorphs and several insulators in an alignment with AlGaN and GaN. We observe a wide conduction-band difference between BN polymorphs and AlGaN.

Table 1.5: Advantageous properties of BN polymorphs in comparison with other materials.

Mater.	Energy gap E_g [eV]	Dielectric constant k	Breakdown field F_{br} [MV/cm]	Thermal conductivity κ [$WK^{-1}m^{-1}$]
GaN	3.4	8.9	3.3	130
AlN	6.2	9.1	~ 10	300
h-BN	~ 5.2	7.0	~ 10	600
w-BN	~ 6	-	-	-
c-BN	~ 6.4	~ 7.0	~ 10	1300
Al_2O_3	6.8	~ 9	9.0	~ 30
TiO_2	3.1	~ 60	-	~ 10

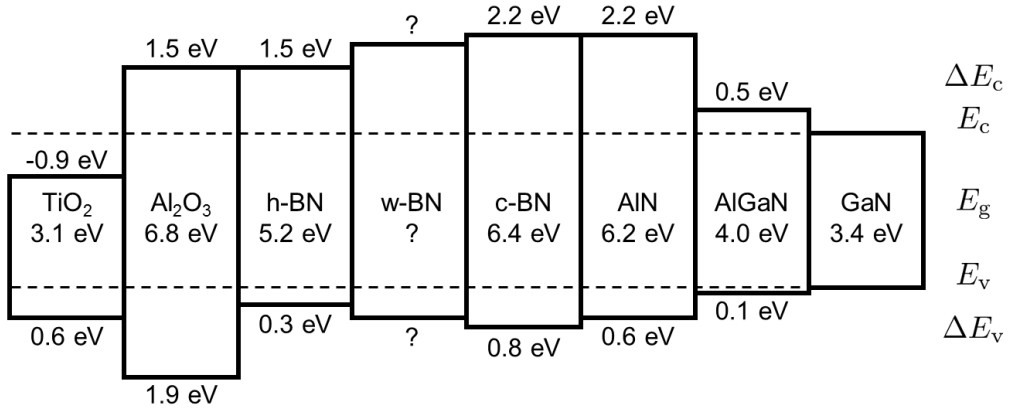


Figure 1.15: Band lineup for BN polymorphs and several insulators, in comparison with AlGaN/GaN.

Owing to the advantageous properties of BN polymorphs, they can be favorable gate insulators [80, 81]. There was a report on BN gate insulator for GaN-based devices by J.-C. Gerbedoen *et al*. [82], in which h-BN films were obtained by chemical vapor deposition. However, device performance was poor, such as a low maximum drain current $\sim$ 590 mA/mm, and a low extrinsic transconductance $\sim$ 60 mS/mm. In addition, electron transport properties for channel conduction and gate leakage were not clarified. Therefore, it is worth to study BN and its applications to BN/AlGaN/GaN MIS-HFETs in details. In this thesis, we will characterize physical properties of BN thin films obtained by RF magnetron sputtering. Using such films, we will fabricate BN/AlGaN/GaN MIS-HFETs, and investigate their temperature-dependent characteristics. We will analyze electron transport properties for channel conduction and gate leakage, and from the latter we will estimate BN/AlGaN interface state density.

1.3.2 Aluminum titanium oxide (AlTiO)

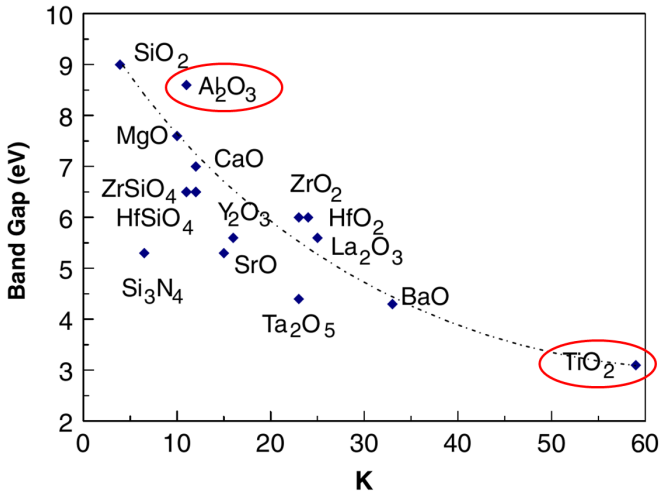


Figure 1.16: Relation between dielectric constant k and energy gap E_g for several oxides [J. Robertson].

Figure 1.16 depicts relation between dielectric constant k and energy gap E_g for several oxides [43]. There is a trade-off between high k and high E_g. Owing to an extremely high k of TiO_2 (~ 60), TiO_2/AlGaN/GaN MIS-HFETs were investigated [46, 48]. Unfortunately, the small energy gap E_g of TiO_2 (~ 3.1 eV) [45] is a drawback, leading to high gate leakage currents [46, 48] and low breakdown fields [83]. On the other hand, Al_2O_3 has a wide $E_g \sim 6.8$ eV, which exhibits very good insulating properties [34, 40, 42]. However, it shows a lower $k \sim 9$ [38]. In order to realize not only high k but also wide E_g, a combination of TiO_2 and Al_2O_3 may be possible. AlTiO, an alloy of TiO_2 and Al_2O_3, which has intermediate properties between TiO_2 and Al_2O_3, as shown in Fig. 1.17, is important to balance k and E_g.

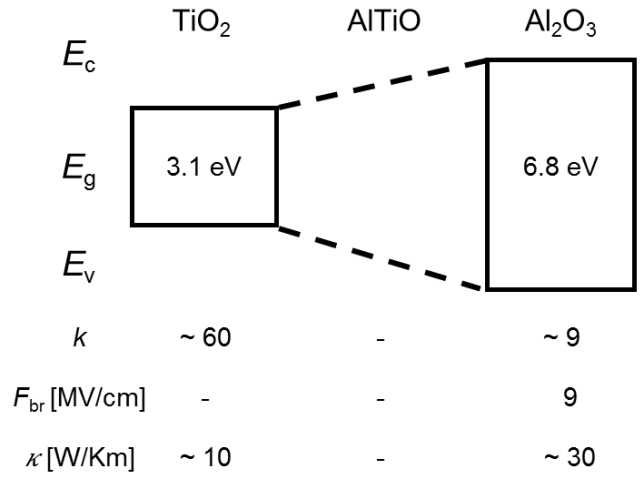


Figure 1.17: AlTiO, an alloy of TiO_2 and Al_2O_3, has intermediate properties between TiO_2 and Al_2O_3.

There were some reports on AlTiO gate insulator for Si-based devices [84–86] and GaAs-based devices [87–89]. However, there was no report on AlTiO gate insulator for GaN-based devices. In order to obtain AlTiO films, several deposition methods, such as sputtering deposition [84], pulsed laser deposition [85], and atomic layer deposition (ALD) [86–89], were utilized. In particular, the ALD is advantageous to produce high-quality films with high reproducibility and fine composition control. In this thesis, we will characterize physical properties of AlTiO thin films obtained by atomic layer deposition, for several Al compositions. Using such films, we will fabricate AlTiO/AlGaN/GaN MIS-HFETs, and investigate their temperature-dependent characteristics. In addition, we will analyze electron transport properties for channel conduction and gate leakage, and from the latter we will estimate AlTiO/AlGaN interface state density.

1.4 Purposes of this study

In order to develop the AlGaN/GaN MIS-HFETs using novel gate insulators suitable for high-speed and high-power applications, we study BN and AlTiO high-k gate insulators.

At first, in order to check BN films obtained by RF magnetron sputtering deposition, BN/n-Si(001) will be characterized by ellipsometry and MIS-capacitor I-V measurements. We will optimize BN deposition conditions, for example N_2 ratio, to obtain highest BN quality. Then, BN will be deposited on an AlGaN/GaN heterostructure, which will be characterized by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS). Using the BN films, we will fabricate BN/AlGaN/GaN MIS-HFETs and investigate their gate leakage and ambient-dependent characteristics. We will also investigate their temperature-dependent characteristics; analyze electron transport properties for channel conduction and gate leakage, and estimate BN/AlGaN interface state density.

Similarly, in order to check AlTiO films obtained by ALD, AlTiO/n-GaAs(001) will be characterized by ellipsometry, XPS, and MIS-capacitor I-V measurements. We will characterize physical properties of AlTiO thin films, for several Al compositions. Using a trade-off composition, AlTiO will be deposited on the same AlGaN/GaN heterostructure, which will be characterized by XRD. Using the AlTiO films, we will fabricate AlTiO/AlGaN/GaN MIS-HFETs and investigate their gate leakage and compare with Al_2O_3/AlGaN/GaN MIS-HFETs. For the AlTiO/AlGaN/GaN MIS-HFETs, we will also investigate their temperature-dependent device characteristics; analyze electron transport properties for channel conduction and gate leakage, and estimate AlTiO/AlGaN interface state density. Finally, we will briefly compare BN and AlTiO as high-k gate insulators.

1.5 Organization of the dissertation

We organize this dissertation into 5 chapters. In chapter 1, at the beginning, we introduce trends of recent semiconductor industry: More Moore and More than Moore. The trade-off between speed and power in semiconductor devices, advantages of GaN to overcome the trade-off are mentioned. We explain the formation of two dimension electron gas at AlGaN/GaN interface. Then, we briefly review researches on GaN-based devices with several oxide and nitride high-k insulators. In details, we evaluate researches on BN and AlTiO, their advantageous properties and applications to AlGaN/GaN HFETs and MIS-HFETs.

Next, in chapter 2, we briefly describe general fabrication process methods for AlGaN/GaN MIS-HFETs. We explain some key points during the process flows, and summary in details conditions for each step.

Then, in chapter 3, we describe a RF magnetron sputtering deposition method to obtain BN films. Fabrication process and I-V characteristics of BN/n-Si(001) MIS capacitors are shown in this chapter. We show XRD and XPS measurement results of BN films on AlGaN/GaN/sapphire(0001). Using the films, we fabricate BN/AlGaN/GaN MIS-HFETs and investigate their characteristics in different ambiences and their temperature dependence of output and transfer characteristics. This chapter shows analysis results of electron transport properties for channel conduction and gate leakage, and estimation of BN/AlGaN interface state density.

After that, in chapter 4 we describe ALD method to obtain AlTiO films. We show relation between Al composition and AlTiO film properties, such as refractive index, energy gap, breakdown field and dielectric constant. We apply a trade-off composition for AlTiO deposition to fabricate AlTiO/AlGaN/GaN MIS-HFETs and show their gate leakage and comparison with Al_2O_3/AlGaN/GaN MIS-HFETs. This chapter also shows temperature dependence of output and transfer characteristics for AlTiO/AlGaN/GaN MIS-HFETs, analysis results of electron transport properties for channel conduction and gate leakage, and estimation of AlTiO/AlGaN interface state density.

Finally, we conclude this work, briefly compare BN and AlTiO Future works are also mentioned.

Chapter 2

Fabrication process methods for AlGaN/GaN MIS-HFETs

Mask pattern using for device fabrication in this research is shown in Fig. 2.1. For evaluating electrical characteristics during the fabrication process, FET, Hall-bar, transmission line model (TLM), and capacitor are fabricated simultaneously. The fabrication process methods for AlGaN/GaN MIS-HFETs includes five steps as follows.

1. Marker formation
2. Ohmic electrode formation
3. Device isolation
4. Gate insulator deposition
5. Gate electrode formation

We describes in details of all steps as follows.

2.1 Marker formation

Marker formation is an important step because markers were utilized to align for all following steps: Ohmic electrode formation, device isolation, and gate electrode formation. For this device fabrication process, we employed an AlGaN/GaN heterostructure, obtained by Metal-Organic Vapor Phase Epitaxy (MOVPE) grown on sapphire(0001) substrate. Marker formation was started by a surface treatment for the heterostructure using organic solvents and O_2 plasma ashing for removing organic contaminants, followed by ammonium-based solutions (Semico-clean) for removing oxides. A clean surface can enhance adhesion between metals and the AlGaN surface. Then, a metal structure of Titanium/Gold (Ti/Au) = 10/150 nm was deposited on the heterostructure by an e-beam evaporator. Conditions of steps and processing for marker formation are listed in Tab. 2.1.

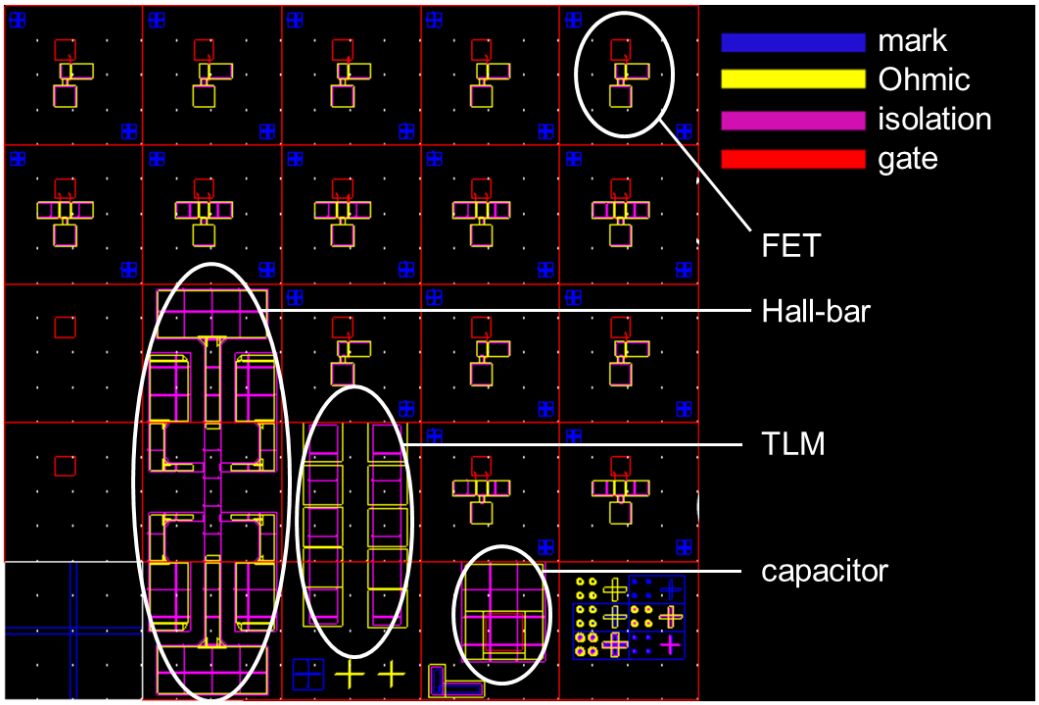


Figure 2.1: Mask pattern with test element groups: FETs, Hall-bars, transmission line models (TLM), and capacitors. Grid size is 125 μm.

Table 2.1: Marker formation process flow.

Process	Conditions
surface treatment	- acetone, methanol, DIW 3 min each - O_2 plasma ashing 50 Pa 10 W 4 min - Semico-clean 5 min, DIW 3 min - bake 110 °C 3 min
resist coating	- LOL2000 3000 rpm 60 s, bake 180 °C 180 s - TSMR-8900 4000 rpm 60 s, bake 110 °C 90 s
patterning	- exposure $\sim$ 12 mW/cm^2 (405 nm) 6.2 s - development NMD-W 60 s, DIW 180 s
surface treatment	- O_2 plasma ashing 50 Pa 10 W 10 s - Semico-clean 5 min, DIW 3 min
deposition	- Ti/Au = 10/150 nm
lift-off	- 1165 60 °C $\sim$ 30 min - acetone, methanol, DIW 3 min each

2.2 Ohmic electrode formation

Conditions of steps and processing for Ohmic electrode formation are listed in Tab. 2.2 and shown in Fig. 2.2.

Table 2.2: Ohmic electrode formation process flow.

Process	Conditions
surface treatment	- acetone, methanol, DIW 3 min each - O_2 plasma ashing 50 Pa 10 W 4 min - Semico-clean 5 min, DIW 3 min - bake 110 °C 3 min
resist coating	- LOL2000 3000 rpm 60 s, bake 180 °C 180 s - TSMR-8900 4000 rpm 60 s, bake 110 °C 90 s
patterning	- exposure $\sim$ 12 mW/cm^2 (405 nm) 6.2 s - development NMD-W 60 s, DIW 180 s
surface treatment	- O_2 plasma ashing 50 Pa 10 W 10 s - Semico-clean 5 min, DIW 3 min
deposition	- Ti/Al/Ti/Au = 10/200/100/50 nm
lift-off	- 1165 60 °C $\sim$ 30 min - acetone, methanol, DIW 3 min each
annealing	- N_2 ambience

Low contact resistance and high stability are important requirements for FET electrodes. In our device fabrication process, an electrode structure of Titanium/Aluminium/Titanium/Gold (Ti/Al/Ti/Au) = 10/200/100/50 nm was deposited on the AlGaN/GaN heterostructure by the e-beam evaporator. Ti with a low work function $\sim$ 4.3 eV [90], exhibits very low barrier height to n-GaN [91]. However, the main reason of using Ti is its ability to extract N out of the AlGaN(GaN) by formation of TiN due to reaction between Ti and N,

$$2\mathrm{Ti} + \mathrm{N_2} = 2\mathrm{TiN},$$

during annealing process. This leaves a high density of N vacancies below the electrodes, acting as donor dope and giving electrons [92]. High electron densities can create tunnel junctions, or Ohmic contacts [93]. Al in the metalization scheme forms an alloy with the Ti layer below, by which the aggressive Ti-GaN reaction is decreased and maintain the TiN layer [94]. Au is deposited as the final metal layer to exclude oxidation of the contact. Ti layer beneath Au has a role to limit the diffusion of Au into the layers below and vice versa.

From transmission line model (TLM) measurements, contact resistance R_c of the Ohmic contacts and sheet resistance ρ_s were obtained by a linear fitting for measurement resistance R to electrode spacing L using

$$R(L) = 2R_c + \rho_s L. \tag{2.1}$$

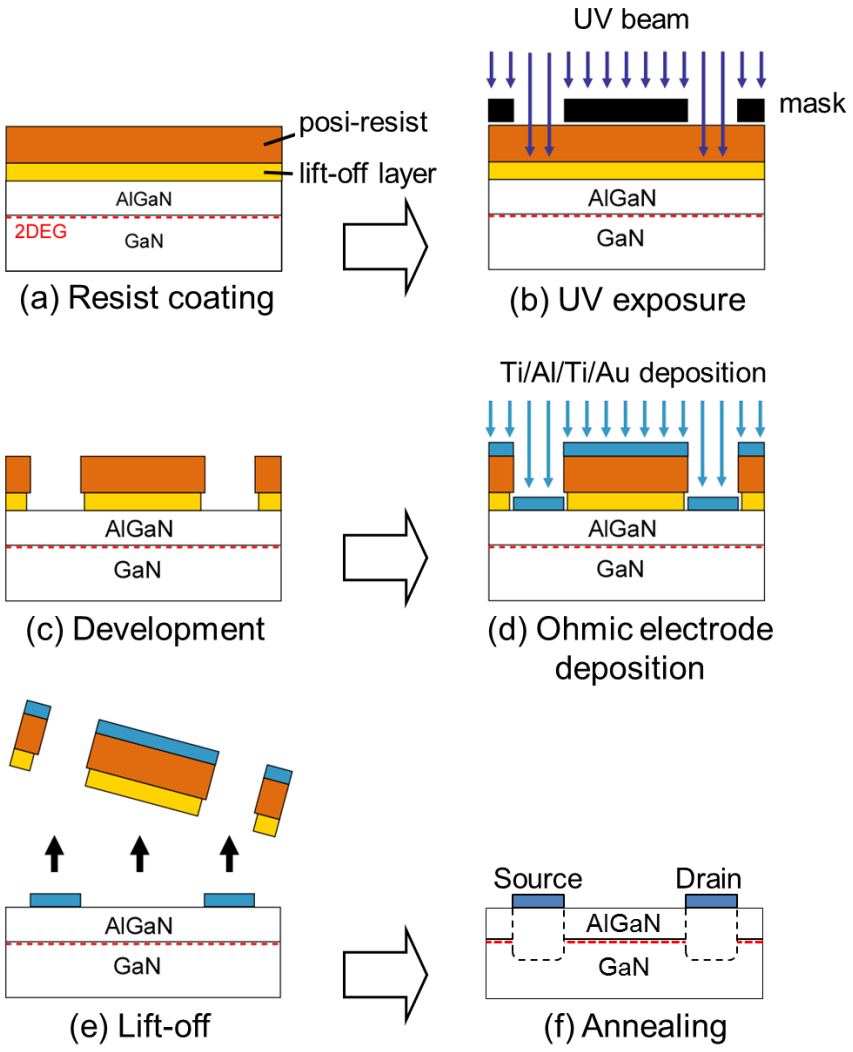


Figure 2.2: Ohmic electrode formation process flow.

Details of TLM method is described in appendix B. Figure 2.3 depicts an example of TLM measurement results after electrode annealing in N_2 ambience at 625 °C for 5 min. It should be recognized that R_c depends on annealing temperature. In order to obtain the lowest R_c, we investigated the annealing-temperature dependence of R_c, shown in Fig. 2.4. The temperature at which R_c is lowest was employed for the annealing. It is noted that the annealing carried out in N_2 ambience can prevent the loss of N atom in AlGaN/GaN channel.

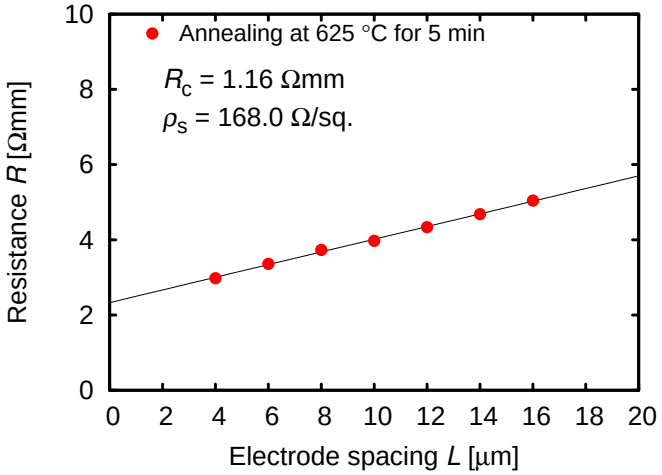


Figure 2.3: Contact resistance R_c and sheet resistance ρ_s of Ohmic electrodes obtained after an annealing in N_2 ambience at 625 °C for 5 min.

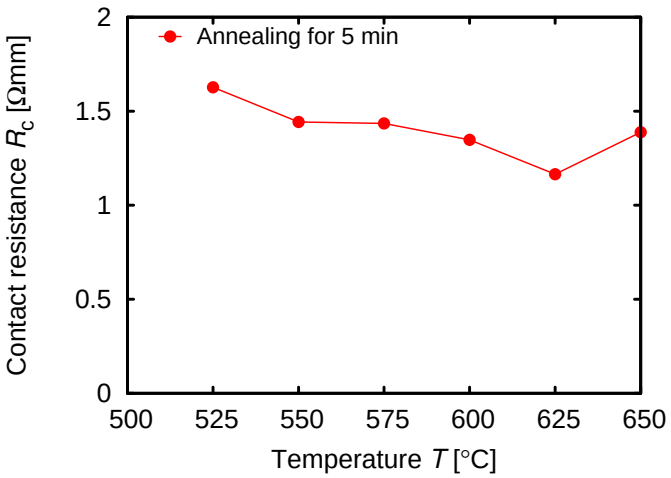


Figure 2.4: Contact resistance R_c as a function of annealing temperature T for 5 min in N_2 ambience.

2.3 Device isolation

Implant isolation has been widely used in compound semiconductor devices for inter-device isolation by compensation of the semiconductor layer due to a damage or chemical mechanism [95]. The implantation of the elements, such as H, He, N, and P have been investigated in GaN for the purpose of creating damages, which have energy levels in or near mid-gap, during implantation [96]. The mid-gap states can trap electrons, or compensate the initial conductivity, and increase resistivity by reduce free carriers in the implanted areas, as shown in Fig. 2.5 [97].

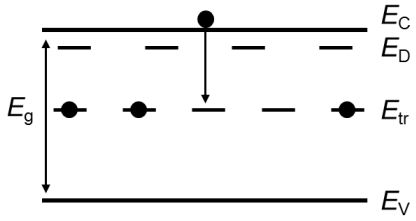


Figure 2.5: Deep level traps at energy E_{tr} induced by ion implantation.

In our process, a light implanted ion B^+ is employed. The depth profile of B^+ concentration in the AlGaN/GaN heterostructure at several implant acceleration voltages obtained by SRIM/TRIM simulation is shown in Fig. 2.6 [98]. From the simulation results, the depth of the implanted ion at acceleration voltages of 30, 50, and 100 kV is from surface to $\sim$ 300 nm with high ion concentration, which is deep enough for isolation for planar devices.

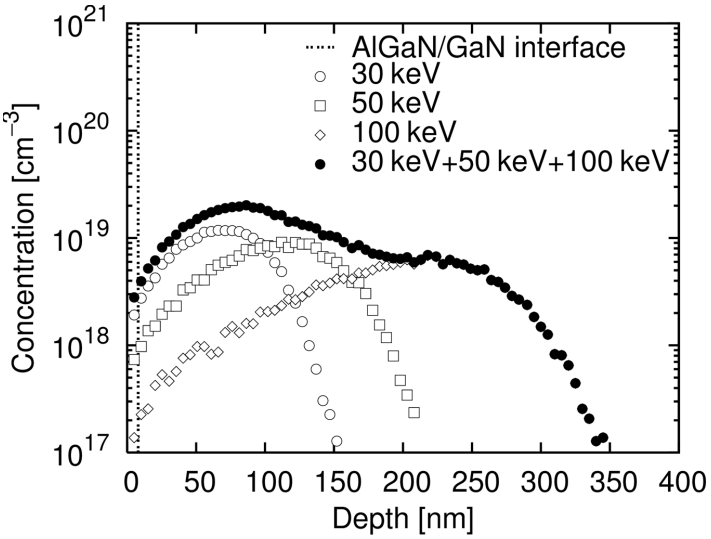


Figure 2.6: Depth profile of B^+ ion concentration in the AlGaN/GaN heterostructure at several implant acceleration voltages obtained by Monte-Carlo simulation.

Conditions of steps and processing for device isolation are listed in Tab. 2.3 and shown in Fig. 2.7.

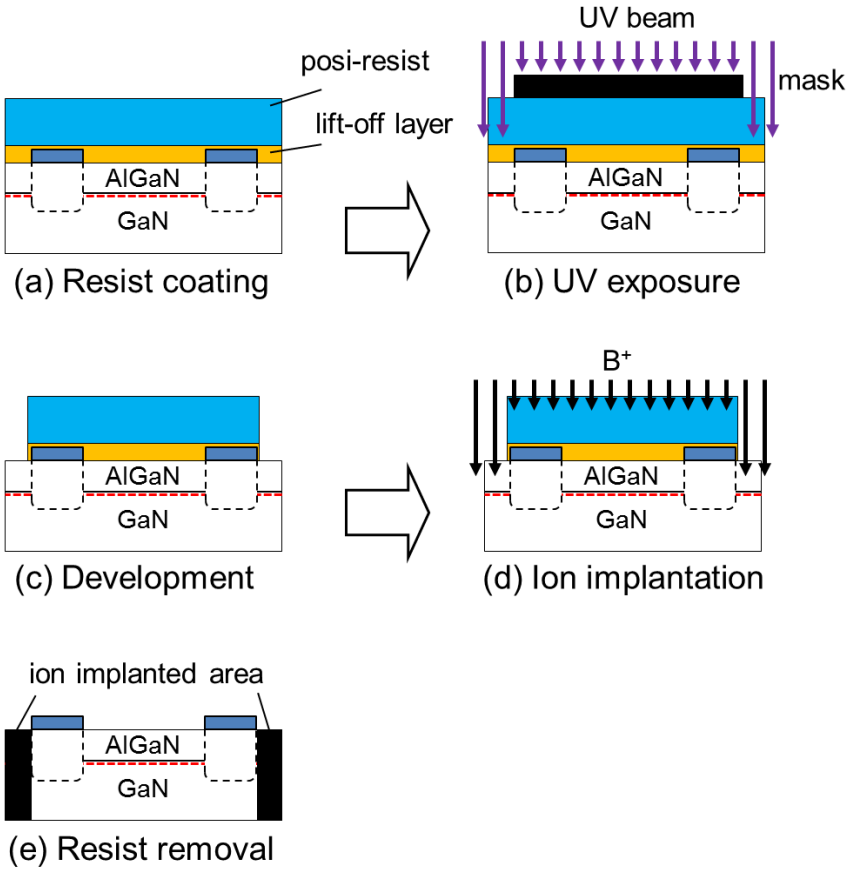


Figure 2.7: Device isolation process flow.

Table 2.3: Device isolation process flow.

Process	Conditions
surface treatment	- acetone, methanol, DIW 3 min each - O_2 plasma ashing 50 Pa 10 W 4 min
resist coating	- LOL2000 3000 rpm 60 s, bake 180 °C 180 s - S1830 4000 rpm 60 s, bake 110 °C 90 s
patterning	- exposure $\sim$ 12 mW/cm^2 (405 nm) 30 s - development NMD-W 50 s, DIW 180 s - bake 140 °C 5 min
ion implantation	- B^+ 30 keV (1×10^{14} cm^{-2}) + 50 keV (1×10^{14} cm^{-2}) + 100 keV (1×10^{14} cm^{-2})
resist removal	- 1165 60 °C $\sim$ 30 min - acetone, methanol, DIW 3 min each - O_2 plasma ashing 50 Pa 30 W 10 min

2.4 Gate insulator deposition

There are many methods to deposit an insulator. In this work, we employs two deposition methods, which are RF magnetron sputtering for deposition of BN and atomic layer deposition (ALD), for deposition of AlTiO. Table 2.4 lists advantageous and disadvantageous of the sputtering in comparison with ALD. Due to limitation of precursors including nitride compounds, nitride materials, such as BN, are difficult to be deposited by ALD. On the other hand, oxide materials, such as TiO_2 and Al_2O_3, i.e., AlTiO, can be deposited by ALD.

Table 2.4: Comparison between sputtering and atomic layer deposition (ALD) methods.

	Sputtering	ALD
advantageous	- High rate - Freedom to choose sources (many sources available) - High pure films	- No damage - Good coverage - High uniformity
disadvantageous	- High damage - Not good coverage	- Low rate - Source (precursor) limitation

For the MIS-HFET fabrication process, after a surface treatment process using organic solvents and oxygen plasma ashing for removing organic contaminants, and followed by Semicoclean for removing oxides, BN or AlTiO was deposited on the AlGaN surface. Figure 2.8 shows the device with the deposited gate insulator.

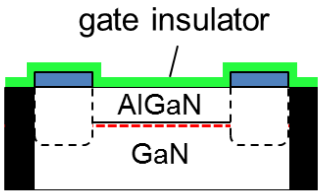


Figure 2.8: Gate insulator deposition on the AlGaN surface.

2.5 Gate electrode formation

Table 2.5: Gate electrode formation process flow.

Process	Conditions
resist coating	- ZEP520-A7 4000 rpm 60 s, bake 120 °C 180 s - Espacer 1500 rpm 60 s, bake 100 °C 180 s
patterning	- exposure (gate) 50 keV 50 pA pitch 1 2.7 μs (dose 135 μC/cm^2) - exposure (pad) 50 keV 50 pA pitch 3 9.0 μs (dose 150 μC/cm^2) - Espacer removal: DIW 60 s - development ZED-N50 60 s, ZMD-B 30 s, N_2 blow
surface treatment	- O_2 plasma ashing 50 Pa 10 W 10 s
deposition	- Ni/Au = 5/35 nm
lift-off	- 1165 60 °C $\sim$ 30 min - acetone, methanol, DIW 3 min each

The device fabrication process was completed by formation of Ni/Au = 5/35 nm gate electrodes on the gate insulator. In order to form fine gate electrodes, electron beam (e-beam) lithography was employed. ZEP520-A7, a high sensitivity e-beam resist, was coated on the sample surface. Then, an espacer layer was coated on ZEP520-A7 to avoid charging up during exposure. Ni was used as gate metal due to its high work function ($\sim$ 5.2 eV [90]), from which high potential barrier is formed at Ni/insulator contact for reduction of gate leakage current. Conditions of steps and processing for device isolation are listed in Tab. 2.5 and shown in Fig. 2.9. The fabricated MIS-HFETs, as shown in Fig. 2.10(a) and (b), have a gate length $\sim$ 270 nm, a gate width $\sim$ 50 μm, a gate-source spacing $\sim$ 2 μm, and a gate-drain spacing $\sim$ 3 μm.

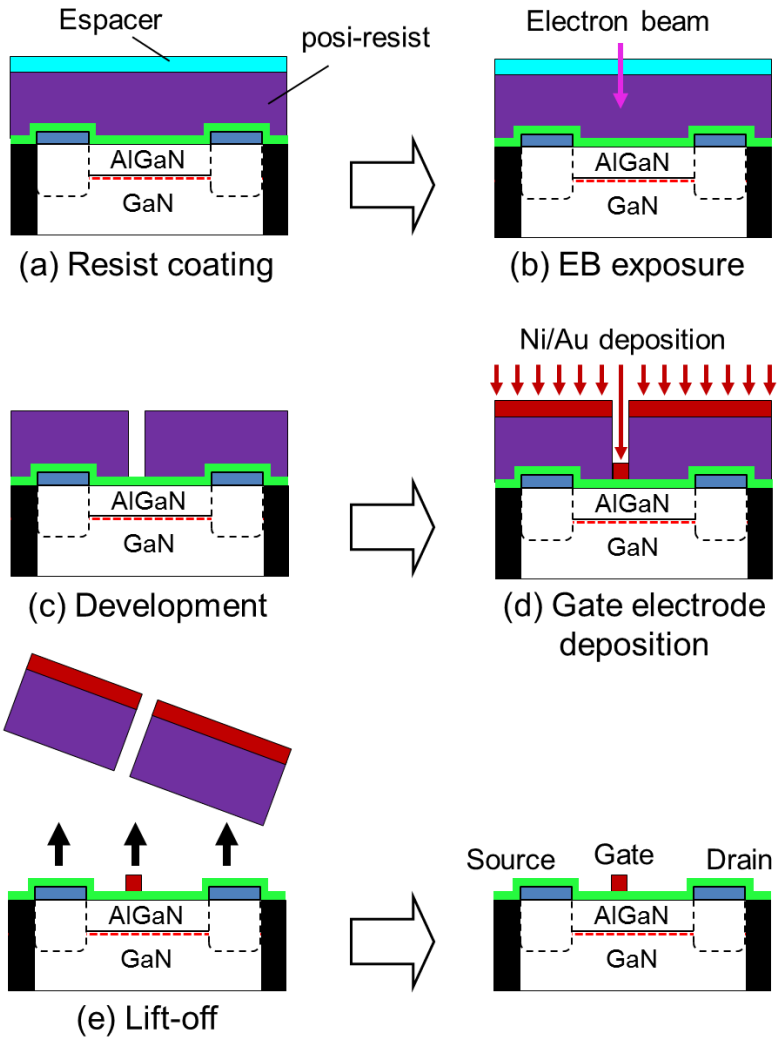
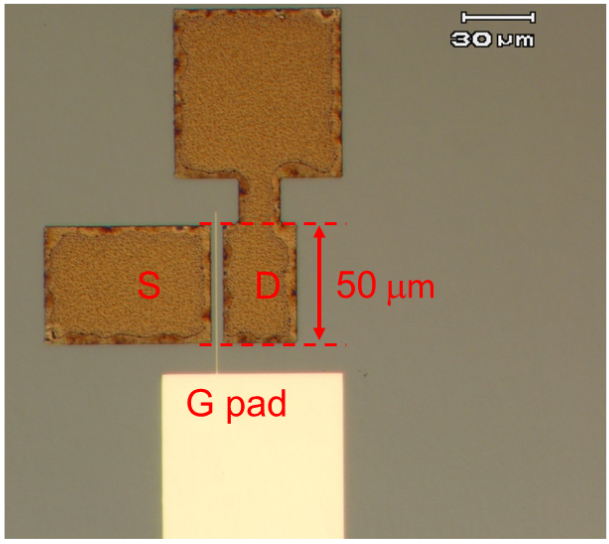
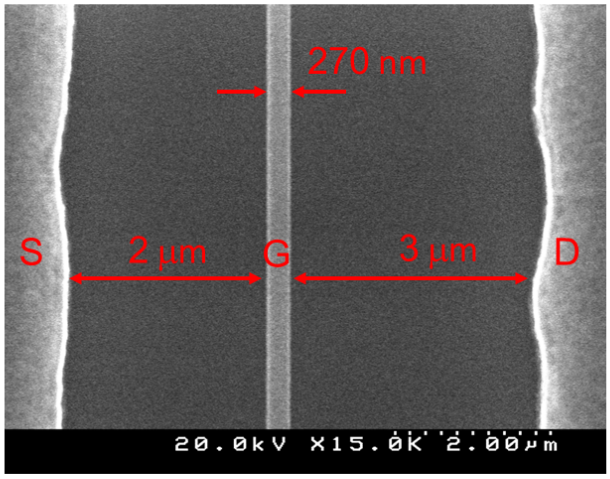


Figure 2.9: Gate electrode formation process flow.



(a)



(b)

Figure 2.10: (a) Optical microscope image and (b) Scanning electron microscope image of fabricated AlGaN/GaN MIS-HFETs with source (S), gate (G), and drain (D) electrodes. The fabricated MIS-HFETs have a gate length $\sim$ 270 nm, a gate width $\sim$ 50 μm, a gate-source spacing $\sim$ 2 μm, and a gate-drain spacing $\sim$ 3 μm.

2.6 Summary of chapter 2

The chapter described five steps of general fabrication process method for the AlGaN/GaN MIS-HFETs. They are marker formation, Ohmic electrode formation, device isolation, gate insulator deposition, and gate electrode formation. In each step, detail conditions were mentioned and process flow was shown. For Ohmic electrode formation, nitrogen vacancy in AlGaN(GaN) is generated by reaction of Ti and N forming an n^+ region under electrodes. B^+ ion implantation is employed for the device isolation, in which deep level traps are created to compensate electrons in GaN conduction band and form high resistance area. After insulator deposition, e-beam lithography is employed to obtained fine gate patterns.

Chapter 3

BN thin films and BN/AlGaN/GaN MIS-HFETs

3.1 Deposition and characterization of BN thin films

3.1.1 RF magnetron sputtering deposition of BN thin films

BN thin films were deposited by a RF magnetron sputtering system, which is depicted in Fig. 3.1. In the sputtering system, we can adjust working gas, working pressure, RF applied power, and substrate temperature to obtain highest quality films. Deposition conditions are shown in Tab. 3.1.

Table 3.1: Conditions for BN deposition by RF magnetron sputtering.

target (100 mmϕ)	hexagonal-BN
substrate-target distance	50 mm
working gas	N_2-mixed Ar
working pressure	0.2 Pa
RF power	40 W
substrate temperature	room temperature

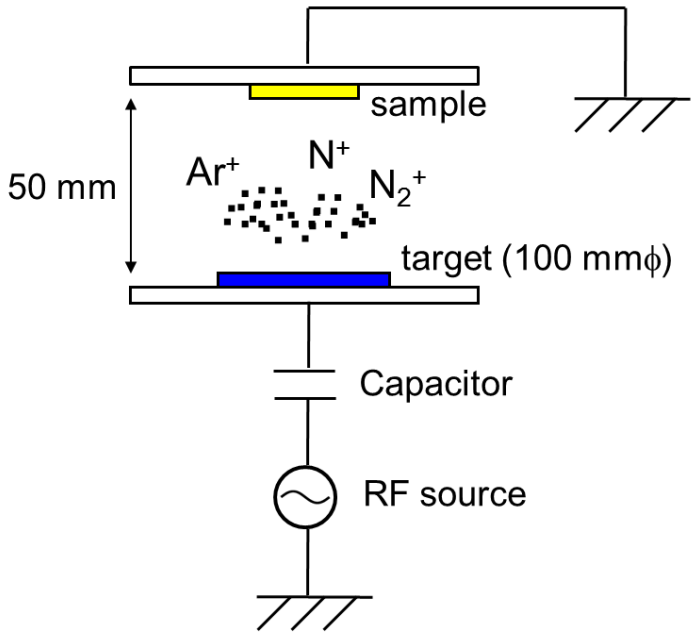


Figure 3.1: Schematic diagram of RF magnetron sputtering deposition system.

3.1.2 Characterization of BN thin films on n-Si(001) substrate

At first, in order to check BN films, BN/n-Si(001) was characterized by ellipsometry and MIS-capacitor I-V measurements. We fabricated BN/n-Si(001) MIS capacitors as follows. A Ni/Au = 5/100-nm-thick metal structure was deposited on backside of a n-Si(001) wafer, having a electron concentration 3×10^{18} cm^{-3}, and followed by an annealing at 500 °C for 5 minutes in H_2-mixed (10 %) Ar ambience to form Ohmic electrodes. After surface treatments using organic solvents and oxygen plasma ashing for removing organic contaminants and HF 6 % volume for removing oxides, a $\sim$ 20-nm-thick BN film was deposited on the Si surface by the RF magnetron sputtering deposition, as shown in Fig. 3.2(b), which was used for ellipsometry measurements. We optimized BN deposition conditions, for example, N_2 ratio, which is defined by

$$N_2 \text{ ratio} = \frac{P_{N_2}}{P_{N_2} + P_{Ar}},$$

where P_{N_2} and P_{Ar} are partial pressure of N_2 and Ar in the sputtering chamber, respectively. The N_2 ratio was changed from 0.1 to 1.0. Finally, Ni/Au = 5/200-nm-thick gate electrode, having a diameter of 100 μm, was formed to complete the device fabrication, as shown in Fig. 3.2(e), which was used for current-voltage (I-V) measurements.

We carried out ellipsometry measurements for BN/n-Si(001) using the structure shown in Fig. 3.2(b). Figure 3.3 shows refractive index n of BN film deposited at N_2 ratio = 0.5 as a function of incident-light wavelength. Typical value of n at wavelength of 630 nm is $\sim$ 1.67. n at a fixed wavelength does not depend on the N_2 ratio, as shown in Fig. 3.4. Similarly, BN-sputtering-deposition rate $\sim$ 0.033 Å/s, depicted in Fig. 3.4, also does not depend on the N_2 ratio.

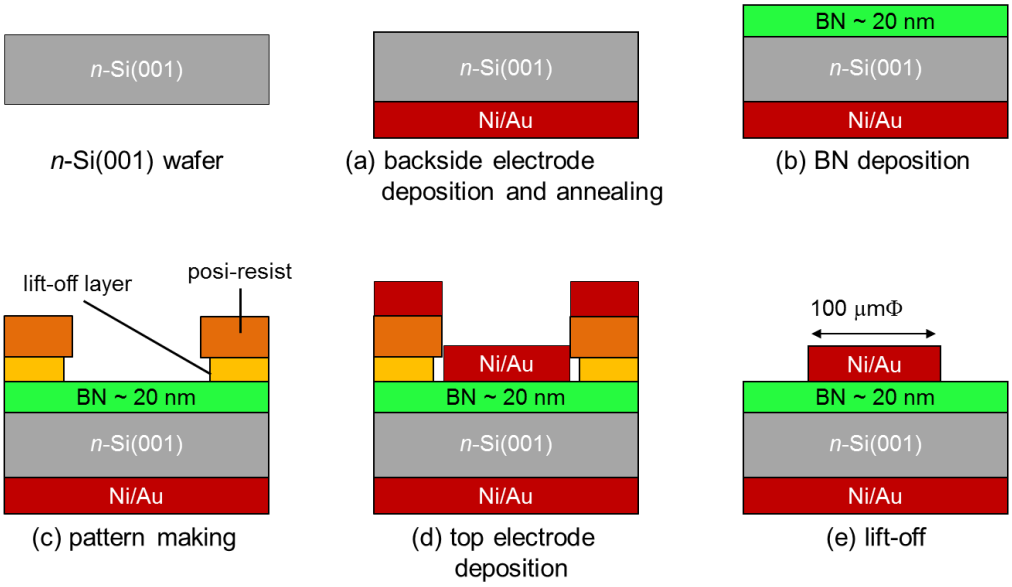


Figure 3.2: Fabrication process flow of BN/n-Si(001) MIS capacitors.

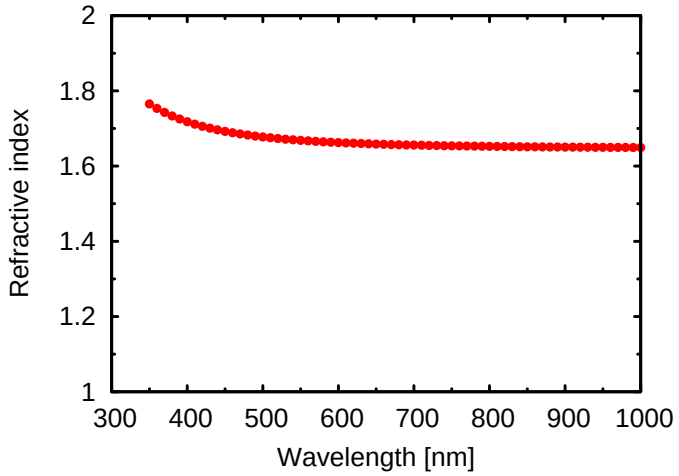


Figure 3.3: Refractive index n of BN film deposited at N_2 ratio = 0.5 as a function of wavelength obtained by ellipsometry measurement. Typical value of n at wavelength of 630 nm is $\sim$ 1.67.

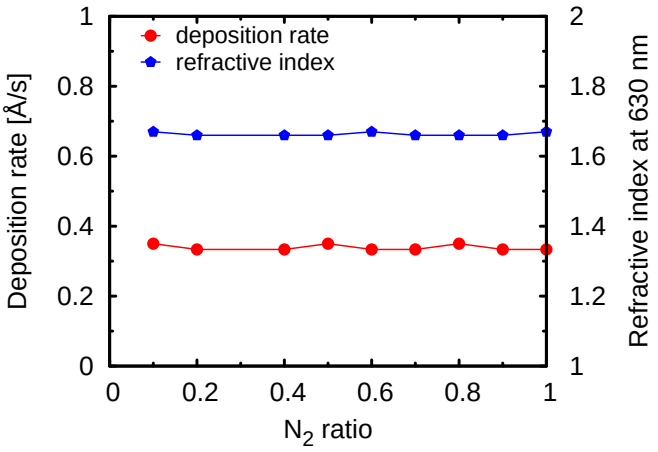


Figure 3.4: Refractive index n at 630-nm wavelength and sputtering deposition rate of the BN films are almost constant to N_2 ratio.

However, current density-voltage (J-V) characteristics, obtained from I-V measurements for BN/n-Si(001) MIS capacitors, exhibits N_2 ratio dependence, as shown in Fig. 3.5. From this, J at +4 V is depicted as a function of N_2 ratio, as shown in Fig. 3.6. We observe a U-shape of J with the lowest point at N_2 ratio ~ 0.5. At low N_2 ratio, high J may be related to N_2 vacancy, which forms donor levels near conduction band of BN, increasing conductance of the films. With increase in N_2 ratio, N_2 vacancy decreases, leading to decrease in J. At higher N_2 ratio, film damage during deposition by N^+ and/or N_2^+ may become more serious. The damage formed dangling bonds inside the films during the sputtering deposition, which increase the conductance of the BN films, leading to higher J. As a result, we obtain lowest current density at N_2 ratio ~ 0.5. Figure 3.7 shows breakdown behavior in current density-electric filed (J-F) characteristics of the BN films at the N_2 ratio = 0.5, exhibiting breakdown field $F_{\rm br} \sim 5.5$ MV/cm. We obtain high reproducibility of J and $F_{\rm br}$ for different devices, indicating high uniformity of the BN films. Based on these results, we decided to apply the sputtering deposition condition of N_2 ratio = 0.5 for fabrication of BN/AlGaN/GaN MIS-HFETs.

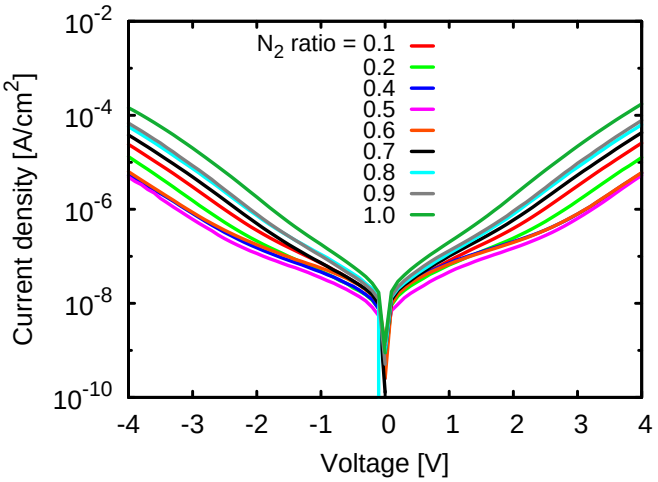


Figure 3.5: Current density-voltage (J-V) characteristics of BN/n-Si(001) MIS capacitors for several N_2 ratios.

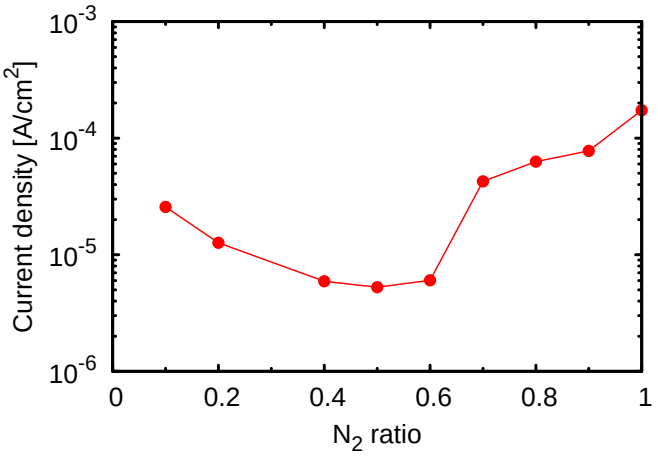


Figure 3.6: Current density J of BN/n-Si(001) MIS capacitors at voltage of +4 V as a function of the N_2 ratio.

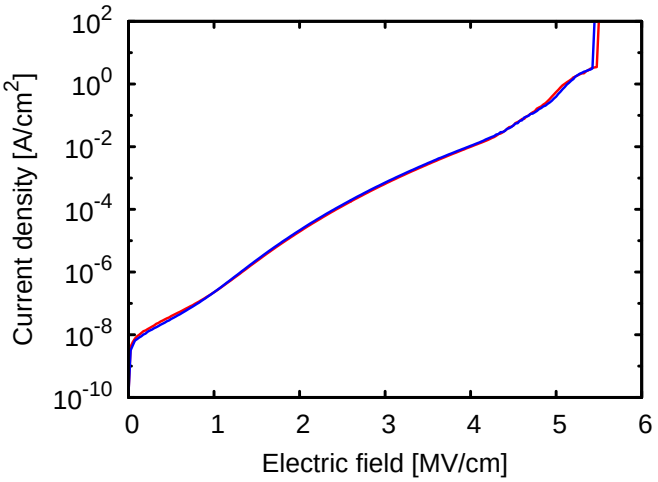


Figure 3.7: Breakdown behavior in current density-electric filed (J-F) characteristics of the BN films at the N_2 ratio = 0.5, from which breakdown filed $F_{\rm br} \sim 5.5$ MV/cm is obtained. Reproducibility of J and $F_{\rm br}$ for different capacitors indicates high uniformity of the BN films.

3.1.3 Characterization of BN thin films on AlGaN/GaN heterostructure

Using the condition, BN film was deposited on an $Al_{0.27}Ga_{0.73}N$(30 nm)/GaN(3000 nm) heterostructure obtained by metal-organic vapor phase epitaxy (MOVPE)-grown on sapphire(0001), as shown in Fig. 3.8. Hall-effect measurements for the heterostructure at room temperature before the deposition exhibited a sheet resistance $\rho_{\rm s} \sim 440\ \Omega$/sq., a sheet electron concentration $n_{\rm s} \sim 11.5 \times 10^{12}$ cm^{-2}, and an electron mobility $\mu \sim 1240$ cm^{2}V^{-1}s^{-1}.

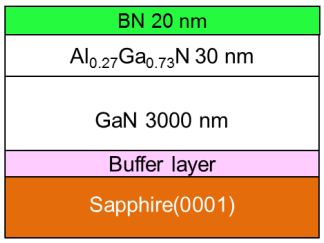


Figure 3.8: Cross section of $\sim$ 20-nm-thick BN film deposited on an $Al_{0.27}Ga_{0.73}N$(30 nm)/GaN(3000 nm) heterostructure obtained by obtained by metal-organic vapor phase epitaxy growth on sapphire(0001).

After surface treatment using organic solvents, and oxygen plasma ashing for removing organic contaminants, followed by ammonium-based solution (Semico-clean) for removing oxides, we deposited $\sim$ 20-nm-thick BN film on the AlGaN/GaN heterostructure at the condition of working gas of the N_2 ratio = 0.5. The formation of the BN on the heterostructure is depicted in Fig. 3.8. Hall-effect measurements at room temperature after the deposition exhibited $\rho_{\rm s} \sim 530\ \Omega$/sq., $n_{\rm s} \sim 9.5 \times 10^{12}$ cm^{-2}, and $\mu \sim 1250$ cm^{2}V^{-1}s^{-1}. In comparison with before deposition, the constant of μ indicates no additional scattering mechanism for 2DEG, suggesting that the decrease of $n_{\rm s}$ may be attributed to surface potential changing or

weak damage.

The sputtered BN films were characterized by XRD measurements, using Cu-$K_{\alpha 1}$ wavelength of 1.5406 Å (8047.8 eV) with a rocking curve detector. Figure 3.9 shows global XRD spectra, obtained by 2θ–ω scan, where GaN, AlGaN peaks [99], and sapphire(0001) peaks [100] are observed. However, by comparison with other XRD measurements for BN [101], we find no peak corresponding to any crystal structures of BN, suggesting an amorphous nature of the sputtered BN films.

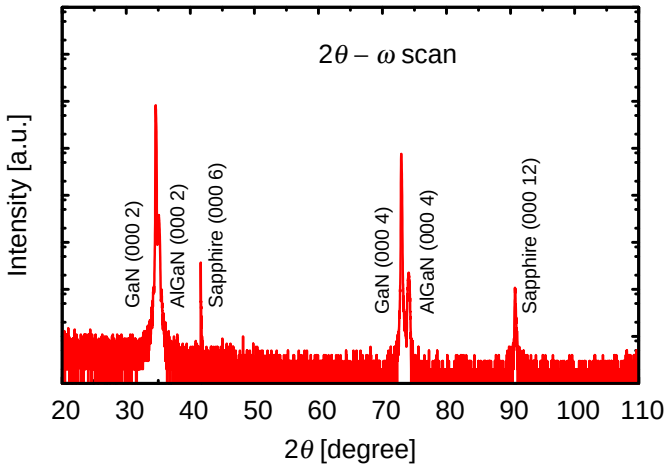


Figure 3.9: XRD measurement result for ∼ 20-nm-thick BN films on the AlGaN/GaN/sapphire(0001) heterostructure.

In addition, the BN films were also characterized by XPS using Al-K_{α} wavelength of 1486.7 eV (8.34 Å). Figure 3.10 shows global XPS spectrum, including O1s, N1s, C1s, B1s, and O2s peaks [80], in which positions of the peaks are corrected by using a C1s peak at 285.0 eV [102, 103]. By analyze B1s and N1s peaks, we obtained information for film properties. Background noise of the XPS measurements is removed by using Shirley method [104]. Figure 3.11 presents a B1s XPS peaks, which is decomposed into four peaks corresponding to B-B, B-N sp^2, B-N sp^3, and B-O bondings. Although the hexagonal-BN target used in the sputtering deposition includes only B-N sp^2 bondings, we observe that the sputtered BN films contain both B-N sp^2 and sp^3 bondings [105], where binding energy for B-N sp^3 bondings is ∼ 0.8 eV higher than that for B-N sp^2 ones [59]. The separation is similar to binding energy difference of ∼ 0.9 eV between C-C sp^3 and sp^2 bondings [106]. Moreover, the B1s signal is dominated by B-N bondings (96 %); we consider that the BN films are almost stoichiometric. In addition, we estimated energy gap E_g of the BN films from XPS N1s electron energy loss spectroscopy, which is ∼ 5.7 eV, as shown in Fig. 3.12. This is larger than that of white-graphite BN (E_g ∼ 5.2 eV), having only sp^2 bondings, and smaller than that of zincblende BN (E_g ∼ 6.4 eV), having only sp^3 bondings, indicating that it is attributed to a mixture of B-N sp^2 and sp^3 bondings in the sputtered BN films.

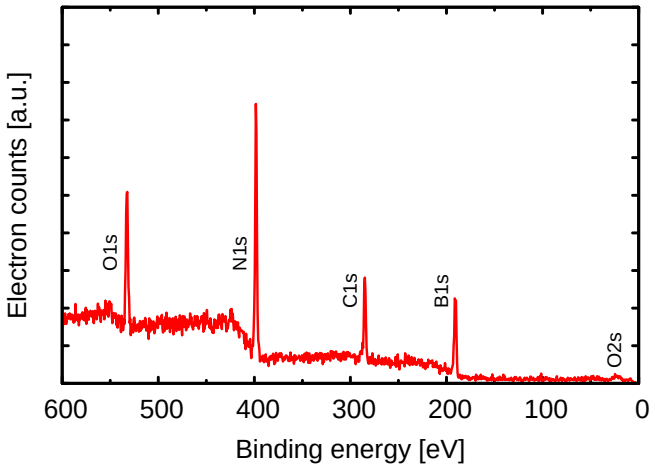


Figure 3.10: Global XPS spectra for $\sim$ 20 nm thick BN films on the AlGaN/GaN heterostructure.

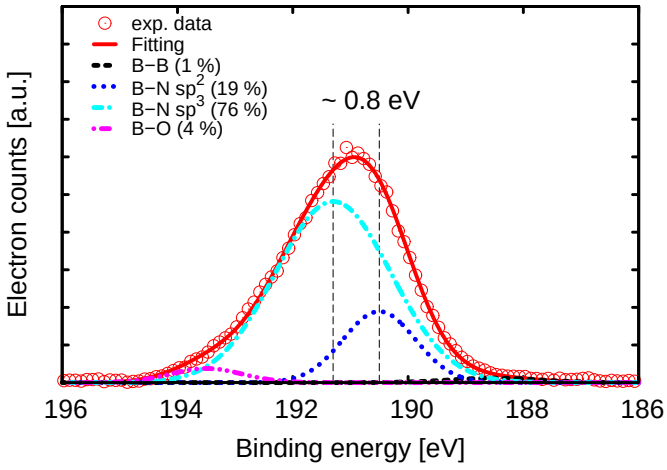


Figure 3.11: Decomposition of B1s XPS signal for $\sim$ 20-nm-thick BN films on the AlGaN/GaN heterostructure. The B1s signal is dominated by B-N bondings (96 %), indicating the BN films are almost stoichiometric.

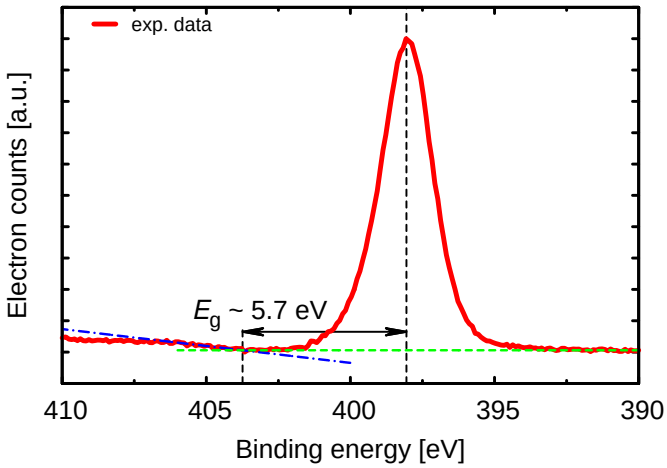


Figure 3.12: N1s electron energy loss spectroscopy for $\sim$ 20-nm-thick BN films on the AlGaN/GaN heterostructure. Estimated energy gap E_g of the sputtered-BN films is $\sim$ 5.7 eV.

3.2 Fabrication and characterization of BN/AlGaN/GaN MIS-HFETs

3.2.1 Fabrication of BN/AlGaN/GaN MIS-HFETs (BN MIS-HFETs)

By using the AlGaN/GaN heterostructure with Ohmic electrodes obtained after the device isolation (section 2.3), we fabricated BN/AlGaN/GaN MIS-HFETs (BN MIS-HFETs) as follows. The heterostructure was cleaned by a surface treatment using organic solvents and oxygen plasma ashing for removing organic contaminants, and followed by ammonium-based solution for removing oxides. Subsequently, $\sim$ 20-nm-thick BN film was deposited on the AlGaN surface by using the RF magnetron sputtering deposition at the condition of the N_2 ratio = 0.5. The other conditions are specified in Tab. 3.1. Finally, the gate electrode Ni/Au was formed on the BN, as mentioned in section 2.5, to complete the device fabrication. We also fabricated AlGaN/GaN Schottky-HFETs using the same AlGaN/GaN heterostructure for comparison. The MIS- and Schottky-HFETs have a gate length $\sim$ 270 nm, a gate width $\sim$ 50 μm, a gate-source spacing $\sim$ 2 μm, and a gate-drain spacing $\sim$ 3 μm. Schematic cross sections of the fabricated BN MIS-HFETs and Schottky-HFETs are depicted in Fig. 3.13.

3.2.2 Effects of ambiences on BN MIS-HFET characteristics

We measured characteristics of BN/AlGaN/GaN MIS-HFETs in air, vacuum, and N_2 gas of 1 atm. Figure 3.13 shows two-terminal (drain open) gate-source leakage current I_{GS} as functions of gate-source voltage V_{GS} of the BN MIS-HFET in the air, in comparison with that of the Schottky-HFETs. We obtain very low gate leakage current of 10^{-9} A/mm range or less, which is $\sim$ 4 orders at reverse biases and $\sim$ 9 orders at forward biases lower than that of the Schottky-HFETs, indicating good insulating properties of BN. In addition, I_{GS} is almost similar in the air, vacuum, and N_2 gas, as shown in Fig. 3.14, indicating that the insulating properties of BN are not influenced by the measurement ambiences.

However, we observe different threshold voltages V_{th} in the ambiences, as shown in Fig. 3.15, where V_{th} is obtained by fitting drain current I_D in the saturation region, given by [107]

$$\sqrt{I_D} \propto (V_{GS} - V_{th}). \tag{3.1}$$

From the fitting, we observe that V_{th} in the vacuum and N_2 gas are similar and shallower than that in the air. This suggests that the origin of V_{th} shift is H_2O or/and O_2 in the air.

On the other hand, we measured capacitance-voltage (C-V) characteristics at 1 MHz of BN/AlGaN/GaN MIS capacitors (BN MIS-cap.) fabricated simultaneously. The gate size of the capacitors is 100 μm $\times$ 100 μm. In contrast to the BN MIS-HFETs, we obtain similar V_{th} in the air and vacuum for the BN MIS capacitors, as shown in Fig. 3.16. This indicates that the V_{th} shift of the BN MIS-HFETs is related to effects of H_2O or/and O_2 in the air, happening surrounding the gate. Owing to the small gate length of the MIS-HFETs, the

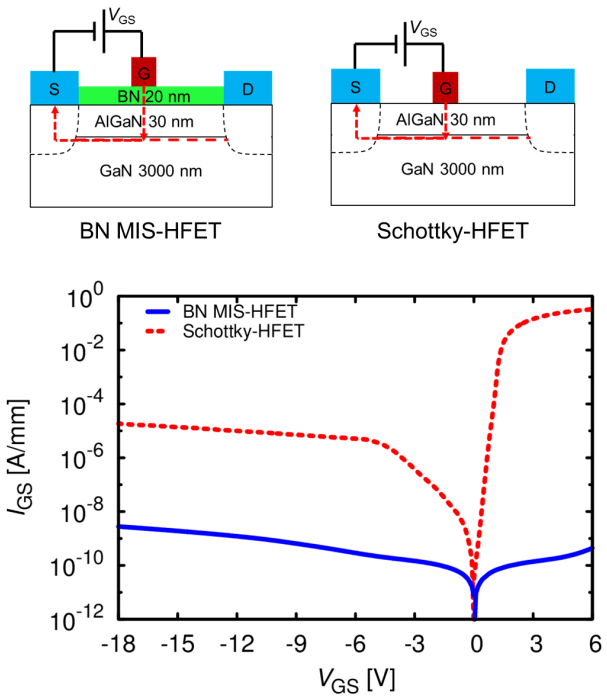


Figure 3.13: Two-terminal (drain-open) gate-source leakage currents I_{GS} as functions of gate-source voltage V_{GS} of the BN MIS-HFETs (blue solid) and the Schottky-HFETs (red dashed). V_{GS} was swept from 0 V to 6 V, and from 0 V to −18 V.

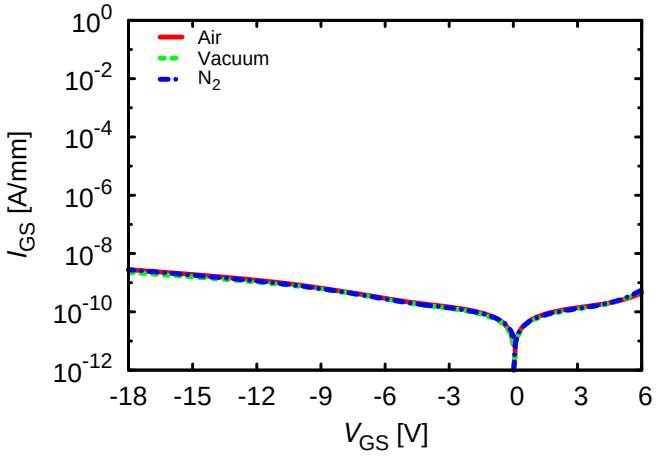


Figure 3.14: Two-terminal (drain open) gate-source leakage current I_{GS} as functions of gate-source voltage V_{GS} of the BN/AlGaN/GaN MIS-HFETs measured in air (red solid), vacuum (green dashed), and N_2 gas of 1 atm (blue dot-dashed). V_{GS} was swept from 0 V to 6 V, and from 0 V to −18 V.

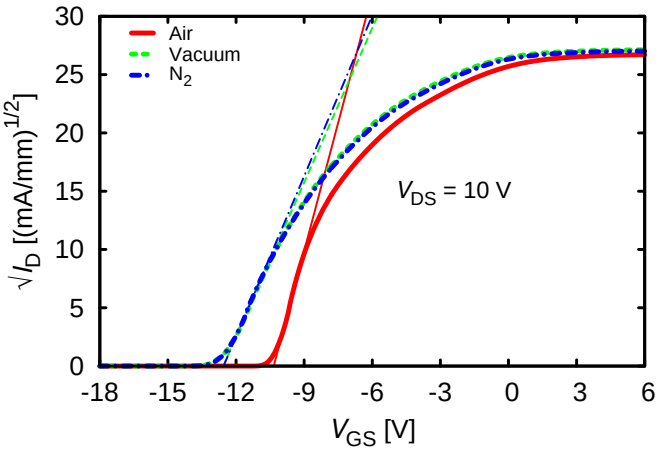


Figure 3.15: Threshold voltages $V_{\rm th}$ of the BN/AlGaN/GaN MIS-HFETs in the air, vacuum, and N_2 gas of 1 atm, under the gate-source voltage $V_{\rm GS}$ sweeps from -18 V to 6 V. $V_{\rm th}$ was obtained by fitting (thin lines) of experimental data (thick lines) using Eq. 3.1. $V_{\rm th}$ in the air is shallower than that in the vacuum and N_2 gas.

effect on the MIS-HFETs is much stronger in comparison to that on the MIS capacitors.

In addition, for BN MIS-cap. at high frequency, total capacitance $C_{\rm t}$ can be calculated by [107]

$$\frac{1}{C_{\rm t}} = \frac{1}{C_{\rm BN}} + \frac{1}{C_{\rm AlGaN}}, \tag{3.2}$$

with BN capacitance $C_{\rm BN}$ and AlGaN capacitance $C_{\rm AlGaN}$. We derive

$$C_{\rm BN} = \frac{\varepsilon_0 k_{\rm BN}}{d_{\rm BN}} = \frac{C_{\rm t} C_{\rm AlGaN}}{C_{\rm AlGaN} - C_{\rm t}}, \tag{3.3}$$

or

$$k_{\rm BN} = \frac{d_{\rm BN}}{\varepsilon_0} \times \frac{C_{\rm t} C_{\rm AlGaN}}{C_{\rm AlGaN} - C_{\rm t}}, \tag{3.4}$$

with vacuum dielectric constant ε_0, dielectric constant $k_{\rm BN}$ and thickness $d_{\rm BN}$ of the sputtered-BN films. Using values of $C_{\rm t} \sim 145$ nFcm^{-2} determined from measurements, as shown in Fig. 3.16, $d_{\rm BN} \sim 20$ nm, and $C_{\rm AlGaN} = k_{\rm AlGaN}\varepsilon_0/d_{\rm AlGaN} \sim 9 \times 8.86 \times 10^{-14}$ C/Vcm $\times\, 1/(30$ nm$) \sim$ 270 nFcm^{-2}, where $k_{\rm AlGaN}$ and $d_{\rm AlGaN}$ are dielectric constant and thickness of AlGaN layer, respectively, we obtain $C_{\rm BN} \sim 310$ nFcm^{-2} and hence, $k_{\rm BN} \sim 7$. The value of $k_{\rm BN}$ is consistent with literature values [52, 77].

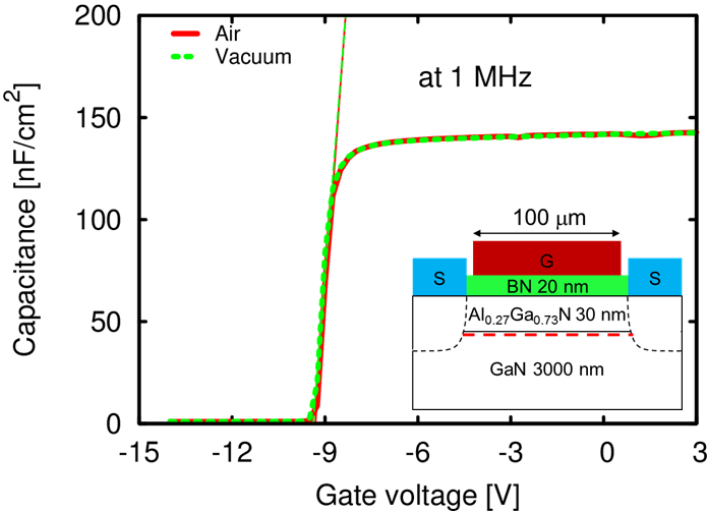


Figure 3.16: Capacitance-voltage (C-V) characteristics at 1 MHz of BN/AlGaN/GaN MIS-capacitor fabricated simultaneously. The inset shows schematic cross section of the capacitor with gate electrode size of 100 μm $\times$ 100 μm. Similar threshold voltage V_{th} in the air and vacuum are observed.

3.2.3 Temperature dependence of output and transfer characteristics of BN MIS-HFETs

In order to deeply investigate the characteristics of BN MIS-HFETs, the temperature-dependent measurements were carried out in the vacuum, using TTP4 probe station of Lake Shore Cryotronics, shown in Fig. 3.17. Temperature T, controlled by heater and liquid N_2, was varied from 150 K to 400 K. Agilent 4155A - Semiconductor Parameter Analyzer was used to measure output and transfer characteristics, and gate leakage currents at every temperature point.

Figure 3.18 shows temperature-dependent output characteristics of the BN MIS-HFETs, obtained under V_{GS} changing from negative to positive with a step of 1 V and a maximum of +3 V. We observe high maximum drain currents, indicating that damage by BN sputtering deposition is weak. In addition, there is no negative conductance, indicating almost no self-heating [51, 55, 108], suggesting good heat release properties owing to the excellent thermal conductivity of BN [72, 78].

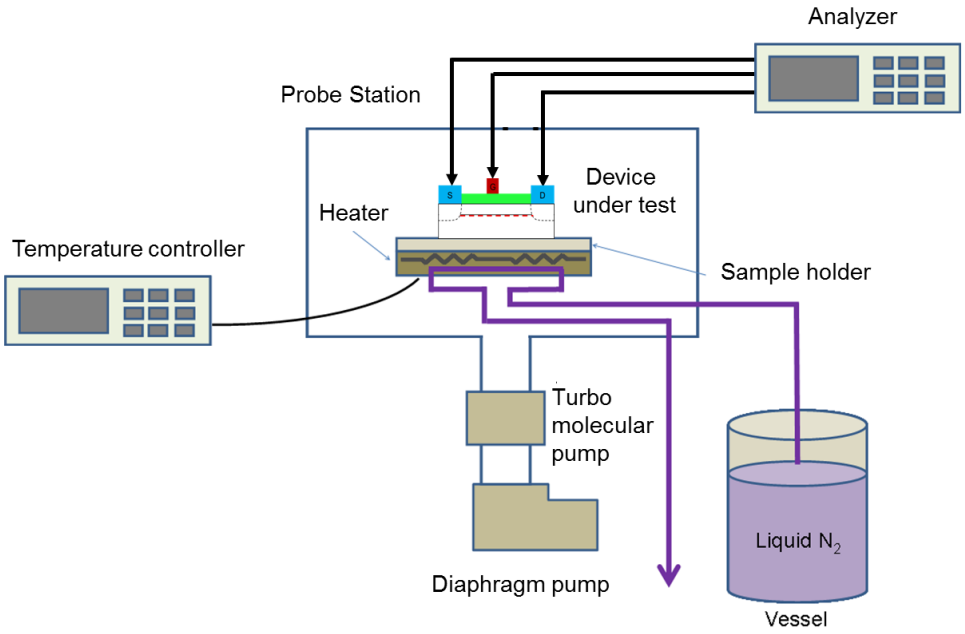
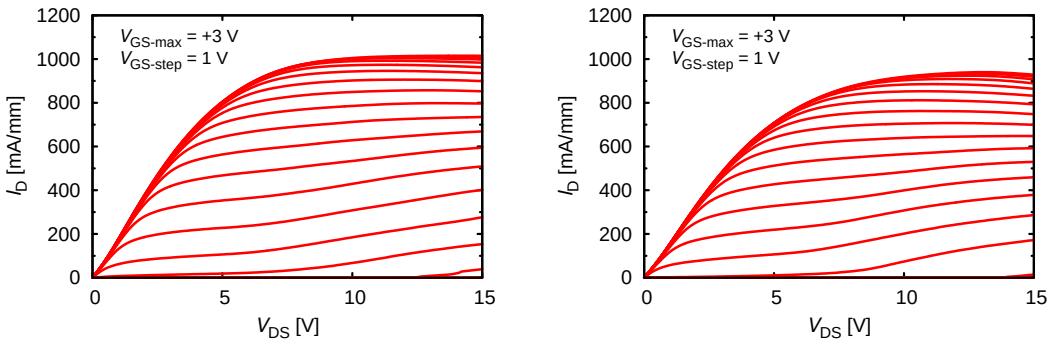
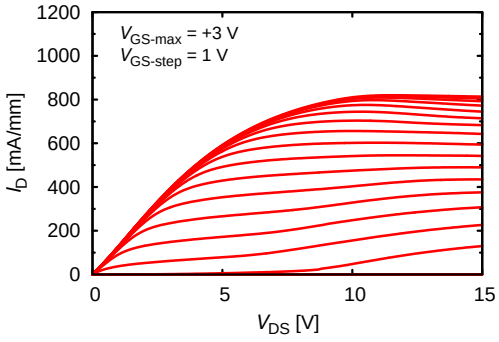


Figure 3.17: Configuration of the temperature-dependent measurement system.

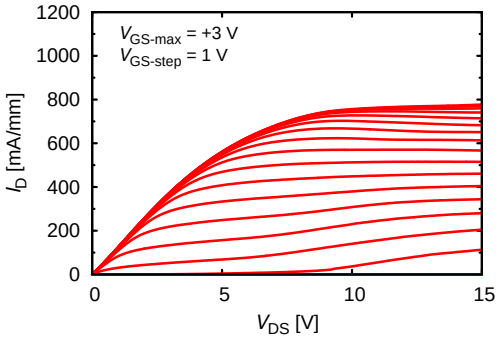


(a) 150 K

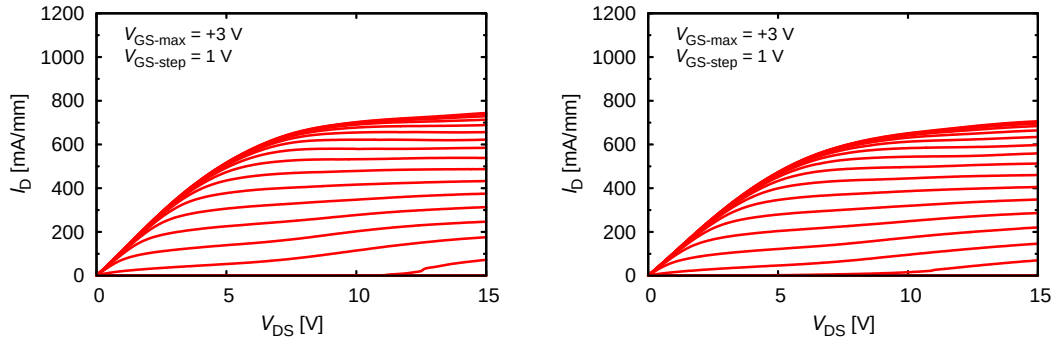
(b) 200 K



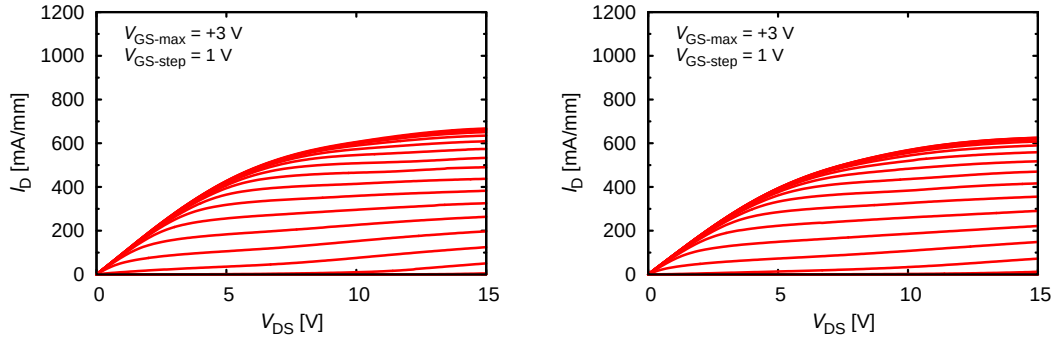
(c) 250 K



(d) 275 K



(e) 300 K (f) 330 K



(g) 360 K (h) 400 K

Figure 3.18: Output characteristics of the BN/AlGaN/GaN MIS-HFETs at temperature from 150 K to 400 K, obtained under gate-source voltage V_{GS} changing from negative to positive with a step of 1 V and a maximum of +3 V.

With regarding to elucidate temperature-dependent channel conduction, we analyzed drain currents I_D at $V_{GS} = 0$ V, as depicted in Fig. 3.19(a). From that data, drain currents I_D in linear (low voltage) region and saturation (high voltage) region were plotted as functions of temperature T, as shown in Fig. 3.19(b). With increase in T, I_D in linear and saturation regions decrease.

On-resistance R_{on}, which is proportional to $1/I_D$ in the linear region, increases ~ 2 times from 150 K to 400 K, as shown in Fig. 3.20(a). On the other hand, Hall-effect measurement results show that n_s is almost constant and $1/\mu$ increases ~ 4 times from 150 K to 402 K, as shown in Fig. 3.20(b). The temperature dependence of $1/\mu$ is similar to Monte-Carlo simulation results [109], as shown in Fig. 3.20(b), and experimental results [110]. As a result, the temperature dependence of $\rho_s = 1/qn_s\mu$, where q is the electron charge, increases ~ 4 times. In comparison, the temperature dependence of ρ_s is stronger than that of R_{on}, given by $R_{on} \simeq 2R_c + \rho_s L_{SD}$, with source-drain spacing L_{SD}, indicating that the effect of contact resistance R_c to R_{on} is strong.

Furthermore, I_D in the saturation region is proportional to the average electron velocity v_{ave}, which should be in-between low-field and high-field velocities. Figure 3.21 shows the relative temperature-dependent v_{ave} obtained by I_D in the saturation region, in comparison with the low- and high-field velocities obtained by Monte-Carlo simulations (v_{LMC} and v_{HMC}) [109]. In fact, the temperature dependence of v_{ave} is in-between those of v_{LMC} and v_{HMC},

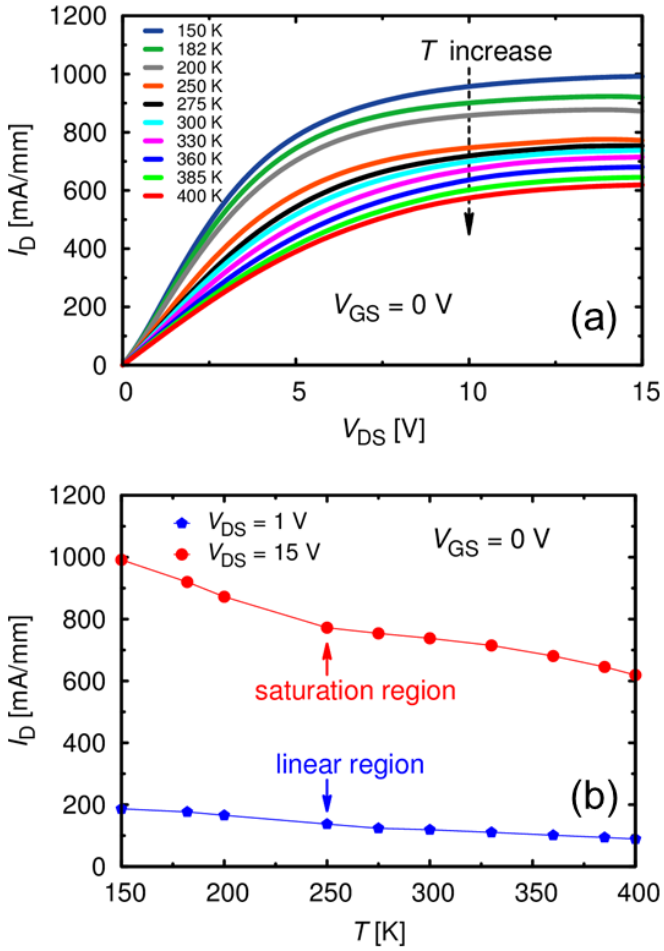


Figure 3.19: (a) Temperature-dependent drain currents I_D at gate-source voltage $V_{GS} = 0$ V. (b) Temperature dependence of I_D in linear (low-voltage) region ($V_{DS} = 1$ V) and saturation (high-voltage) region ($V_{DS} = 15$ V). With increase in temperature T, I_D in the both regions decreases.

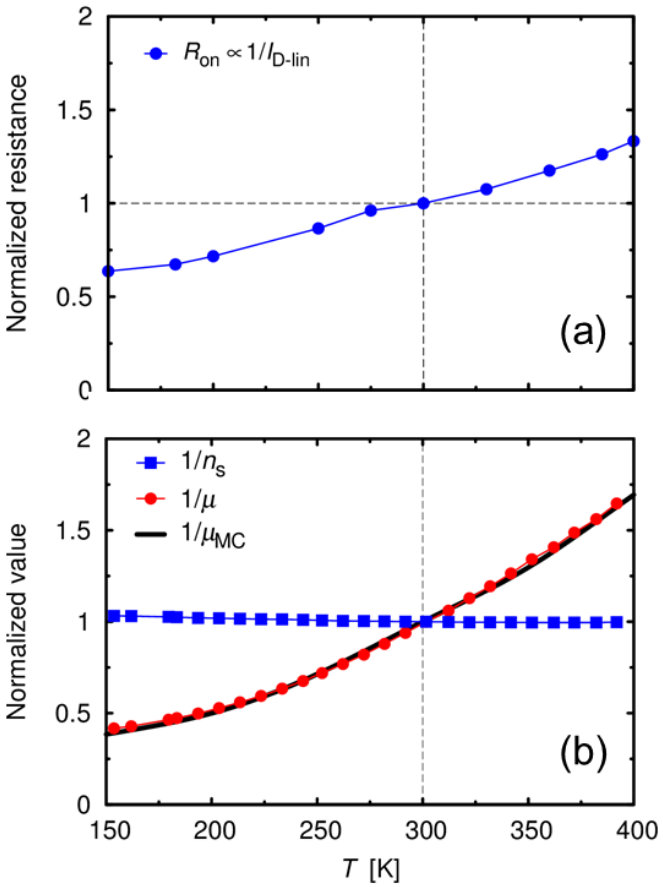


Figure 3.20: (a) Temperature dependence of on-resistance R_{on} obtained by drain current inverse $1/I_D$ in the linear region. (b) Temperature dependence of the normalized electron mobility inverse $1/\mu$ and the sheet electron concentration inverse $1/n_s$ obtained by Hall-effect measurements. The mobility μ is compared with the Monte-Carlo-simulated μ_{MC}.

where v_{LMC} shows a stronger dependence and v_{HMC} shows a weaker dependence, as indicated by experiments [51, 111].

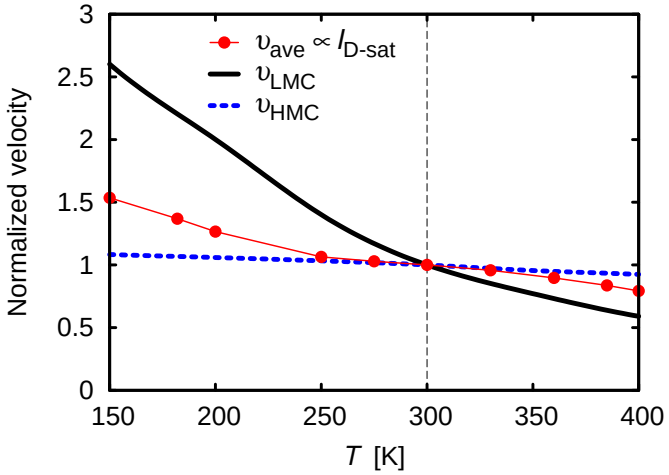
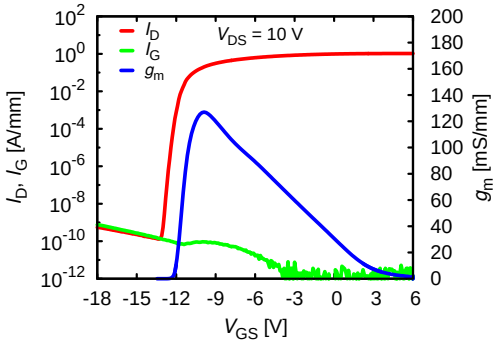
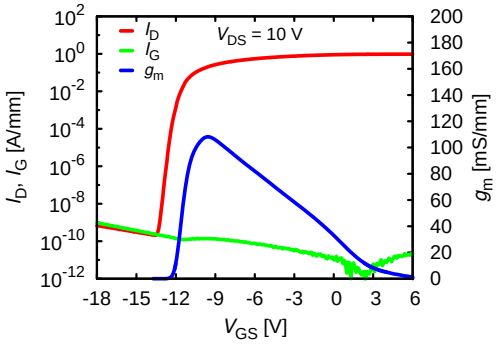


Figure 3.21: Relative temperature-dependent average velocity v_{ave}, obtained by drain current I_{D} in the saturation region, in comparison with the low- and high-field velocities obtained by Monte-Carlo simulations (v_{LMC} and v_{HMC}).

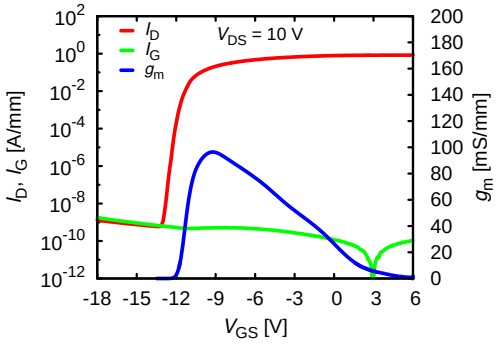
Figure 3.22 exhibits transfer characteristics of the BN/AlGaN/GaN MIS-HFETs at temperatures from 150 K to 400 K. Drain current I_{D}, gate current I_{G}, and transconductance g_{m} are obtained at $V_{\mathrm{DS}} = 10$ V and V_{GS} sweep from -18 V to $+6$ V. We obtain high drain current on/off ratios, which is ~ 8 orders at 300 K. We observe high g_{m} peak, but rapid decrease for forward biases, indicating a weak gate controllability, suggesting high-density BN/AlGaN interface states. In addition, gate leakage increases with increase in temperature.



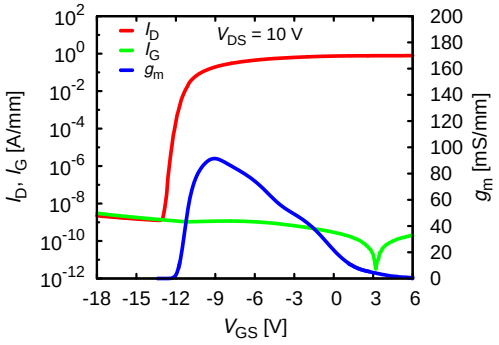
(a) 150 K



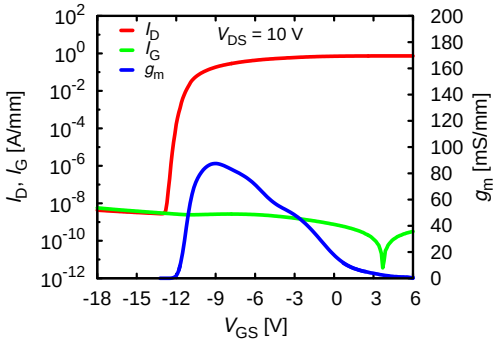
(b) 200 K



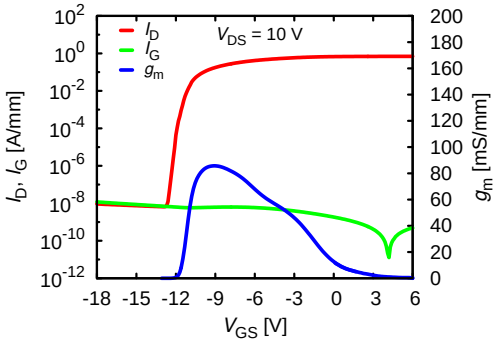
(c) 250 K



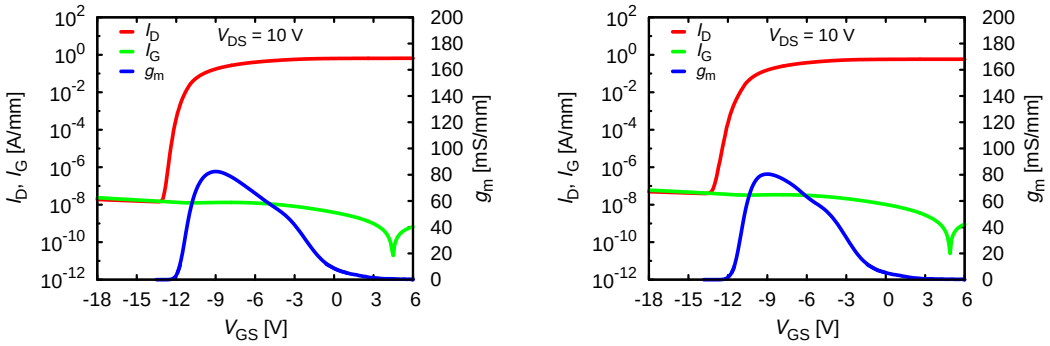
(d) 275 K



(e) 300 K



(f) 330 K



(g) 360 K (h) 400 K

Figure 3.22: Transfer characteristics of the BN/AlGaN/GaN MIS-HFETs at temperature from 150 K to 400 K, where drain current I_D, gate current I_G, and transconductance g_m were obtained under gate-source voltage V_{GS} sweep of -18 V $\rightarrow +6$ V at drain-source voltage V_{DS} of 10 V.

3.2.4 Temperature dependence of gate leakage of BN MIS-HFETs

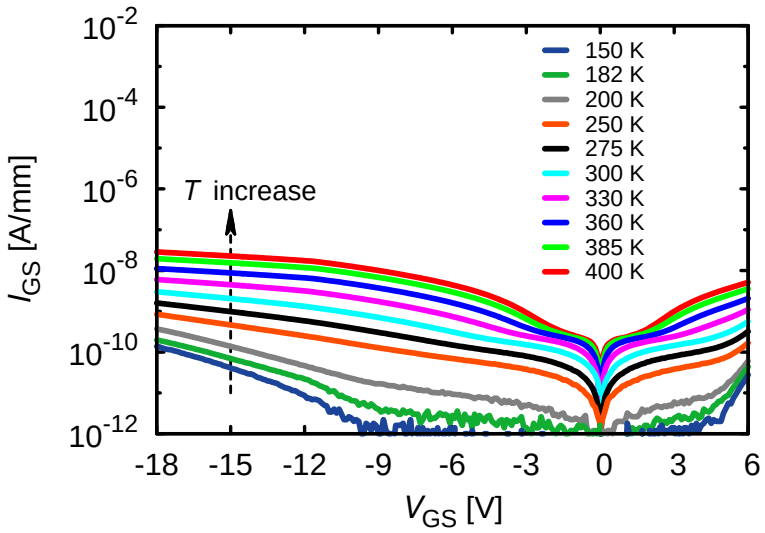


Figure 3.23: Temperature-dependent two-terminal (drain open) gate-source leakage current I_{GS} as functions of gate-source voltage V_{GS} of the BN/AlGaN/GaN MIS-HFETs. V_{GS} was swept from 0 V to +6 V, and from 0 V to -18 V. With increase in temperature T, I_{GS} increases.

In order to elucidate temperature-dependent gate leakage of the BN MIS-HFETs, we carried out two-terminal (drain open) I-V measurements, shown in Fig. 3.23. We obtain gate leakage increases (or decreases) with the increase (or decrease) in temperature, suggesting that gate leakage is attributed to thermal process. With regard to explain the behavior, we

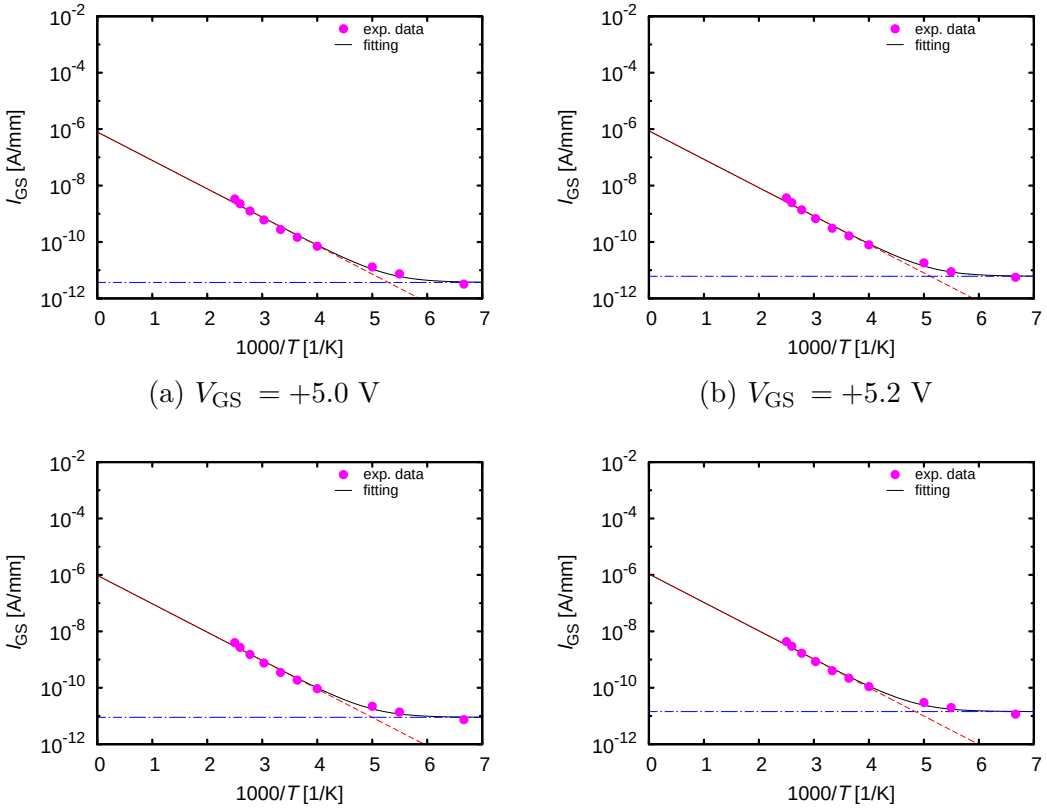
fitted gate-source leakage current I_{GS} using a function

$$I_{\mathrm{GS}}(V_{\mathrm{GS}}, T) = I_0(V_{\mathrm{GS}}) \exp\left[-\frac{E_{\mathrm{a}}(V_{\mathrm{GS}})}{k_{\mathrm{B}}T}\right] + I_1(V_{\mathrm{GS}}), \tag{3.5}$$

with Boltzmann constant k_{B}, activation energy E_{a}, and prefactors I_0 and I_1, where the first term is temperature-dependent and the second term is temperature-independent. We obtain the well fitting at large forward biases, shown in Fig. 3.24. Fitting results are summarized in Fig. 3.25, where $I_0(V_{\mathrm{GS}})$ and $I_1(V_{\mathrm{GS}})$ exponentially increase, as shown in Fig. 3.25(a), while $E_{\mathrm{a}}(V_{\mathrm{GS}})$ is almost constant, as shown in Fig. 3.25(b), with increase in V_{GS} at large forward biases. These indicate that the first term does not obey Poole-Frenkel (PF) mechanism, given by [112, 113]

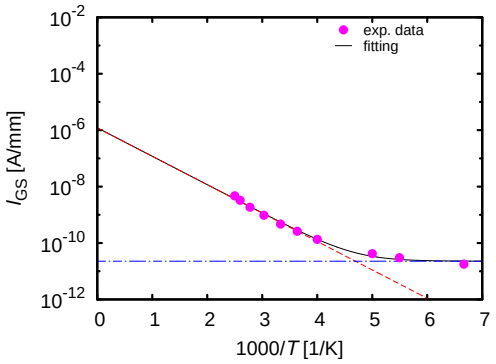
$$I_{\mathrm{PF}}(F, T) \propto F \exp\left[-\frac{1}{k_{\mathrm{B}}T}\left(\phi - \sqrt{\frac{q^3 F}{\pi \varepsilon_0 k}}\right)\right],$$

which is obtained in appendix A, with electron charge q, vacuum dielectric constant ε_0, insulator relative dielectric constant k, electric field in BN F, and trap depth ϕ, in which the exponential part is a function of F and the prefactor is a linear function of F or applied voltage.

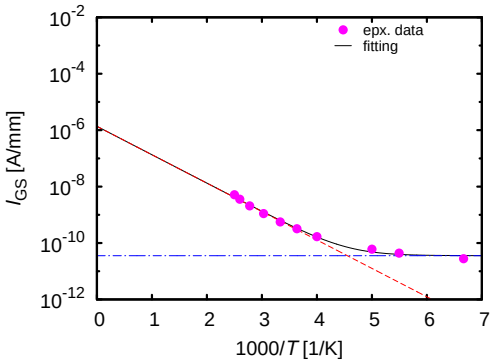


(a) $V_{\mathrm{GS}} = +5.0$ V (b) $V_{\mathrm{GS}} = +5.2$ V

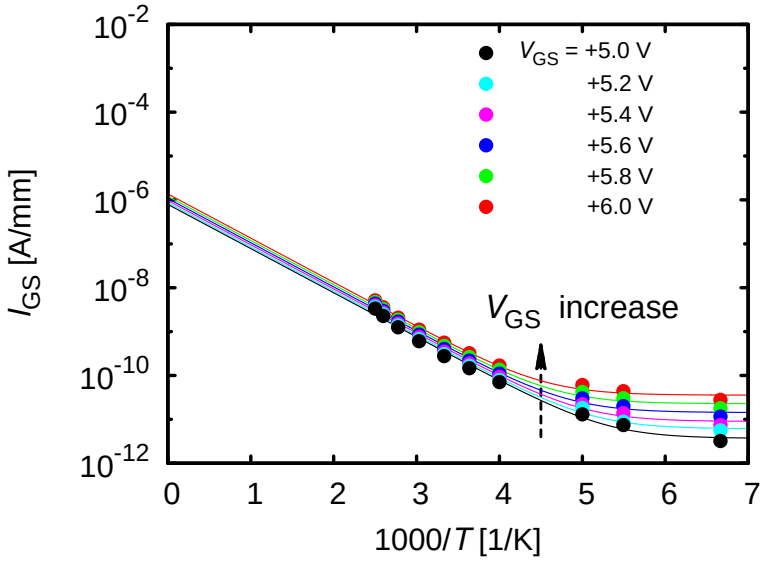
(c) $V_{\mathrm{GS}} = +5.4$ V (d) $V_{\mathrm{GS}} = +5.6$ V



(e) V_{GS} = +5.8 V



(f) V_{GS} = +6.0 V



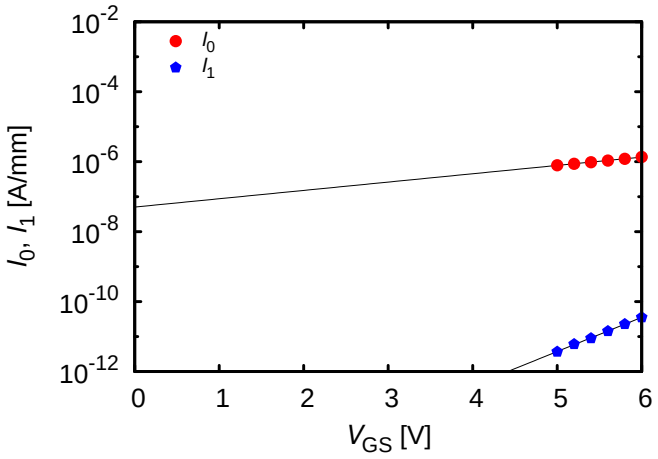
(g) Summary

Figure 3.24: (a) - (f) Two-terminal (drain open) gate-source leakage current I_{GS} at several large forward biases are well fitted by Eq. 3.5, in which red dashed line is temperature-dependent and blue dot-dashed line is temperature-independent. (g) Summary of the fitting for the large forward biases.

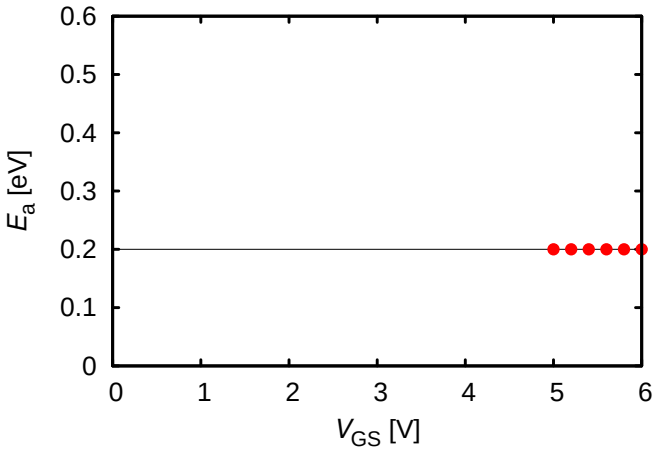
In order to explain the behaviors, we propose a mechanism with temperature-enhanced tunneling corresponding the first term, and temperature-independent tunneling, corresponding the second term, as depicted in Fig. 3.26(a). The temperature-enhanced tunneling is given by thermal electron trapping at BN/AlGaN interface states with the activation energy E_a, implicating temperature dependence, and following electron tunneling through BN barrier, which exponential increases with increase in V_{GS} [114]. The temperature-independent tunneling is given by electron tunneling through AlGaN, BN/AlGaN interface, and BN barriers, which also exponential increases with increase in V_{GS}.

We can estimate BN/AlGaN interface state density D_i by considering an equivalent circuit for DC limit, as shown in Fig. 3.26(b) [115]. From the circuit, the gate voltage change ΔV_{GS} is divided into BN ΔV_{BN} and AlGaN ΔV_{AlGaN}, given by

$$\Delta V_{GS} = \Delta V_{BN} + \Delta V_{AlGaN}. \tag{3.6}$$



(a) Prefactor I_0 and I_1 as functions of V_{GS}.



(b) Activation energy E_a as a function of V_{GS}.

Figure 3.25: Fitting results at large forward biases for gate leakage currents of BN/AlGaN/GaN MIS-HFETs.

Fitting result of E_a indicates that $\Delta V_{AlGaN} \sim 0$ at high forward biases, or the voltage ratio

$$\frac{\Delta V_{AlGaN}}{\Delta V_{GS}} \sim 0. \tag{3.7}$$

From the equivalent circuit, we can obtain charge distribution in BN and AlGaN and interface, given by

$$\Delta V_{BN} C_{BN} = \Delta V_{AlGaN}(C_{AlGaN} + C\mathrm{i}) = \Delta V_{AlGaN}(C_{AlGaN} + q^2 D\mathrm{i}),$$

or

$$\Delta V_{BN} = \Delta V_{AlGaN} \frac{C_{AlGaN} + q^2 D_i}{C_{BN}}, \tag{3.8}$$

with BN capacitance C_{BN}, AlGaN capacitance C_{AlGaN} and BN/AlGaN interface state capacitance C_i obtained from D_i. Substitute Eq. 3.8 into Eq. 3.6 and compare with Eq. 3.7, we derive the voltage ratio

$$\frac{\Delta V_{AlGaN}}{\Delta V_{GS}} = \frac{C_{BN}}{C_{BN} + C_{AlGaN} + q^2 D_i} \sim 0. \tag{3.9}$$

This leads to

$$q^2 D_i \gg C_{BN}. \tag{3.10}$$

From this, by using values of $C_{BN} \sim 310$ nFcm^{-2}, we obtain BN/AlGaN interface state density $D_i \gg 10^{12}$ cm^{-2}eV^{-1} ($> 10^{13}$ - 10^{14} cm^{-2}eV^{-1}). Due to the high D_i near the conduction band according to the U-shaped density of states of the BN/AlGaN interface, for large forward biases, AlGaN/GaN band is not effectively modulated by gate voltage change, but BN is modulated, leading to almost constant of E_a, exponentially increase of I_0 and I_1 to V_{GS}. These results in the weak gate controllability for the BN MIS-HFETs.

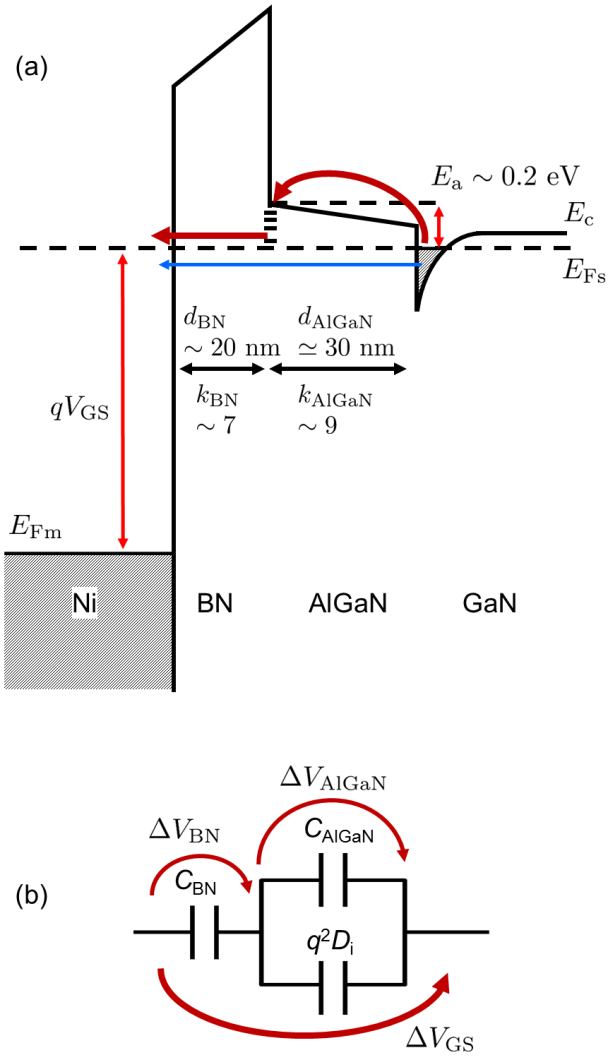


Figure 3.26: (a) Conduction band diagram of Ni/BN/AlGaN/GaN showing a mechanism with temperature-enhanced tunneling and temperature-independent tunneling. (b) The equivalent circuit for the DC limit [E. H. Nicollian and J. R. Brews] with BN capacitance C_{BN}, AlGaN capacitance C_{AlGaN}, and BN/AlGaN interface state density D_i, including applied voltage V_{GS}, voltage V_{BN} dropped on BN, and V_{AlGaN} dropped on AlGaN.

3.3 Summary of chapter 3

BN possesses several advantageous properties, such as high F_{br}, high k, and very high κ. Therefore, we consider that BN is favorable as a gate insulator for the MIS-HFETs. In this chapter, we characterized physical properties of amorphous BN thin films obtained by RF magnetron sputtering, which have $E_{\mathrm{g}} \sim 5.7$ eV, $F_{\mathrm{br}} \sim 5.5$ MV/cm, and $k \sim 7$.

Using the BN films, we fabricated BN/AlGaN/GaN MIS-HFETs (BN MIS-HFETs), which exhibit very low gate leakage current, indicating good insulating properties of BN. In addition, the insulating properties of BN are not influenced by measurement ambiences. However, threshold voltage in the air is shallower than that in the vacuum and N_2 gas, suggesting that the origin of the threshold voltage shifts is H_2O or/and O_2 in the air.

We carried out temperature-dependent measurements for the BN MIS-HFETs in the vacuum. We do not observe negative conductance in drain current I_{D}, suggesting good thermal release properties owing to the excellent thermal conductivity of BN. We obtain decreasing drain current and increasing gate current with increase in temperature. We analyzed temperature-dependent channel conduction of the BN MIS-HFETs, where I_{D} decreases with increase in temperature. In the linear region, the decrease in I_{D} is attributed to decrease in the electron mobility, while the sheet electron concentration is constant. In the saturation region, the decreased I_{D} is proportional to the average electron velocity, whose temperature dependence is in-between those of the low- and high-field velocities.

Furthermore, we elucidated the temperature-dependent gate leakage, attributed to a mechanism with temperature-independent tunneling, dominant at low temperatures, and temperature-enhanced tunneling, dominant at high temperatures, from which we estimated the BN/AlGaN interface state density, which is $\gg 10^{12}$ $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ ($> 10^{13}$ - 10^{14} $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$). High-density BN/AlGaN interface states leads to the weak gate controllability for the BN MIS-HFETs.

Chapter 4

AlTiO thin films and AlTiO/AlGaN/GaN MIS-HFETs

4.1 Deposition and characterization of AlTiO thin films

4.1.1 Atomic layer deposition of AlTiO thin films

Al_xTi_yO thin films were deposited by ALD using trimethyl aluminum ($Al[CH_3]_3$ - TMA), tetrakis-dimethylamino titanium ($Ti[N(CH_3)_2]_4$ - TDMAT), and H_2O [89]. Molecular structure of TMA and TDMAT are drawn in Fig. 4.1 [116]. For Al_2O_3 deposition by TMA-H_2O supply with reaction equation

$$2Al[CH_3]_3+3H_2O \rightarrow Al_2O_3+6CH_4,$$

we obtained a growth rate of 1.1 Å/cycle (0.31 monolayer/cycle). On the other hand, for TiO_2 deposition by TDMAT-H_2O supply with reaction equation

$$Ti[N(CH_3)_2]_4+2H_2O \rightarrow TiO_2+4HN(CH_3)_2,$$

we obtained a growth rate of 0.72 Å/cycle (0.23 monolayer/cycle). Schematic diagram of the deposition for Al_2O_3 and TiO_2 is shown in Fig. 4.2 [117].

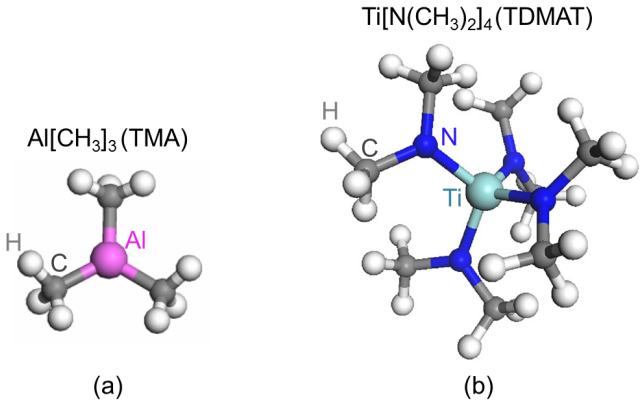


Figure 4.1: Molecular structure of (a) trimethylaluminum (TMA) and (b) tetrakis-dimethylamino titanium (TDMAT) [Airliquide].

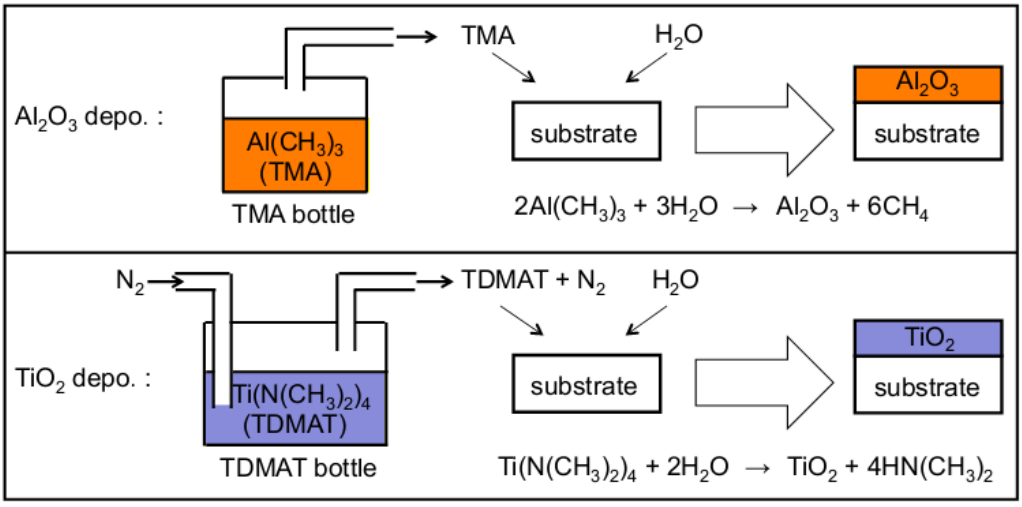


Figure 4.2: Schematic diagram of atomic layer deposition for Al_2O_3 with trimethylaluminum (TMA)-H_2O supply and TiO_2 with tetrakis-dimethylamino titanium (TDMAT)-H_2O supply.

4.1.2 Characterization of AlTiO thin films on n-GaAs(001) substrate

At first, in order to check AlTiO films, AlTiO/n-Si(001) was characterized by XPS, ellipsometry and MIS-capacitor I-V measurements. We fabricated Al_xTi_yO/n-GaAs(001) MIS capacitors as follows. An AuGe/Ni/Au metal structure was deposited on backside of a n-GaAs(001) wafer, having a electron concentration 1.6×10^{18} cm^{-3}, and followed by an annealing at 400 °C for 1 minutes in H_2-mixed (10 %) Ar ambience to form Ohmic electrodes. After surface treatments using organic solvents and oxygen plasma ashing for removing organic contaminants and ammonium-based solution for removing oxides, a $\sim$ 25-nm-thick Al_xTi_yO film was deposited on the GaAs surface by ALD, and followed by an annealing at 350 °C for 30 minutes in H_2-mixed (10 %) Ar ambience. In order to investigate physical properties of the Al_xTi_yO films, we deposited the films at different compositions, which is controlled by alternative supply of l-cycle TMA-H_2O and m-cycle TDMAT-H_2O, as shown in Fig. 4.3(b), where 6 combinations of $(l, m) = (0, 1)$, $(1, 3)$, $(1, 2)$, $(1, 1)$, $(2, 1)$, and $(1, 0)$ were employed. Finally, Ni/Au = 5/200 nm gate electrodes, having a diameter of 100 μm, were formed to complete the device fabrication. The schematic cross section of fabricated Al_xTi_yO/n-GaAs(001) MIS capacitors is shown in Fig. 4.3(e).

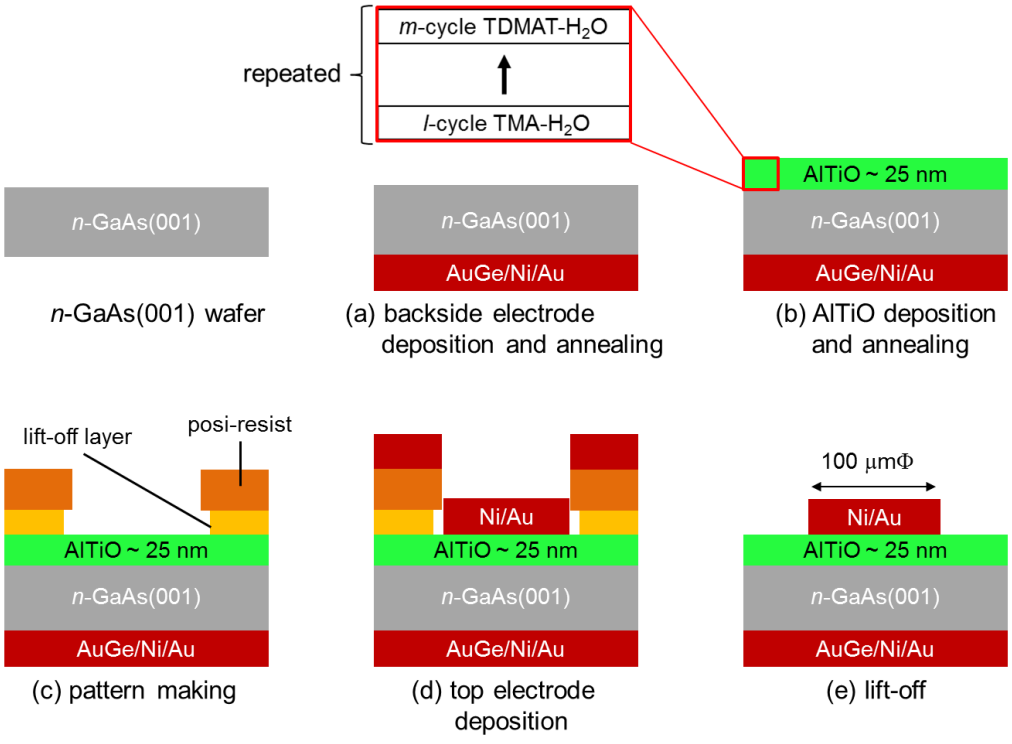


Figure 4.3: Fabrication process flow of AlTiO/n-GaAs(001) MIS capacitor.

We carried out XPS and ellipsometry measurements for the AlTiO films by using the structure shown in Fig. 4.3(b). Figure 4.4 shows global XPS spectra, including Al2s, Al2p, Ti2p, Ti3s and Ti3p peaks, which give the atomic compositions $x : y$. By integral peak

intensity ratios of Al2s, Al2p, Ti2p, Ti3s and Ti3p, we observe a good linear relation

$$\frac{x}{x+y} \simeq \frac{2.7l}{m+2.7l},$$

as shown in Fig. 4.5. From the relation, we found that $(l, m) = (0, 1)$, $(1, 3)$, $(1, 2)$, $(1, 1)$, $(2, 1)$, and $(1, 0)$ give $x : y = 0 : 1$, $0.47 : 0.53$, $0.57 : 0.43$, $0.73 : 0.27$, $0.84 : 0.16$, and $1 : 0$, respectively. In addition, XPS measurements give O1s electron energy loss spectra, from which we obtain energy gap E_g of the Al_xTi_yO films, as shown in Fig. 4.6, which increases with increase in the Al composition. Fig. 4.6 also shows the refractive index n at wavelength of 630 nm, obtained by ellipsometry measurements, which decreases with increase in the Al composition.

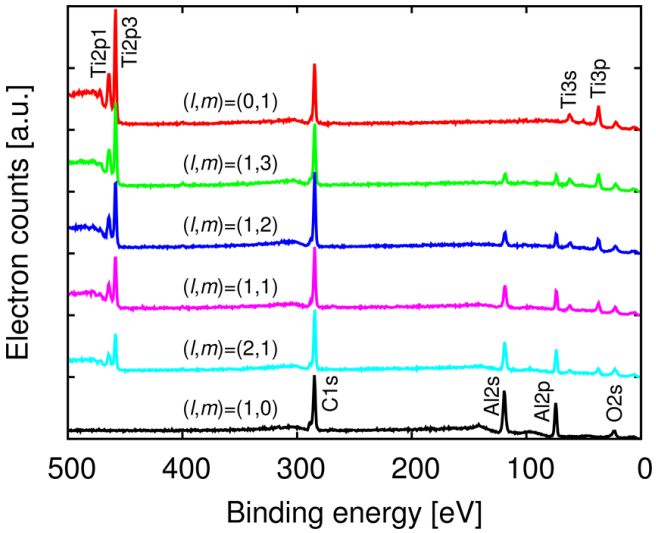


Figure 4.4: Global XPS spectra for ∼ 25-nm-thick AlTiO thin films on n-GaAs(001), including Ti2p1, Ti2p3, Al2s, Al2p, Ti3s, and Ti3p peaks, giving the atomic compositions.

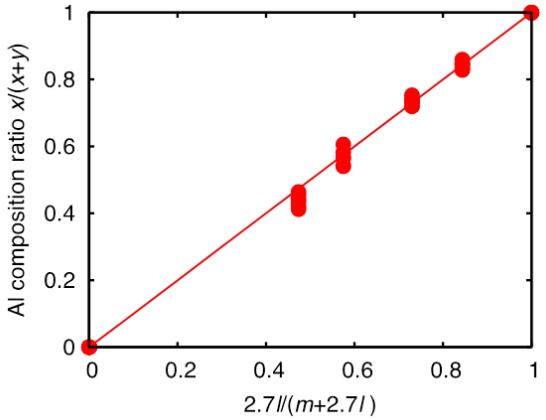


Figure 4.5: Relation between cycle numbers l and m and Al composition ratio $x/(x + y)$ obtained by integral XPS peak intensity of Al (Al2s, Al2p) and Ti (Ti2p, Ti3s, and Ti3p) XPS peaks.

We measured temperature-dependent J-V characteristics of Al_xTi_yO/n-GaAs(001) MIS capacitors, using the prober drawn in Fig. 3.17. Figure 4.7 shows breakdown behavior of J

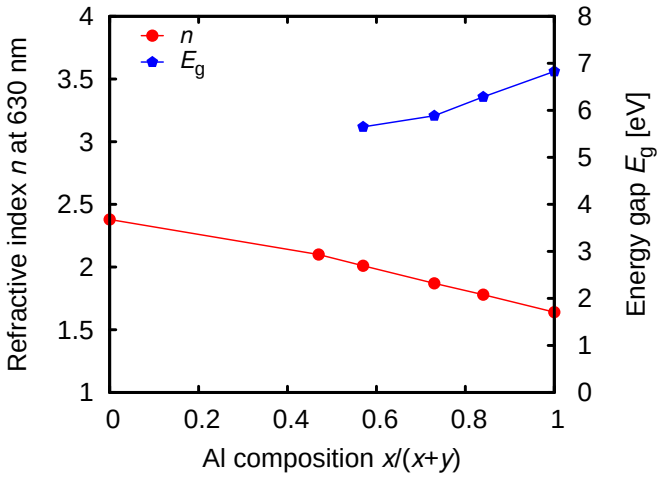


Figure 4.6: Relation between the Al compositions and refractive index n at 630-nm wavelength and energy gap E_g of the Al_xTi_yO films.

at room temperature as a function of electric field F of the Al_xTi_yO ($x/(x+y) = 0.47$-1). As a result, we obtain the breakdown field F_{br} of the films, as given in Fig. 4.8, which is $\sim$ 5-7 MV/cm and increases with increase in the Al composition. We can not obtain the breakdown behavior and F_{br} of TiO_2 ($x/(x+y) = 0$) due to the large current. In addition, we found that Al_xTi_yO MIS capacitors ($x/(x+y)$=0.47-0.84) exhibit Poole-Frenkel (PF) conduction, from which, we estimated the dielectric constants k which increases with decrease in the Al composition [89], as shown in Fig. 4.8. Considering the trade-off between F_{br} and k, we applied Al_xTi_yO with $x/(x+y) = 0.73$ to AlTiO/AlGaN/GaN MIS-HFETs, where the AlTiO has $F_{br} \sim 6.5$ MV/cm, $k \sim 24$ obtained by the PF analysis, and $E_g \sim 6$ eV obtained by the XPS O1s electron energy loss spectra.

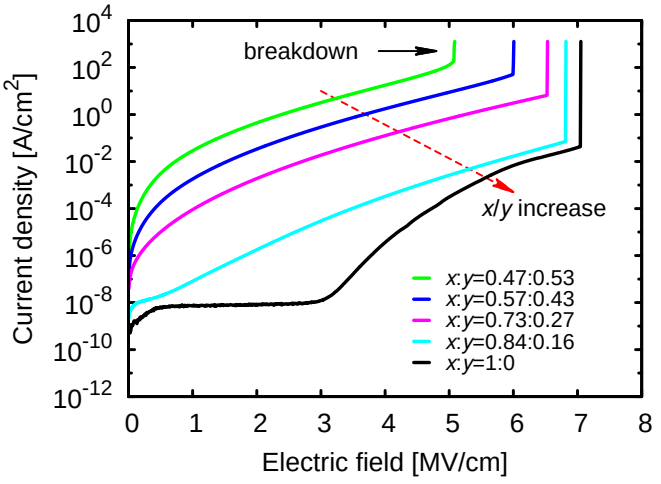


Figure 4.7: Breakdown behavior in current density-electric filed (J-F) characteristics of the Al_xTi_yO ($x/(x+y) = 0.47$-1).

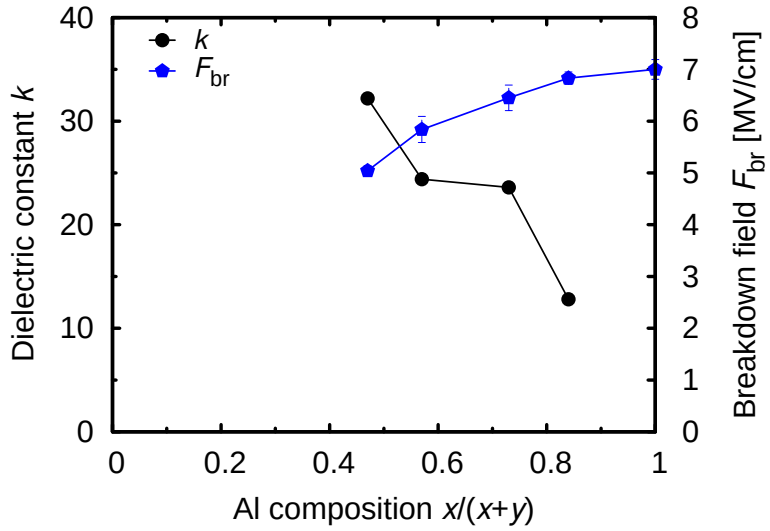


Figure 4.8: Relation between the Al composition and breakdown field $F_{\rm br}$ and dielectric constant k of the Al_xTi_yO. Considering the trade-off between k and $F_{\rm br}$, we decided to apply Al_xTi_yO with $x/(x+y) = 0.73$ to fabrication of AlTiO/AlGaN/GaN MIS-HFETs..

4.1.3 Characterization of AlTiO thin films on AlGaN/GaN heterostructure

A $\sim$ 29-nm-thick Al_xTi_yO ($x/(x+y) = 0.73$) films were deposited on the AlGaN/GaN heterostructure, which was described in sec. 3.1.3, as shown in Fig. 4.9. We characterized the film by XRD measurements using Cu-$K_{\alpha 1}$ wavelength of 1.5406 Å (8047.8 eV) with a rocking curve detector. The global XRD spectra, obtained by 2θ–ω scan, is shown in Fig. 4.10, in which only GaN, AlGaN peaks [99], and sapphire(0001) peaks [100] are observed. There is no peak corresponding to any crystal structures of Al_2O_3, TiO_2, or combination of Al_2O_3 and TiO_2, suggesting an amorphous nature of the ALD-AlTiO films. Likewise, we carried out XPS measurements for the AlTiO/AlGaN/GaN and obtained almost similar results to those for the AlTiO/n-GaAs, which are shown in Fig. 4.4.

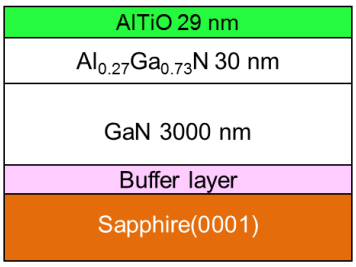


Figure 4.9: Cross section of $\sim$ 29-nm-thick AlTiO film deposited on the $Al_{0.27}Ga_{0.73}N$(30 nm)/GaN(3000 nm) heterostructure obtained by obtained by metal-organic vapor phase epitaxy growth on sapphire(0001).

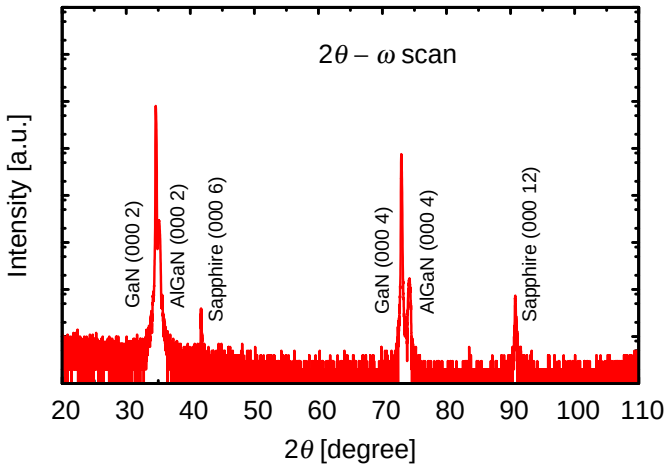


Figure 4.10: XRD measurement result for ∼ 29-nm-thick AlTiO films on the AlGaN/GaN/sapphire(0001) heterostructure.

4.2 Fabrication and characterization of AlTiO/AlGaN/GaN MIS-HFETs

4.2.1 Fabrication of AlTiO/AlGaN/GaN MIS-HFETs (AlTiO MIS-HFETs)

By using the AlGaN/GaN heterostructure with Ohmic electrodes obtained after the device isolation (section 2.3), we fabricated AlTiO/AlGaN/GaN MIS-HFETs (AlTiO MIS-HFETs) as follows. The heterostructure was cleaned by a surface treatment using organic solvents and oxygen plasma ashing for removing organic contaminants, and followed by ammonium-based solution for removing oxides. Subsequently, $\sim$ 29-nm-thick Al_xTi_yO ($x/(x+y) = 0.73$) film was deposited on the AlGaN surface by ALD. In order to investigate effects of annealing, we fabricated two chips; one was annealed at 350 °C for 30 minutes in H_2-mixed (10 %) Ar ambience, and the other not annealed. Finally, Ni/Au gate electrode formation completed the device fabrication. We also fabricated AlGaN/GaN Schottky-HFETs using the same AlGaN/GaN heterostructure for comparison. The MIS- and Schottky-HFETs have a gate length $\sim$ 270 nm, a gate width $\sim$ 50 μm, a gate-source spacing $\sim$ 2 μm, and a gate-drain spacing $\sim$ 3 μm. Schematic cross section of the fabricated AlTiO MIS-HFETs and Schottky-HFETs is depicted in Fig. 4.11.

4.2.2 Effects of annealing on gate leakage of AlTiO MIS-HFETs

We measured characteristics of the devices at room temperature. Figure 4.11 shows two-terminal (drain open) gate-source leakage current I_{GS} as functions of gate-source voltage V_{GS} of the AlTiO MIS-HFETs with annealing and without annealing, and the Schottky-HFETs. The MIS-HFETs with annealing give the lowest I_{GS}, which is $\sim$ 2 and $>$ 4 orders lower than that given by the MIS-HFET without annealing and the Schottky-HFET, respectively. This indicates that the annealing is effective to obtain good insulating properties of the AlTiO films. The decrease in I_{GS} by the annealing can be attributed to the decrease in densities of bulk-oxide defects and/or AlTiO/AlGaN interface states [118]. We concentrate to analyze characteristics of the MIS-HFET with annealing, owing to its extremely low I_{GS}, which leads to low power dissipation at off-states and high drain current on/off ratios.

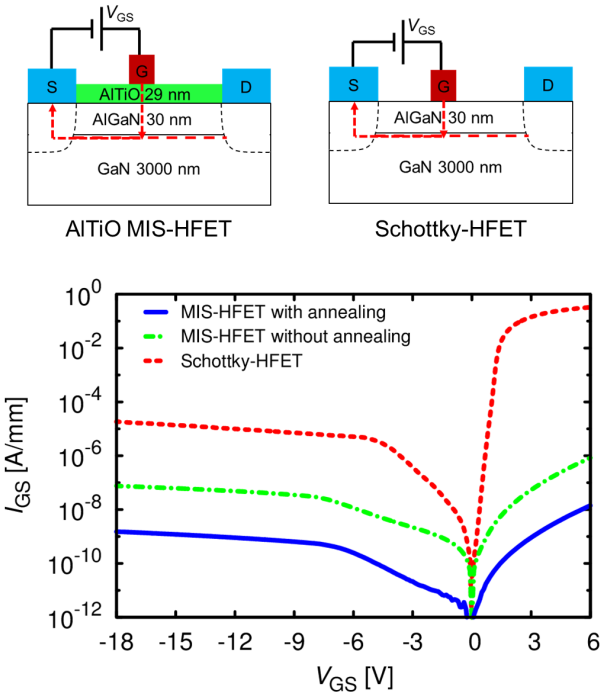


Figure 4.11: Two-terminal (drain-open) gate-source leakage currents I_{GS} as functions of gate-source voltage V_{GS} of the AlTiO MIS-HFET with annealing (blue solid) and without annealing (green dot-dashed), and the Schottky-HFET (red dashed). V_{GS} was swept from 0 V to +6 V, and from 0 V to −18 V.

4.2.3 Advantages of AlTiO in comparison with Al_2O_3

AlTiO, the alloy of TiO_2 and Al_2O_3, possesses intermediate properties of TiO_2 and Al_2O_3. Owing to the small energy gap E_g of TiO_2 ($\sim$ 3 eV) [45], TiO_2/AlGaN/GaN MIS-HFETs exhibited high gate leakage currents [46, 48] and low breakdown fields [83]. The AlTiO MIS-HFETs show extremely low I_{GS}, depicted in Fig. 4.11, indicating that insulating properties of the AlTiO is much better than that of TiO_2. How about device characteristics for the AlTiO MIS-HFETs in comparison with that of Al_2O_3 ones?

In order to compare AlTiO and Al_2O_3, we fabricated $\sim$ 29-nm-thick Al_2O_3 MIS-HFETs simultaneously, using the same AlGaN/GaN heterostructure. Output and transfer characteristics of the devices at room temperature in the air are depicted in Fig. 4.12. In comparison with the Al_2O_3 MIS-HFETs, the AlTiO MIS-HFETs exhibit several advantages, such as a higher maximum I_D, a higher peak and better linearity of g_m, and a shallower threshold voltage V_{th}. However, they exhibit a higher I_G, but still very low. From these results, we concluded that AlTiO is more favorable than Al_2O_3 for applications to AlGaN/GaN MIS-HFETs.

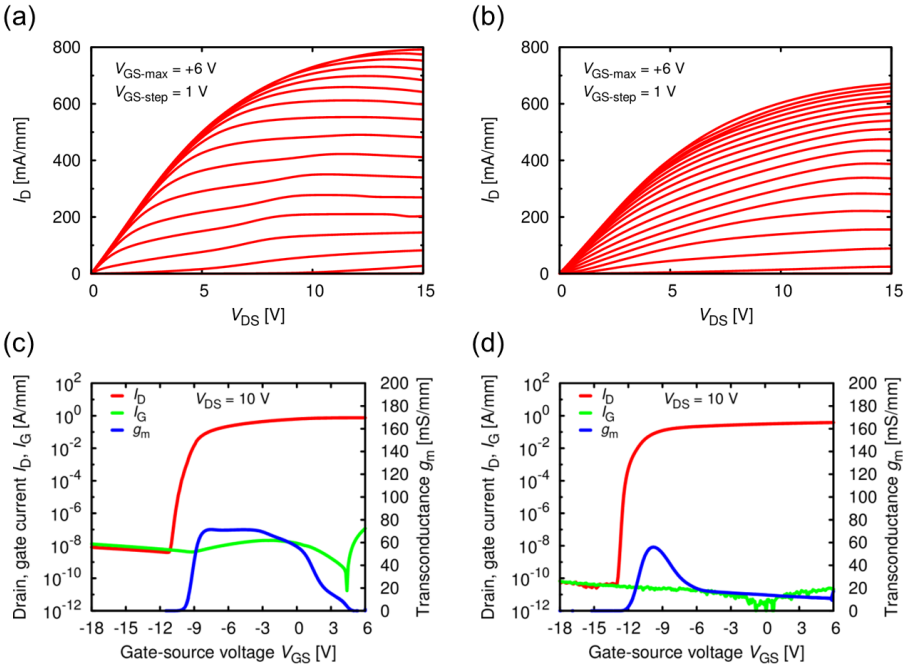
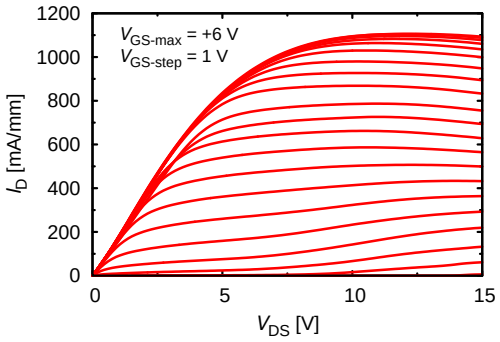


Figure 4.12: Room-temperature characteristics of AlTiO MIS-HFETs: (a) and (c), and Al_2O_3 MIS-HFETs: (b) and (d). In (a) and (b), drain current I_D was obtained with gate-source voltage V_{GS} changing from negative to positive with a step of 1 V and maximum of +6 V. In (c) and (d), I_D, gate current I_G, and transconductance g_m were obtained under V_{GS} sweep from -18 V $\rightarrow$ +6 V at drain-source voltage V_{DS} of 10 V.

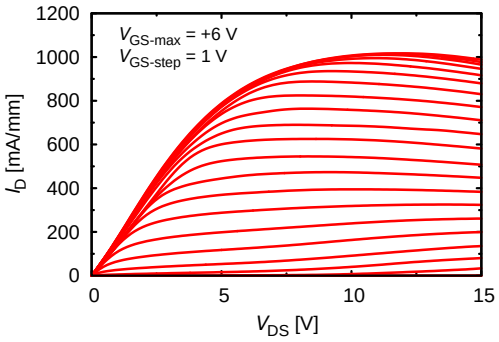
4.2.4 Temperature dependence of output and transfer characteristics of AlTiO MIS-HFETs

In order to investigate temperature-dependent characteristics for AlTiO MIS-HFETs, we carried out measurements in the vacuum, using TTP4 probe station of Lake Shore Cryotronics, shown in Fig. 3.17. Temperature T, controlled by heater and liquid N_2, was varied from 150 K to 402 K. Characteristics of the devices at room temperature in the air and vacuum are similar, in contrast to BN MIS-HFETs. This suggests that the measurement ambience has no effect on the device characteristics.

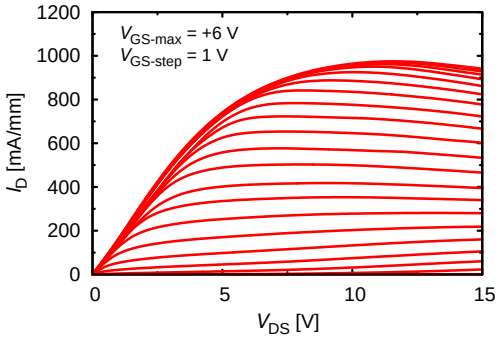
Figure 4.13 shows output characteristics the MIS-HFETs, obtained under gate-source voltage V_{GS} changing from -14 V to +6 V with a step of 1 V, exhibiting high maximum drain currents I_D. Weak negative conductances are observed for high I_D and high V_{DS}, indicating decrease in channel-electron velocity, related to increase in device temperature due to the self-heating effect at high power consumption [51, 55, 108]. This suggests a low thermal conductivity of AlTiO because of alloy effects [119].



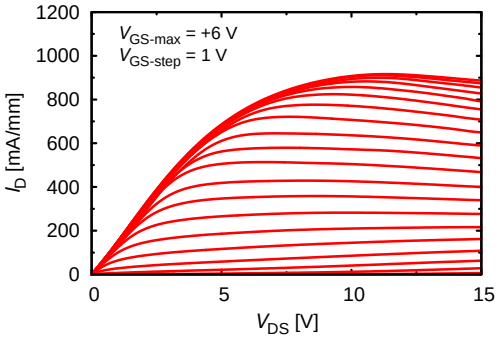
(a) 150 K



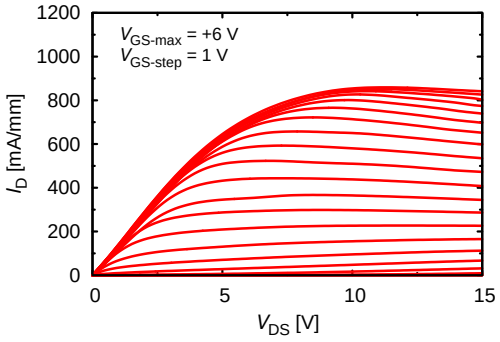
(b) 182 K



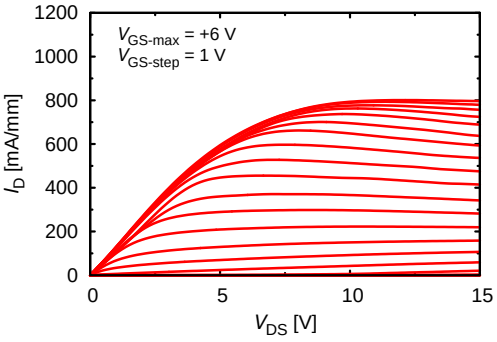
(c) 200 K



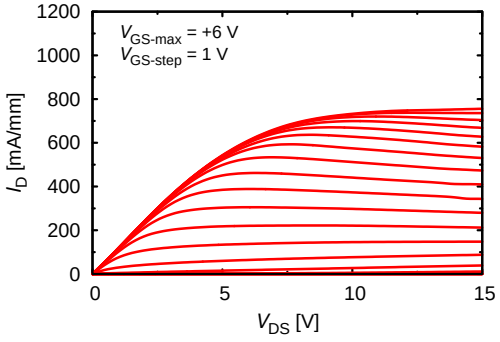
(d) 225 K



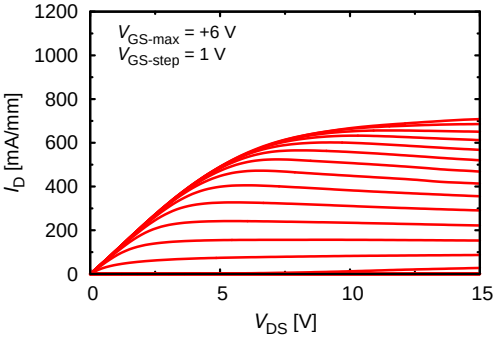
(e) 250 K



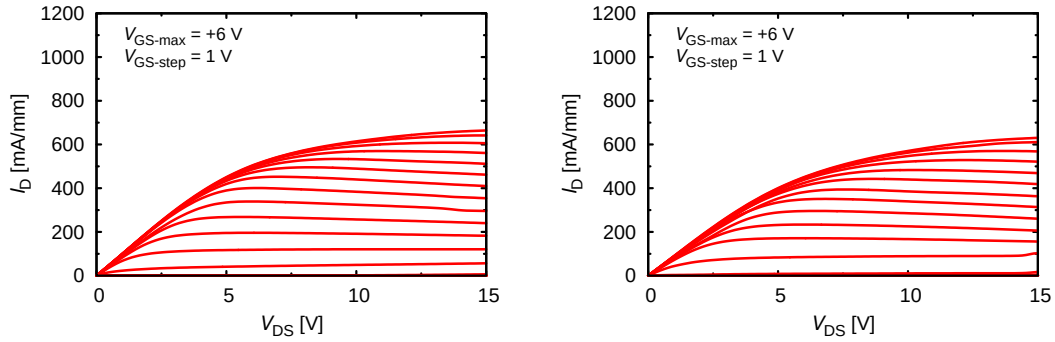
(f) 275 K



(g) 300 K



(h) 330 K



(i) 365 K (j) 402 K

Figure 4.13: Output characteristics of the AlTiO/AlGaN/GaN MIS-HFETs at temperature from 150 K to 402 K, obtained under gate-source voltage V_{GS} changing from negative to positive with a step of 1 V and a maximum of +6 V.

With regard to elucidate temperature-dependent channel conduction, we analyzed drain currents I_D at $V_{GS} = 0$ V, as depicted in Fig. 4.14(a). From which, drain currents I_D in linear (low-voltage) and saturation (high-voltage) regions were plotted as functions of temperature T, as shown in Fig. 4.14(b). With increase in T, I_D in linear and saturation regions decrease.

The on-resistance R_{on}, which is proportional to $1/I_D$ in the linear region, increases ~ 2 times from 150 K to 402 K. This is compared with transmission line model (TLM) measurements and Hall-effect measurements. Figure 4.15(a) shows the temperature dependence of normalized contact resistance R_c and sheet resistance ρ_s obtained by TLM measurements, where R_c is almost constant and ρ_s increases ~ 4 times from 150 K to 402 K. The temperature dependence of $\rho_s = 1/qn_s\mu$, where q is the electron charge, is in agreement with the Hall-effect measurement results, where n_s is almost constant and $1/\mu$ increases ~ 4 times from 150 K to 402 K, as shown in Fig. 4.15(b). The temperature dependence of μ is similar to Monte-Carlo simulation result [109] and experimental results [110]. As shown in Fig. 4.15(c), we find that the sum of $2R_c$ and $\rho_s L_{SD}$, where L_{SD} is source-drain spacing, increases ~ 2 times from 150 K to 402 K, which is consistent with R_{on} of the MIS-HFETs. Therefore, we conclude that the decrease in I_D in the linear region is mainly due to the decrease in μ.

On the other hand, I_D in the saturation region is proportional to the average electron velocity v_{ave}, which should be in-between low-field and high-field velocities. Figure 4.16 shows the relative temperature-dependent v_{ave} obtained by I_D in the saturation region, in comparison with the low- and high-field velocities obtained by Monte-Carlo simulations (v_{LMC} and v_{HMC}) [109]. In fact, the temperature dependence of v_{ave} is in-between those of v_{LMC} and v_{HMC}, where v_{LMC} shows a stronger dependence and v_{HMC} shows a weaker dependence, as indicated by experiments [51, 111]. Temperature-dependent channel conduction of the AlTiO MIS-HFETs is similar to that of the BN MIS-HFETs.

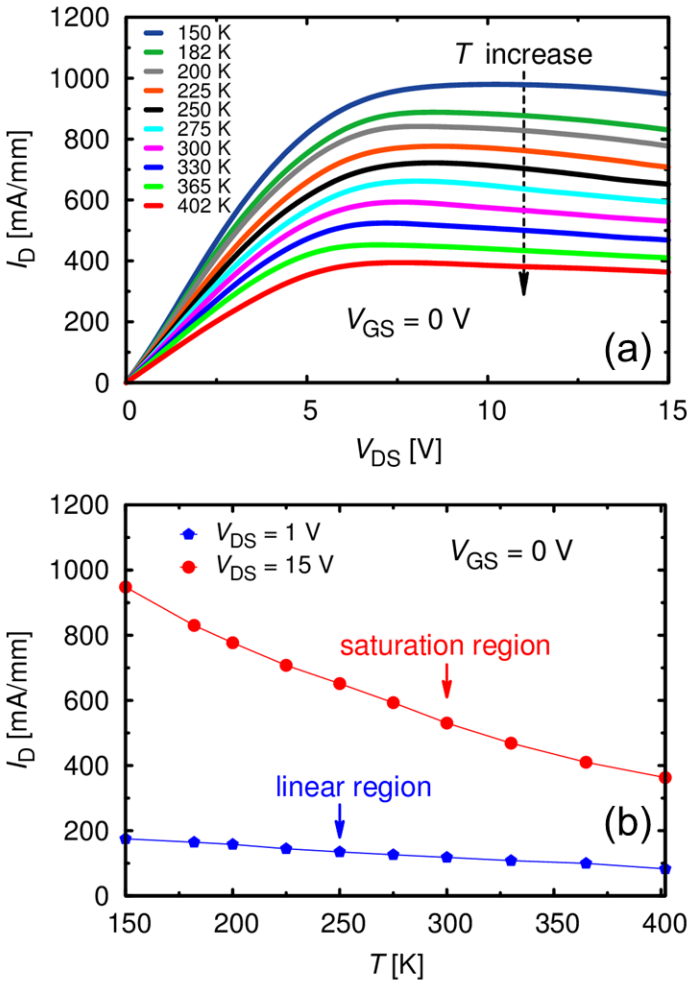


Figure 4.14: (a) Temperature-dependent drain currents I_D at gate-source voltage $V_{GS} = 0$ V. (b) Temperature dependence of I_D in linear (low-voltage) region ($V_{DS} = 1$ V) and saturation (high-voltage) region ($V_{DS} = 15$ V). With increase in temperature T, I_D in the both regions decreases.

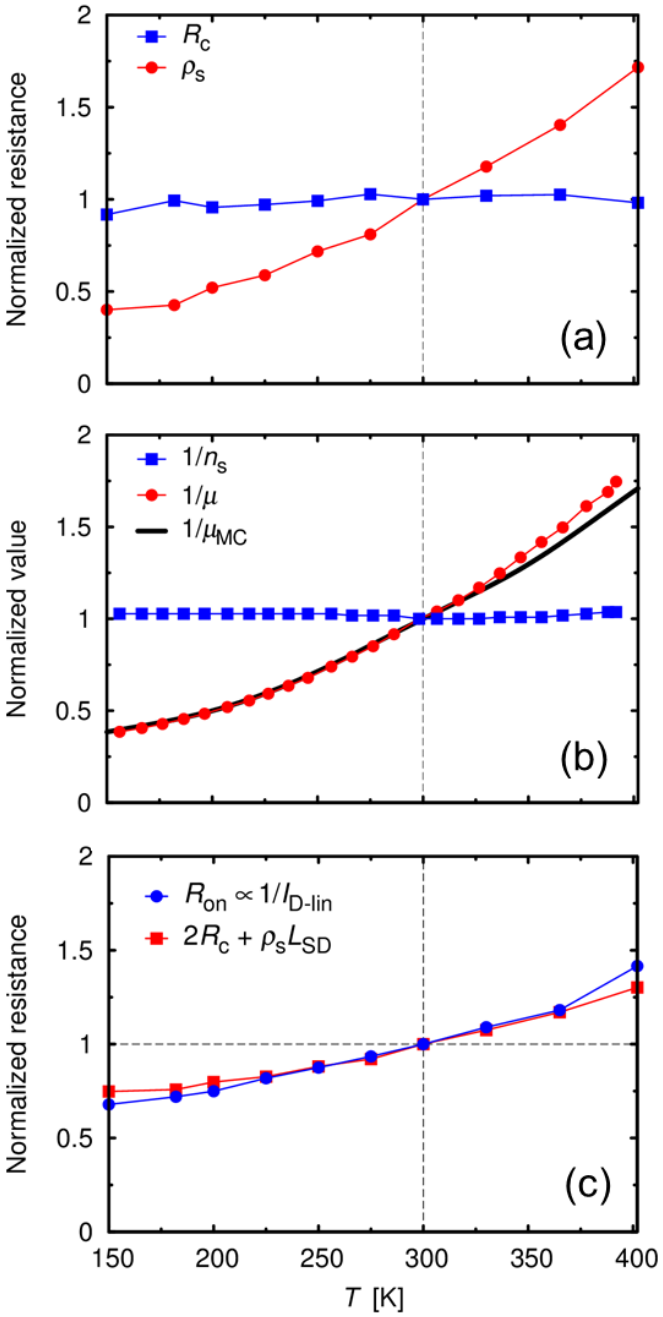


Figure 4.15: (a) Temperature dependence of the normalized contact resistance R_c and the normalized sheet resistance ρ_s obtained by TLM measurements. (b) Temperature dependence of the normalized electron mobility inverse $1/\mu$ and the sheet electron concentration inverse $1/n_s$ obtained by Hall-effect measurements. The mobility μ is compared with the Monte-Carlo-simulated μ_{MC}. (c) The consistency of the sum of $2R_c$ and $\rho_s L_{SD}$ (L_{SD}: source-drain spacing) with the on-resistance R_{on} obtained by drain current I_D in the linear region.

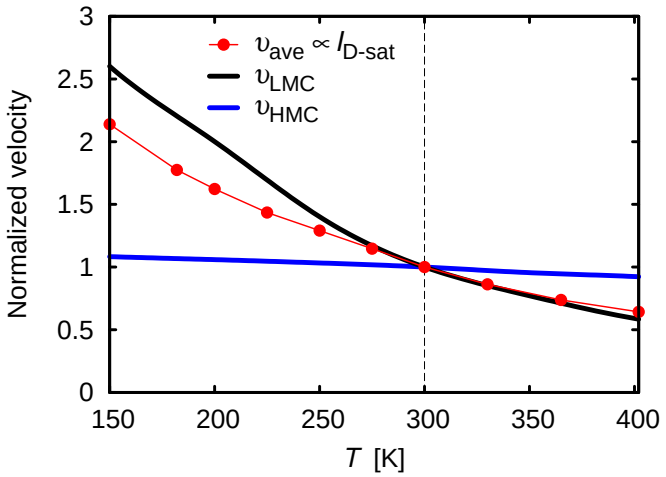
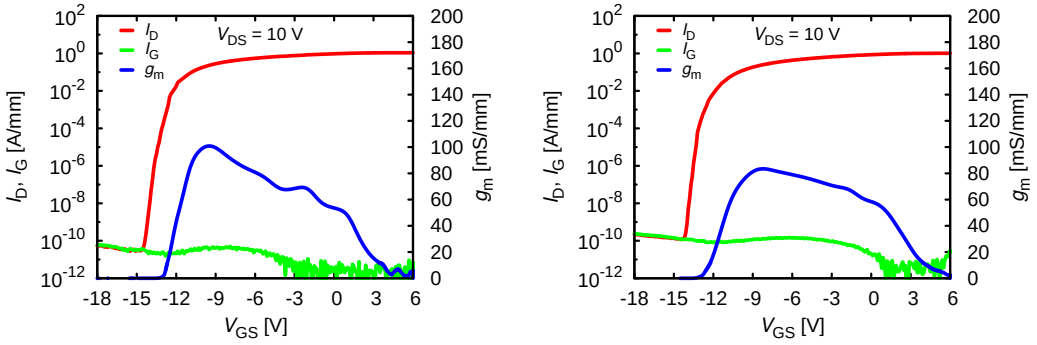
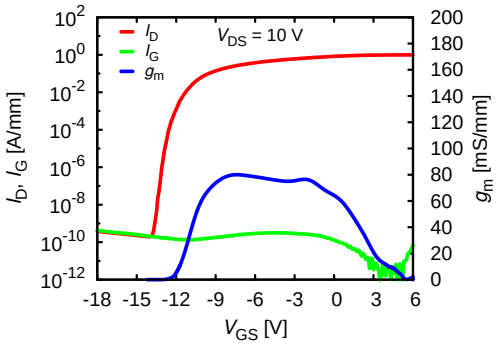


Figure 4.16: Relative temperature-dependent average velocity v_{ave}, obtained by drain current I_{D} in the saturation region, in comparison with the low- and high-field velocities obtained by Monte-Carlo simulations (v_{LMC} and v_{HMC}).

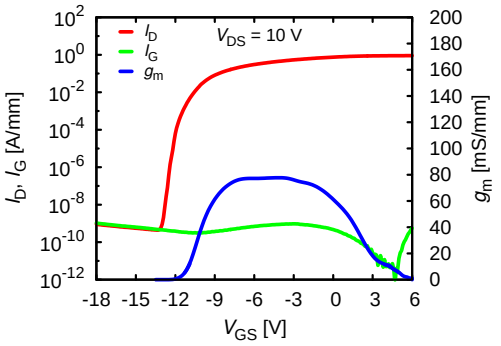
Transfer characteristics of the MIS-HFETs at temperature T from 150 K to 402 K are shown in Fig. 4.17, where drain current I_{D}, gate current I_{G}, and transconductance g_{m} were obtained under V_{GS} sweep of -18 V $\rightarrow$ $+6$ V at $V_{\mathrm{DS}} = 10$ V. We obtain high drain current on/off ratios and good linearity of transconductance g_{m}, indicating a good gate controllability, suggesting low density of AlTiO/AlGaN interface states. In addition, we observe increasing gate leakage with increase in temperature and a bump in gate current I_{G} at high I_{D}, suggesting increase in device temperature due to the self-heating effect at high-power consumption.



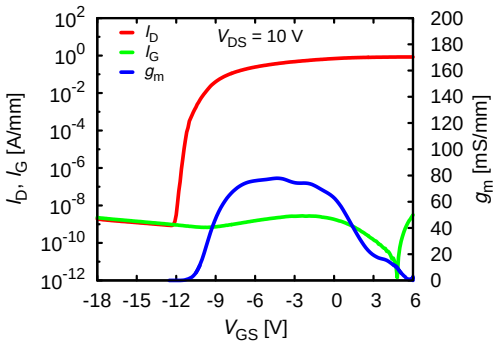
(a) 150 K (b) 182 K



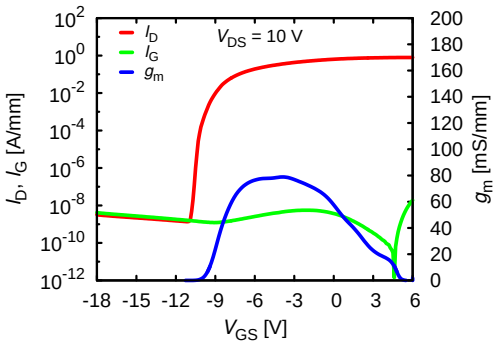
(c) 200 K



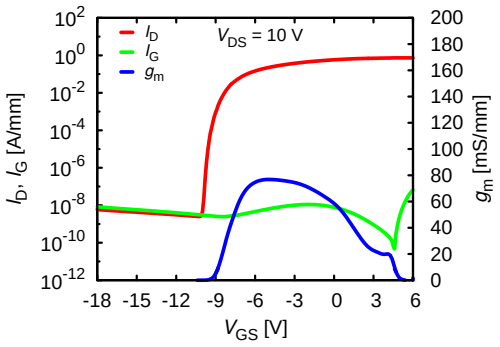
(d) 225 K



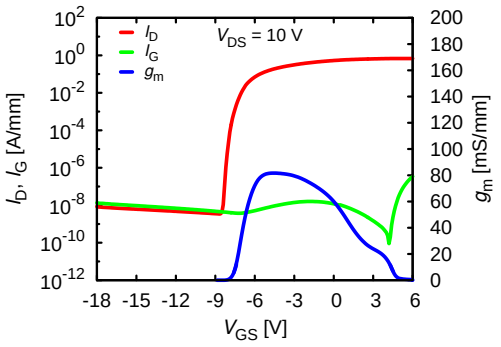
(e) 250 K



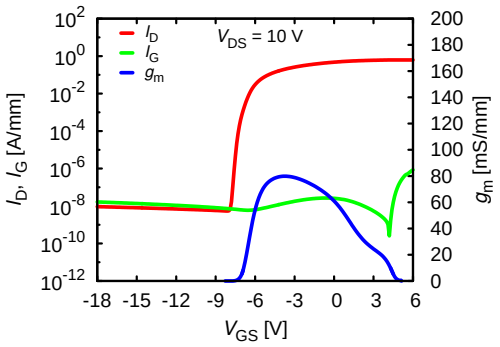
(f) 275 K



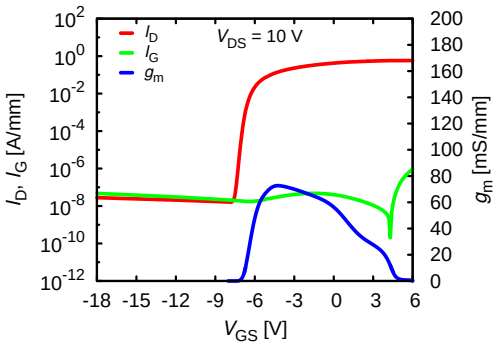
(g) 300 K



(h) 330 K



(i) 365 K



(j) 402 K

Figure 4.17: Transfer characteristics of the AlTiO/AlGaN/GaN MIS-HFETs at temperature from 150 K to 402 K, where drain current I_D, gate current I_G, and transconductance g_m were obtained under gate-source voltage V_{GS} sweep of -18 V $\rightarrow$ $+6$ V at drain-source voltage V_{DS} of 10 V.

In order to confirm that, we check V_{DS} dependence of the bumps, including the drain open case, as shown in Fig. 4.18. As a result, as V_{DS} decreases, I_D decreases, leading to the lower power consumptions. Therefore, the self-heating is weaker and the bump is smaller. In contract to the high V_{DS} cases, at drain open, there is no power consumption, hence, no self-heating, leading to no bump. Therefore, we conclude that the strong self-heating at high-power consumption is the origin of the bumps.

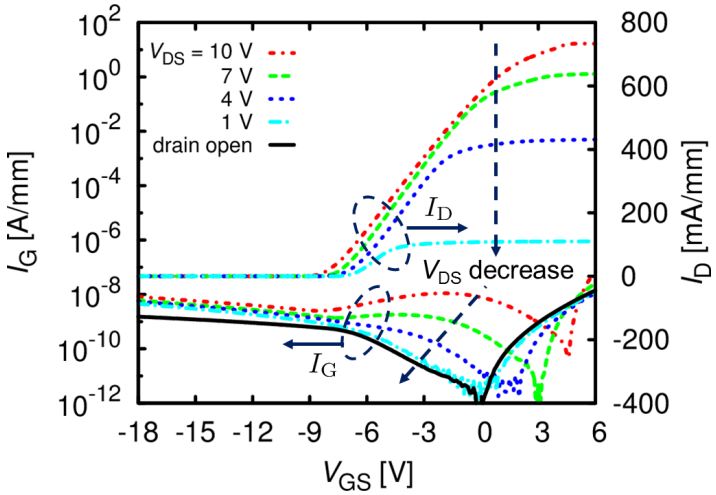


Figure 4.18: Drain-source voltage V_{DS} dependence of the bumps at 300 K, including the drain open case. The higher V_{DS}, the larger bump is.

We make a comparison between the AlTiO and BN MIS-HFETs [120], about the bumps. At room temperature, for similar power consumption, only AlTiO MIS-HFETs exhibit a bump, but no bump for BN MIS-HFETs, as shown in Fig. 4.19(a). This can be attributed to lower thermal conductivity κ of AlTiO than that of BN. In general, alloy materials have very low κ due to random effects [119]. On the other hand, at 150 K, we observe similar bumps, as shown in Fig. 4.19(b), which may be related to temperature dependence of κ of AlTiO and BN.

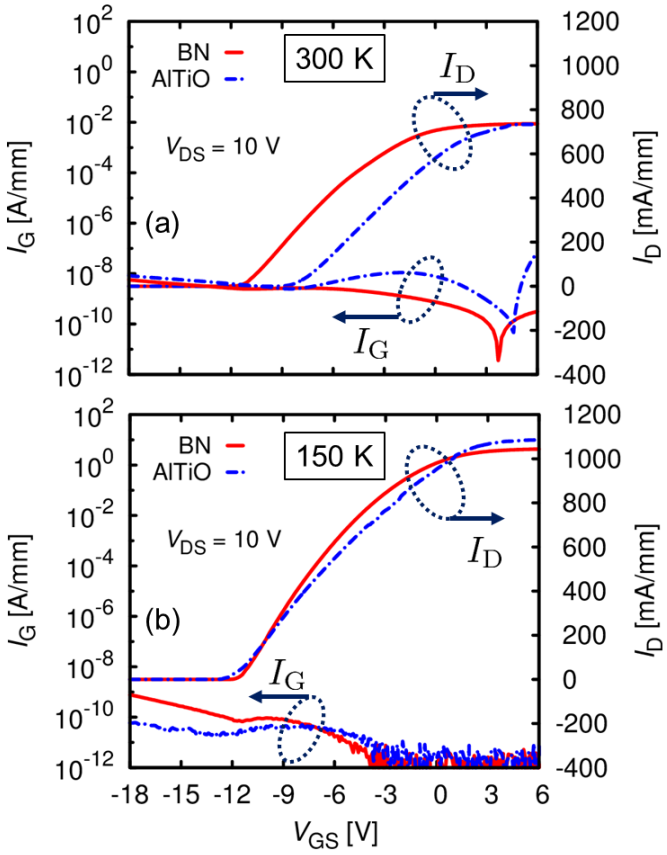


Figure 4.19: Comparison between the AlTiO and BN MIS-HFETs, about the bumps at (a) 300 K and (b) 150 K.

4.2.5 Temperature dependence of gate leakage of AlTiO MIS-HFETs

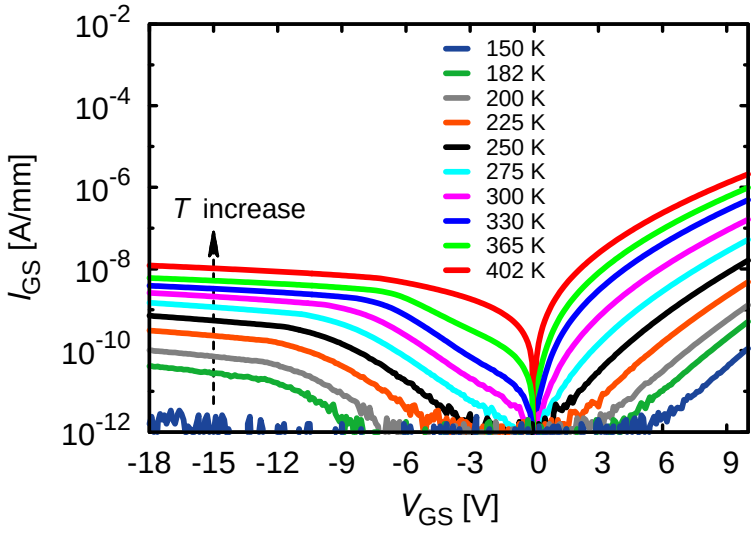


Figure 4.20: Temperature-dependent two-terminal (drain open) gate-source leakage current I_{GS} as functions of gate-source voltage V_{GS} of the AlTiO/AlGaN/GaN MIS-HFETs. V_{GS} was swept from 0 V to +6 V, and from 0 V to −18 V. With increase in temperature T, I_{GS} increases.

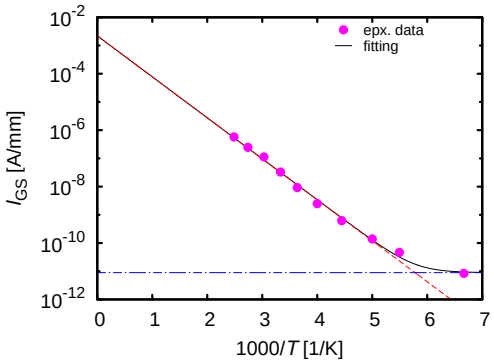
We investigated temperature-dependent two-terminal (drain-open) gate-source leakage currents I_{GS} shown in Fig. 4.20, in which I_{GS} increases (decreases) with the increase (decrease) in temperature. This confirms the bump in the 3-terminal cases, attributed to high temperature in the device channel due to the self-heating. Moreover, the dependence of I_{GS} to temperature suggests that it is related to thermal processes. As shown in Fig. 4.21, the experimental data at large forward biases are well-fitted by Eq. 3.5. Fitting results are shown in Fig. 4.22. We observe temperature-independent term $I_1(V_{GS})$ exponentially increases with increase in V_{GS}, shown in Fig. 4.22(a), suggesting tunneling current through AlGaN and AlTiO barriers at low temperatures [114]. In addition, we find that $I_0(V_{GS})$ is a linear function of V_{GS}, or proportional to $(V_{GS} - V_0)$ with $V_0 \simeq 2.9$ V, as shown in Fig. 4.22(b); and $E_a(V_{GS})$ is a linear function of $\sqrt{V_{GS} - V_0}$, as shown in Fig. 4.22(c). The behaviors can be explained by the PF conduction, described by [112, 113]

$$I_{PF}(F,T) \propto F \exp\left[-\frac{1}{k_B T}\left(\phi - \sqrt{\frac{q^3 F}{\pi \varepsilon_0 k}}\right)\right], \tag{4.1}$$

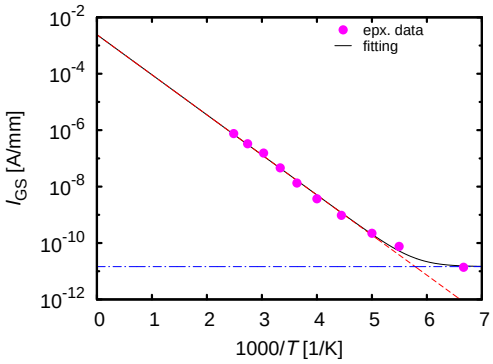
which is obtained in appendix A, with electron charge q, vacuum dielectric constant ε_0, insulator relative dielectric constant k, trap depth ϕ, electric field in AlTiO F, which is given by

$$F \simeq \alpha(V_{GS} - V_0) \tag{4.2}$$

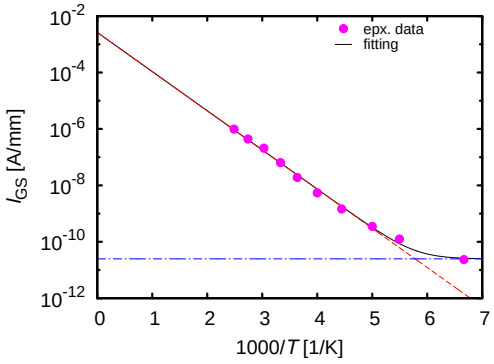
with a proportional factor α.



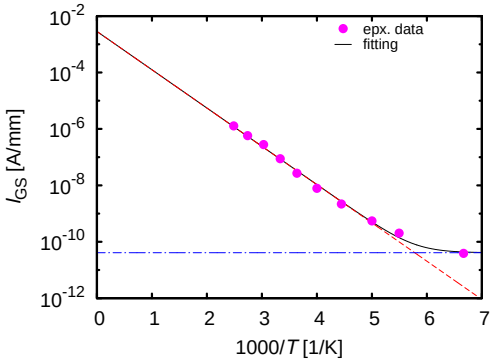
(a) V_{GS} = +7.5 V



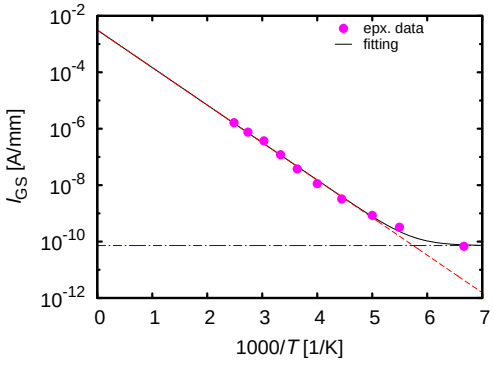
(b) V_{GS} = +8.0 V



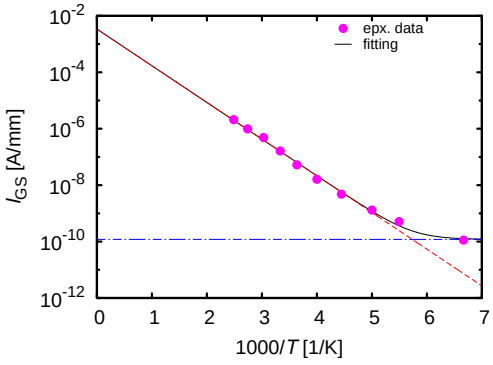
(c) V_{GS} = +8.5 V



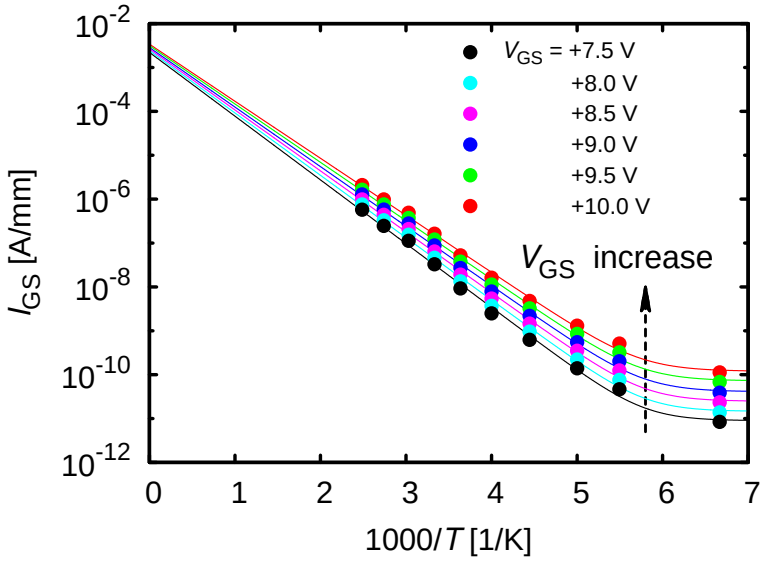
(d) V_{GS} = +9.0 V



(e) V_{GS} = +9.5 V



(f) V_{GS} = +10.0 V



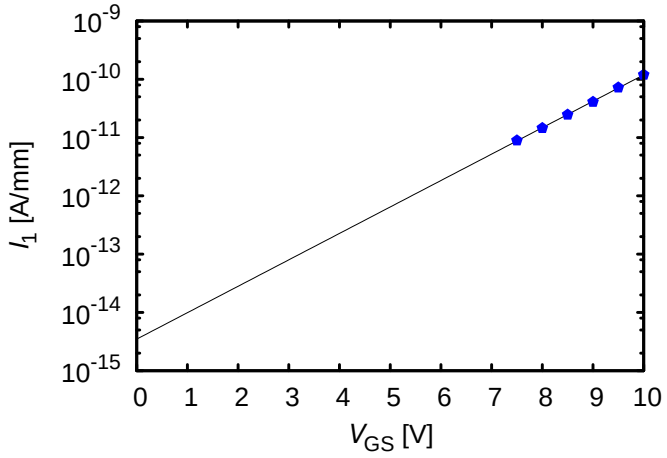
(g) Summary

Figure 4.21: (a) - (f) Two-terminal (drain open) gate-source leakage current I_{GS} at several large forward biases are well fitted by Eq. 3.5, in which red dashed line is temperature-dependent and blue dot-dashed line is temperature-independent. (g) Summary of the fitting for the large forward biases.

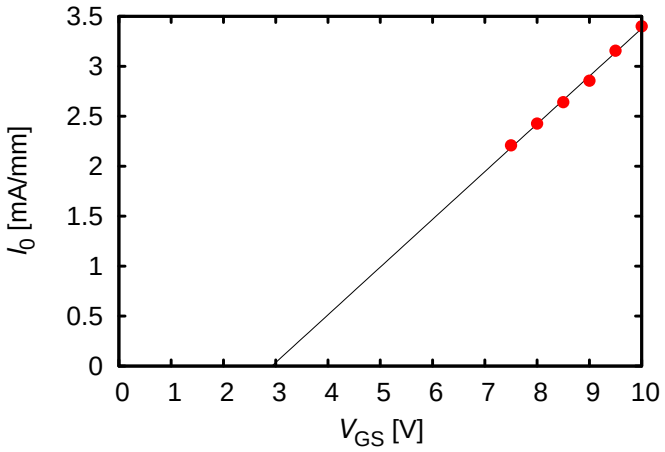
By compare Eq. 3.5 and Eq. 4.1, we obtain equation for activation energy E_a, given by

$$E_a(V_{GS}) = \phi - \sqrt{\frac{q^3\alpha(V_{GS} - V_0)}{\pi\varepsilon_0 k}}. \tag{4.3}$$

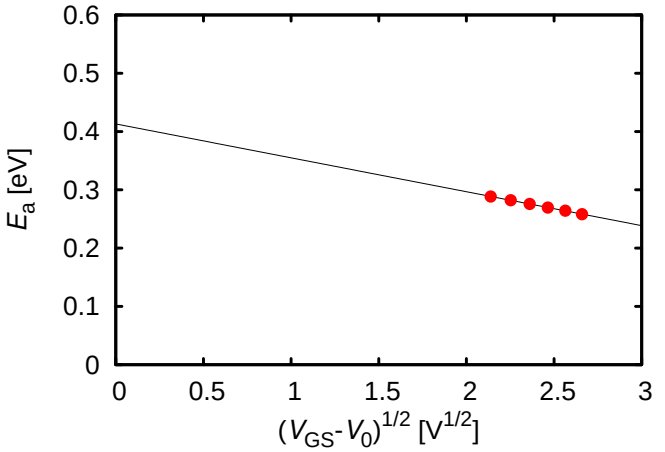
Using $k = k_{AlTiO} \sim 24$ obtained by the PF analysis [89], fitting of E_a gives $\phi \simeq 0.41$ eV and $\alpha \sim 1.4\times10^5$ cm^{-1}. Figure 4.23(a) shows the conduction band diagram of Ni/AlTiO/AlGaN/GaN, which includes temperature-independent tunneling current and temperature-dependent current exhibited PF mechanism with the trap depth ϕ.



(a) I_1 as an exponential function of V_{GS}.



(b) Prefactor I_0 as a linear function of gate-source voltage V_{GS}, or proportional to $(V_{\mathrm{GS}} - V_0)$ with $V_0 \simeq 2.9$ V.



(c) Activation energy E_{a} as a linear function of $\sqrt{V_{\mathrm{GS}} - V_0}$.

Figure 4.22: The fitting results at large forward biases.

We can estimate AlTiO/AlGaN interface state density D_{i} by considering an equivalent circuit for DC limit, as shown in Fig. 4.23(b) [115], from which, the gate voltage change is divided into AlTiO $\Delta V_{\mathrm{AlTiO}}$ and AlGaN $\Delta V_{\mathrm{AlGaN}}$ as

$$\Delta V_{\mathrm{GS}} = \Delta V_{\mathrm{AlTiO}} + \Delta V_{\mathrm{AlGaN}}. \tag{4.4}$$

The voltage change in AlTiO, obtained from Eq. 4.2, is

$$\Delta V_{\mathrm{AlTiO}} = d_{\mathrm{AlTiO}} \Delta F \simeq d_{\mathrm{AlTiO}} \alpha \Delta V_{\mathrm{GS}},$$

with the AlTiO thickness $d_{\mathrm{AlTiO}} \sim 29$ nm. Therefore, we find a voltage ratio

$$\frac{\Delta V_{\mathrm{AlTiO}}}{\Delta V_{\mathrm{GS}}} \simeq \alpha d_{\mathrm{AlTiO}} \sim 1.4 \times 10^5 \ \mathrm{cm}^{-1} \times 29 \ \mathrm{nm} \sim 0.4. \tag{4.5}$$

From the equivalent circuit, we can obtain charge distribution in AlTiO and AlGaN and

interface, given by

$$\Delta V_{\mathrm{AlTiO}} C_{\mathrm{AlTiO}} = \Delta V_{\mathrm{AlGaN}} (C_{\mathrm{AlGaN}} + C\mathrm{i}) = \Delta V_{\mathrm{AlGaN}} (C_{\mathrm{AlGaN}} + q^2 D\mathrm{i})$$

or

$$\Delta V_{\mathrm{AlGaN}} = \Delta V_{\mathrm{AlTiO}} \frac{C_{\mathrm{AlTiO}}}{C_{\mathrm{AlGaN}} + q^2 D_{\mathrm{i}}}, \tag{4.6}$$

with AlTiO capacitance C_{AlTiO}, AlGaN capacitance C_{AlGaN} and AlTiO/AlGaN interface state capacitance C_{i} obtained from D_{i}. Substitute Eq. 4.6 into Eq. 4.4 and compare with Eq. 4.5, we derive the voltage ratio

$$\frac{\Delta V_{\mathrm{AlTiO}}}{\Delta V_{\mathrm{GS}}} = \frac{C_{\mathrm{AlGaN}} + q^2 D_{\mathrm{i}}}{C_{\mathrm{AlTiO}} + C_{\mathrm{AlGaN}} + q^2 D_{\mathrm{i}}} \sim 0.4. \tag{4.7}$$

From this, by using values of $C_{\mathrm{AlTiO}} = k_{\mathrm{AlTiO}} \varepsilon_0 / d_{\mathrm{AlTiO}} \sim 24 \times 8.86 \times 10^{-14}$ C/Vcm $\times$ 1/(29 nm) $\sim$ 730 nFcm^{-2} and $C_{\mathrm{AlGaN}} = k_{\mathrm{AlGaN}} \varepsilon_0 / d_{\mathrm{AlGaN}} \sim 9 \times 8.86 \times 10^{-14}$ C/Vcm $\times$ 1/(30 nm) $\sim$ 270 nFcm^{-2}, where k_{AlGaN} and d_{AlGaN} are dielectric constant and thickness of AlGaN, respectively, we obtain the AlTiO/AlGaN interface state density $D_{\mathrm{i}} \sim 2 \times 10^{12}$ cm^{-2}eV^{-1}. The low D_{i} of the AlTiO/AlGaN interface leads to the good gate controllability.

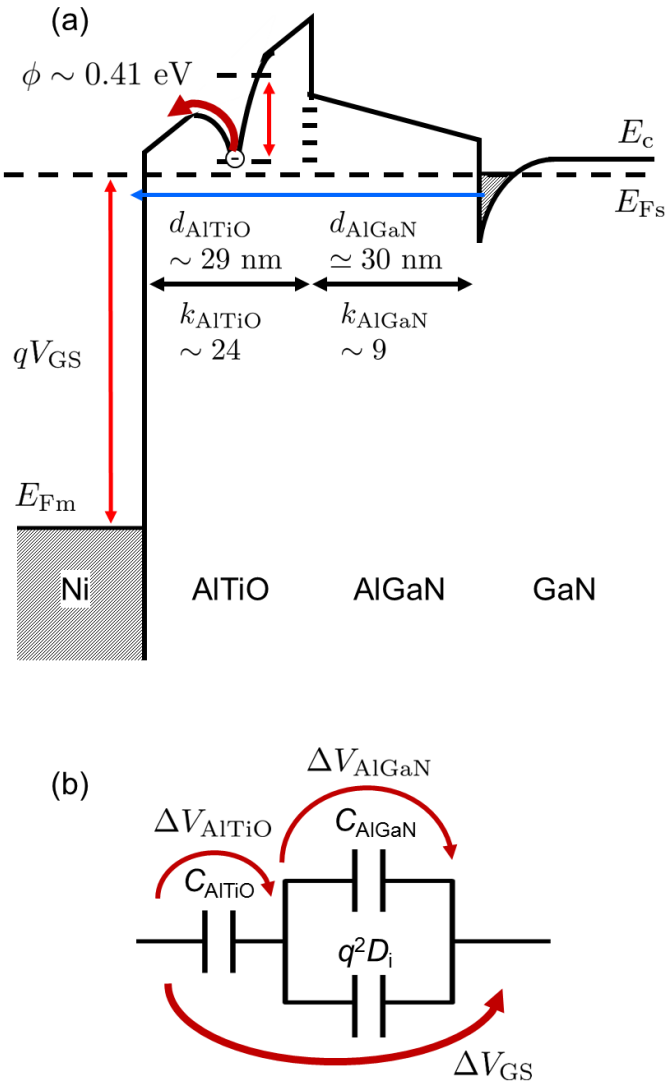


Figure 4.23: (a) Conduction band diagram of Ni/AlTiO/AlGaN/GaN showing temperature-independent tunneling current (blue solid) and Pool-Frenkel current (red curve) with a trap depth $\phi \sim 0.41$ eV. (b) The equivalent circuit for the DC limit [E. H. Nicollian and J. R. Brews] with AlTiO capacitance C_{AlTiO}, AlGaN capacitance C_{AlGaN}, and AlTiO/AlGaN interface state density D_i, including applied voltage V_{GS}, voltage V_{AlTiO} dropped on AlTiO, and V_{AlGaN} dropped on AlGaN.

We examine the effect of the annealing by fitting gate leakages for the devices with and without annealing to PF mechanism, described by

$$I_{\mathrm{GS}}(V_{\mathrm{GS}}, T) = A(V_{\mathrm{GS}} - V_0) \exp\left\{ -\frac{1}{k_{\mathrm{B}}T} \left[\phi - \sqrt{\frac{q^3 \alpha (V_{\mathrm{GS}} - V_0)}{\pi \varepsilon_0 k_{\mathrm{AlTiO}}}} \right] \right\}. \tag{4.8}$$

where A is a prefactor. We obtained good fitting as shown in Fig. 4.24. Assuming similar k_{AlTiO} and ϕ, we find that the annealing leads to similar α, suggesting similar interface state density. In addition, ~ 2 orders smaller A, which is proportional to the bulk trap density in AlTiO, suggesting decrease of bulk trap density with the annealing.

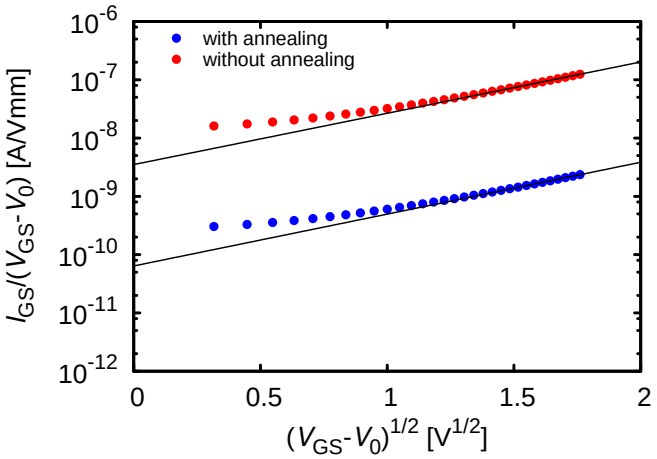


Figure 4.24: Poole-Frenkel fitting for AlTiO MIS-HFETs with and without annealing.

4.3 Summary of chapter 4

Al_xTi_yO (alloy of the extremely-high-k TiO_2 and the wide energy gap Al_2O_3) film, which has intermediate properties between TiO_2 and Al_2O_3, is important to balance k and E_g. In this chapter, we characterized physical properties of Al_xTi_yO thin films obtained by atomic layer deposition, for several Al compositions $x/(x+y)$. We observe increasing E_g and breakdown field F_{br}, and decreasing k with increase in the Al composition. Considering the trade-off between k and F_{br}, we applied Al_xTi_yO with $x/(x+y) = 0.73$ to fabricate AlTiO/AlGaN/GaN MIS-HFETs (AlTiO MIS-HFETs).

The AlTiO MIS-HFETs annealed in H_2-mixed Ar ambience just after AlTiO deposition, exhibit very low gate leakage, which is ~ 2 orders lower than that given by AlTiO MIS-HFETs without annealing and > 4 orders lower than that given by AlGaN/GaN Schottky-HFETs. suggesting that the annealing is effective to obtain good insulating properties of AlTiO. In comparison with Al_2O_3/AlGaN/GaN MIS-HFETs, the AlTiO MIS-HFETs exhibit higher maximum I_D, higher peak and better linearity of transconductance, shallower threshold voltage, and higher gate leakage (but still very low), suggesting that AlTiO is more favorable than Al_2O_3 for applications to AlGaN/GaN MIS-HFETs.

We investigated temperature-dependent channel conduction of the AlTiO MIS-HFETs, where I_D decreases with increase in temperature. In the linear region, the decrease in I_D is mainly due to decrease in the electron mobility, while the contact resistance and the sheet electron concentration are almost constant. In the saturation region, the decreased I_D is proportional to the average electron velocity, whose temperature dependence is in-between those of the low- and high-field velocities. Temperature-dependent channel conduction of the AlTiO MIS-HFETs is similar to that of the BN MIS-HFETs. Moreover, we observe bumps in gate current for high drain-source voltages and high I_D, indicating increase in channel temperature due to the self-heating effect at high power consumption. This suggests low thermal conductivity of AlTiO due to random effects in alloy materials. In addition, we elucidated the temperature-dependent gate leakage, attributed to a mechanism with two terms. One is temperature-independent tunneling, dominant at low temperatures. The other exhibits Poole-Frenkel mechanism, dominant at high temperatures, from which we estimated AlTiO/AlGaN interface state density, which is $\sim 2 \times 10^{12}$ $cm^{-2}eV^{-1}$. Low-density AlTiO/AlGaN interface states lead to the strong gate controllability for the AlTiO MIS-HFETs.

Chapter 5

Conclusions and future works

5.1 Conclusions

GaN-based metal-insulator-semiconductor heterojunction field-effect transistor (MIS-HFETs) have been investigated owing to the merits of gate leakage reduction and passivation to suppress the current collapse. Gate insulators, such as Al_2O_3, HfO_2, TiO_2, or AlN, have been studied. Further developments of the MIS-HFETs using novel gate insulators suitable according to applications are important. A desired gate insulator should have:

- wide energy gap E_g and high breakdown field F_{br} for high voltage operation,
- high dielectric constant k for high transconductance, and
- high thermal conductivity κ for good heat release suitable for high power operation

In particular, boron nitride (BN) and aluminum titanium oxide (AlTiO: an alloy of TiO_2 and Al_2O_3) are promising candidates owing to their advantageous properties.

In this work, we characterized physical properties of amorphous BN thin films obtained by RF magnetron sputtering, which have $E_g \sim 5.7$ eV, $F_{br} \sim 5.5$ MV/cm, and $k \sim 7$. We deposited BN films on an $Al_{0.27}Ga_{0.73}N$ (30 nm)/GaN (3000 nm) heterostructure obtained by metal-organic vapor phase epitaxy growth on sapphire(0001) and fabricated BN/AlGaN/GaN MIS-HFETs (BN MIS-HFETs). The BN MIS-HFETs exhibit very low gate leakage, which is ~ 9 orders at forward biases and ~ 4 orders at reverse biases lower than that of AlGaN/GaN Schottky-HFETs, indicating good insulating properties of BN. We measured characteristics of the MIS-HFETs in the air, vacuum, and N_2 gas of 1 atm. We obtain almost similar gate leakage current in the air, vacuum, and N_2 gas, indicating that the insulating properties of BN is not influenced by the ambiences. However, we observe that threshold voltage V_{th} of the MIS-HFETs in the air is shallower than that in the vacuum and N_2 gas. In addition, V_{th} of BN/AlGaN/GaN MIS-capacitors is similar in the ambiences, indicating the V_{th} shift of the MIS-HFETs is related to the influence of H_2O or/and O_2 in the air surrounding gate areas. In order to deeply understand the insight, we carried out temperature-dependent measurements and analyzed electron transport properties for the BN MIS-HFETs. We obtain high maximum drain current I_D and no negative conductance, suggesting good thermal release

properties owing to the excellent κ of BN. We elucidated temperature-dependent channel conduction, where I_{D} decreases with increase in temperature. In the linear region, the decrease in I_{D} is attributed to decrease in the electron mobility, while the sheet electron concentration is constant. In the saturation region, the decreased I_{D} is proportional to the average electron velocity, whose temperature dependence is in-between those of the low- and high-field velocities. Furthermore, we elucidated the temperature-dependent gate leakage, attributed to a mechanism with temperature-independent tunneling, dominant at low temperatures, and temperature-enhanced tunneling, dominant at high temperatures, from which we estimated the BN/AlGaN interface state density, which is $\gg 10^{12}$ cm^{-2}eV^{-1}. High-density BN/AlGaN interface states lead to the weak gate controllability for the BN MIS-HFETs.

We also characterized physical properties of $\mathrm{Al}_x\mathrm{Ti}_y\mathrm{O}$ thin films obtained by atomic layer deposition, for several Al compositions $x/(x+y)$. We observe increasing E_{g} and F_{br}, and decreasing k with increase in the Al composition. Considering the trade-off between k and F_{br}, we applied $\mathrm{Al}_x\mathrm{Ti}_y\mathrm{O}$ with $x/(x+y) = 0.73$, where $E_{\mathrm{g}} \sim 6$ eV, $F_{\mathrm{br}} \sim 6.5$ MV/cm, and $k \sim 24$, to fabrication of AlTiO/AlGaN/GaN MIS-HFETs (AlTiO MIS-HFETs). The AlTiO MIS-HFETs annealed in H_2-mixed Ar ambience just after AlTiO deposition, exhibit very low gate leakage, which is ~ 2 orders lower than that given by AlTiO MIS-HFETs without annealing and > 4 orders lower than that given by AlGaN/GaN Schottky-HFETs. suggesting that the annealing is effective to obtain good insulating properties of AlTiO. In comparison with $\mathrm{Al}_2\mathrm{O}_3$/AlGaN/GaN MIS-HFETs, the AlTiO MIS-HFETs exhibit higher maximum I_{D}, higher peak and better linearity of transconductance, shallower threshold voltage, and higher gate leakage (but still very low), suggesting that AlTiO is more favorable than $\mathrm{Al}_2\mathrm{O}_3$ for applications to AlGaN/GaN MIS-HFETs. We investigated temperature-dependent channel conduction of the AlTiO MIS-HFETs, where I_{D} decreases with increase in temperature. In the linear region, the decrease in I_{D} is mainly due to decrease in the electron mobility, while the contact resistance and the sheet electron concentration are almost constant. In the saturation region, the decreased I_{D} is proportional to the average electron velocity, whose temperature dependence is in-between those of the low- and high-field velocities. Temperature-dependent channel conduction of the AlTiO MIS-HFETs is similar to that of the BN MIS-HFETs. Moreover, we observe bumps in gate current for high drain-source voltages and high I_{D}, indicating increase in channel temperature due to the self-heating effect at high power consumption. This suggests low thermal conductivity of AlTiO due to random effects in alloy materials. In addition, we elucidated the temperature-dependent gate leakage, attributed to a mechanism with two terms. One is temperature-independent tunneling, dominant at low temperatures. The other exhibits Poole-Frenkel mechanism, dominant at high temperatures, from which we estimated AlTiO/AlGaN interface state density, which is $\sim 2 \times 10^{12}$ cm^{-2}eV^{-1}. Low-density AlTiO/AlGaN interface states lead to the strong gate controllability for the AlTiO MIS-HFETs.

Finally, we concluded that AlTiO films have low thermal conductivity, but low interface state density in comparison with those of BN films.

5.2 Future works

In this work, the BN/AlGaN/GaN MIS-HFETs show no bump and no negative conductance, confirming the high thermal conductivity of the BN films, which is an advantage for high-speed, high-power, and high-temperature device applications. However, BN/AlGaN interface state density is quite high, leading to weak gate controllability. In contrast to BN, AlTiO/AlGaN interface state density is low, leading to strong gate controllability, but AlTiO exhibits low thermal conductivity. Therefore, combination of BN and AlTiO may show high thermal conductivity of BN and low-density AlTiO/AlGaN interface states Hence, our next task is fabrication and characterization of BN/AlTiO gate stack for AlGaN/GaN MIS-HFETs. The devices, for example, will have $\sim$ 1-nm-thick AlTiO and $\sim$ 20-nm-thick BN, as shown in Fig. 5.1.

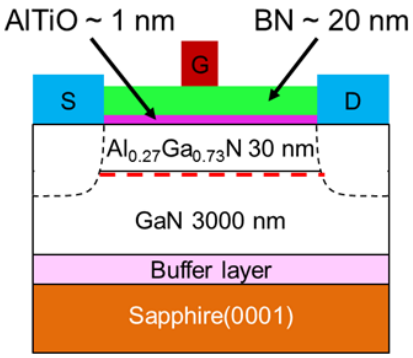


Figure 5.1: AlTiO/BN gate stack is a promising gate insulator for AlGaN/GaN MIS-HFETs.

On the other hand, the physical properties of AlTiO, such as energy gap E_g, dielectric constant k, breakdown field F_{br} are functions of the Al composition, as shown in Fig. 4.6 and 4.8. Based on the the trade-off between k and F_{br}, the Al_xTi_yO film with $x/(x+y) = 0.73$ was applied for fabrication of AlTiO/AlGaN/GaN MIS-HFETs However, Al_xTi_yO films with other compositions will be also favorable according to applications. Therefore, our other task is fabrication and characterization of Al_xTi_yO/AlGaN/GaN MIS-HFETs with other Al_xTi_yO compositions.

Appendix A

Poole-Frenkel mechanism

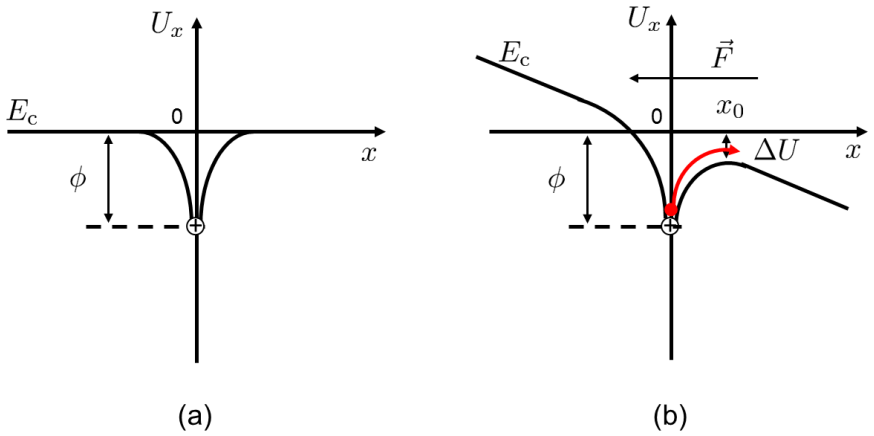


Figure A.1: Potential caused by a trap in (a) the absence of electric field and (b) the external electric field F, in which barrier height or trap depth is lowered by the field, enhance electron ionizations from the traps, showing Poole-Frenkel mechanism.

Figure A.1 shows energy barrier height in the case of without (a) and with electric field (b). Current density J under applied electric field F is given by:

$$J = qn\mu F \tag{A.1}$$

with electron charge q and electron density n. In the absence of F , the free electron density n due to the thermal ionization of the atoms, is proportional to ionization energy or trap depth ϕ, given by:

$$n \propto \exp\left[-\frac{\phi}{k_B T}\right] \tag{A.2}$$

In addition, potential $U(x)$ due to a trap at distance x from the trap is described by

$$U(x) = -\frac{q^2}{4\pi\varepsilon_0 kx} \tag{A.3}$$

In an external field, the potential is lowered by an additional amount of $-qFx$. Therefore,

we obtain

$$U(x) = -\frac{q^2}{4\pi\varepsilon_0 kx} - qFx \tag{A.4}$$

The maximum potential occurs at x_0, obtained by:

$$\frac{\mathrm{d}U(x)}{\mathrm{d}x}\Big|_{x=x_0} = \frac{q^2}{4\pi\varepsilon_0 kx_0^2} - qF = 0$$

or

$$x_0 = \sqrt{\frac{q}{4\pi\varepsilon_0 kF}} \tag{A.5}$$

Hence, the maximum barrier height for electron ionization from the trap, as shown in Fig. A.1(b), is given by

$$\phi - \Delta U = \phi - U(x_0) = \phi - \sqrt{\frac{q^3 F}{\pi\varepsilon_0 k}} \tag{A.6}$$

Therefore, the electron density n can be ionized from traps in the external electric field F is described by:

$$n = n_0 \exp\left[-\frac{1}{k_\mathrm{B}T}(\phi - \Delta U)\right] = \exp\left[-\frac{1}{k_\mathrm{B}T}\left(\phi - \sqrt{\frac{q^3 F}{\pi\varepsilon_0 k}}\right)\right] \tag{A.7}$$

Substitute Eq. A.7 into Eq. A.1, we obtain density of current dominant by electrons from traps in an materials, given by:

$$J = q\mu n_0 F \exp\left[-\frac{1}{k_\mathrm{B}T}\left(\phi - \sqrt{\frac{q^3 F}{\pi\varepsilon_0 k}}\right)\right] \tag{A.8}$$

Equation A.8 describes Poole-Frenkel mechanism [112, 113].

Appendix B

Transmission Line Model

Theory

Consider a slab of a semiconductor material having cross-sectional area A, thickness t, width W, and length L as shown in Fig. B.1. The resistance of the semiconductor material from end to end is

$$R_{\text{sem}} = \rho \frac{L}{A} = \rho_{\text{s}} \frac{L}{W},$$

where ρ [Ω.cm] and ρ_{s} [Ω/sq.] are resistivity and sheet resistance of the semiconductor, respectively. The ohmic contact covers each end of the slab. Each ohmic contact has a contact resistance R_{c}, Therefore, the total measurement resistance is simply

$$R_{\text{tt}} = 2R_{\text{c}} + R_{\text{sem}} = 2R_{\text{c}} + \rho_{\text{s}} \frac{L}{W}. \tag{B.1}$$

The values of the contact resistances depends on the contact sizes. Hence, they are normalized in term of the contact width, usually 1 mm.

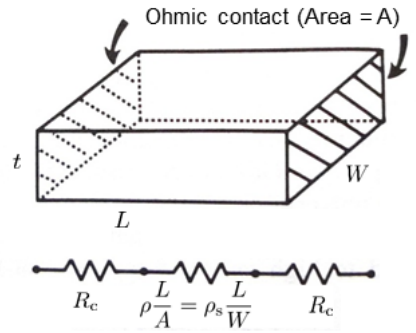


Figure B.1: A slab of material with ohmic contact on the two ends

In addition, the specific contact resistance ρ_{c} is often used for characterizing the resistance of the contacts. It is the contact resistance of a unit area for current flow perpendicular to the contact. The relation between the specific contact resistance and the contact resistance

has a form

$$R_c = \rho_c A. \tag{B.2}$$

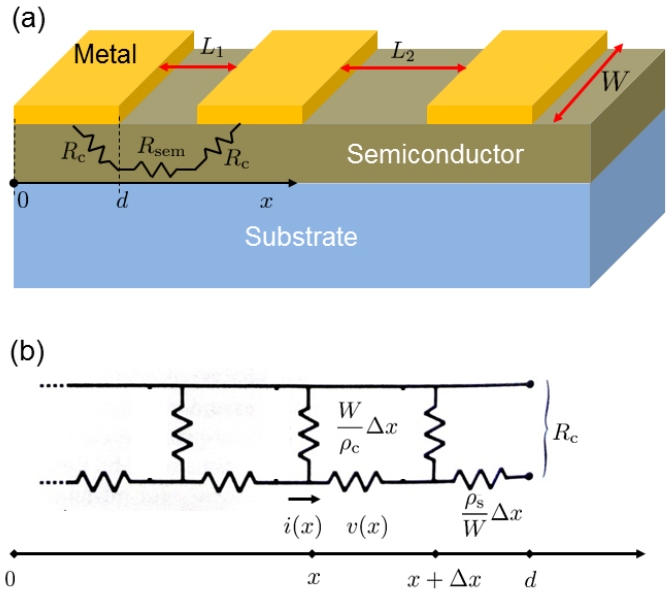


Figure B.2: Planar contact between the metal and the semiconductor

Practically, the contact between the metal and the semiconductor is planar as model shown in Fig. B.2(a). At this model, the contact between the metal and the semiconductor can be described as the set of resistors ρ_s/W, and conductors W/ρ_c which are defined in the unit contact length shown in Fig. B.2(b).

The voltage $v(x)$ and the current flowing the contact $i(x)$ follow differential equations

$$\frac{\mathrm{d}v}{\mathrm{d}x} = -\frac{\rho_s}{W}\, i, \tag{B.3}$$

and

$$\frac{\mathrm{d}i}{\mathrm{d}x} = -\frac{W}{\rho_c}\, v. \tag{B.4}$$

The second order differential equations have forms

$$\frac{\mathrm{d}^2 v}{\mathrm{d}x^2} = \frac{\rho_s}{\rho_c}\, v, \tag{B.5}$$

and

$$\frac{\mathrm{d}^2 i}{\mathrm{d}x^2} = \frac{\rho_s}{\rho_c}\, i. \tag{B.6}$$

The solution of Eq. B.6 is

$$i(x) = B\exp(\frac{x}{L_t}) + C\exp(-\frac{x}{L_t}), \tag{B.7}$$

where $L_t = \sqrt{\rho_c/\rho_s}$ is the transfer length. It is the distance from the edge that the current fall to 1/e (e being the base of the natural logarithm) of its original value. A and B are

constants defined from the boundary conditions, at $x = 0$,

$$i(0) = B + C = 0, \tag{B.8}$$

and at $x = d$,

$$i(L) = B \exp(d/L_t) + C \exp(d/L_t) = I_0. \tag{B.9}$$

Substituting Eq. B.8 into Eq. B.9, we get

$$B = \frac{I_0}{2\sinh(d/L_t)},$$

and

$$C = -B = -\frac{I_0}{2\sinh(d/L_t)}.$$

The current in Eq. B.7 is written again as

$$\begin{aligned} i(x) &= \frac{I_0}{2\sinh(d/L_t)} \left\{ \exp\left(\frac{x}{L_t}\right) - \exp\left(\frac{-x}{L_t}\right) \right\} \\ &= I_0 \frac{\sinh(x/L_t)}{\sinh(d/L_t)}. \end{aligned} \tag{B.10}$$

Substituting Eq. B.10 into Eq. B.4, we get the formula for the voltage

$$v(x) = -\frac{\rho_c}{W}\frac{\mathrm{d}i(x)}{\mathrm{d}x} = -\frac{\sqrt{\rho_c \rho_s}}{W} I_0 \frac{\cosh(x/L_t)}{\sinh(d/L_t)}. \tag{B.11}$$

The resistance at the edge $x = d$ is the contact resistance R_c and defined as

$$R_c = -\frac{v(d)}{i(d)} = \frac{\sqrt{\rho_c \rho_s}}{W} \frac{1}{\tanh(d/L_t)}. \tag{B.12}$$

If the length d of metal pad in the contact with the semiconductor is very large in comparison with the transfer length, $d/L_t \gg 1$, so $\tanh(d/L_t) \simeq 1$. The contact resistance is given

$$R_c \simeq \frac{\sqrt{\rho_c \rho_s}}{W}. \tag{B.13}$$

In opposite, if the length d of metal pad in the contact with the semiconductor is very small in comparison with the transfer length, $d/L_t \ll 1$, so $\tanh(d/L_t) \simeq d/L_t$. The contact resistance is derived

$$R_c \simeq \frac{\rho_c}{Wd} = \frac{\rho_c}{A}, \tag{B.14}$$

which is similar to Eq. B.2.

Measurement

The basic technique used to measure the contact resistance of planar ohmic contacts employs a test pattern composed of differently spaced ohmic contacts, as illustrated in Fig. B.2(a). We assume that the length of the contact between the metal and the semiconductor is very large.

Therefore, the contact resistance can be calculated by Eq. B.13. The total measurement resistance between two metal electrodes has the form

$$R_{\mathrm{tt}} = \frac{\rho_{\mathrm{s}}}{W} L + 2R_{\mathrm{c}} \simeq \frac{\rho_{\mathrm{s}}}{W} L + 2\frac{\sqrt{\rho_{\mathrm{c}}\rho_{\mathrm{s}}}}{W}. \tag{B.15}$$

The total resistance is a linear function of channel lengths L.

For determining the parameters of the contacts, we fit the experimental data by the linear function

$$y = aL + b, \tag{B.16}$$

in which $y = R_{\mathrm{tt}}W$, $a = \rho_{\mathrm{s}}$, and $b = 2\sqrt{\rho_{\mathrm{c}}\rho_{\mathrm{s}}}$. Example of measurement data and fitting function is shown in Fig. B.3. Fitting line cuts the vertical axis at $2\sqrt{\rho_{\mathrm{c}}\rho_{\mathrm{s}}}$ and the horizontal axis at $-2L_{\mathrm{t}}$. From the fitting, we can obtain the values of the contact resistance, the sheet resistance, and the specific contact resistance.

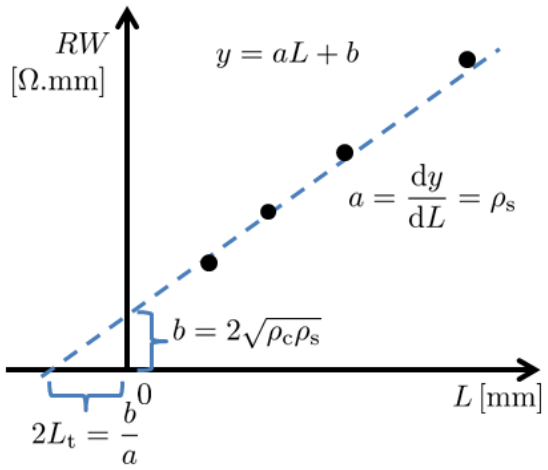


Figure B.3: Example of the ohmic contact experimental data fitting

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List of Publications

Journals

1. T. Q. Nguyen, H.-A. Shih, M. Kudo, and T. Suzuki: "Fabrication and characterization of BN/AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors with sputtering-deposited BN gate dielectric", Physica Status Solidi C **10**, 1401 (2013).

2. S. P. Le, T. Q. Nguyen, H.-A. Shih, M. Kudo, and T. Suzuki, "Low-frequency noise in AlN/AlGaN/GaN metal-insulator-semiconductor devices: a comparison with Schottky devices", Journal of Applied Physics, *in press*.

Conferences

International

1. H.-A. Shih, T. Q. Nguyen, M. Kudo, and T. Suzuki: "Characterization of gate-control efficiency in AlN/AlGaN/GaN metal-insulator-semiconductor structure by capacitance-frequency-temperature mapping", 2012 International Conference on Solid State Devices and Materials, Kyoto, Japan, September 25-27, F-7-3 (2012). Oral presentation

2. T. Q. Nguyen, H.-A. Shih, M. Kudo, and T. Suzuki: "AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistor (MIS-HFET) with sputtering-deposited BN gate dielectric", The 40th International Symposium on Compound Semiconductors, Kobe, Japan, May 19–23, TuC3-4 (2013). Oral presentation

3. M. Kudo, T. Q. Nguyen, H.-A. Shih, and T. Suzuki: "X-ray photoelectron spectroscopy for BN/AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors", 10th Topical Workshop on Heterostructure Microelectronics (TWHM 2013), Hakodate, Japan, September 2–5, 4-4 (2013). Poster presentation

4. T. Q. Nguyen, T. Ui, M. Kudo, Y. Yamamoto, H.-A. Shih, and T. Suzuki: "Application of AlTiO thin films to AlTiO/AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors", 2013 International Conference on Solid State Devices and Materials, Fukuoka, Japan, September 24–27, J-2-2 (2013). Oral presentation

5. T. Q. Nguyen, T. Ui, M. Kudo, H.-A. Shih, N. Hashimoto, and T. Suzuki: "Temperature-dependent characteristics of AlTiO/AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors", 2014 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD2014), Kanazawa, Japan, July 1–3, 7A-3 (2014). Oral presentation

Domestic

6. H.-A. Shih, T. Q. Nguyen, M. Kudo, and T. Suzuki: "Gate-control efficiency in AlN/AlGaN/GaN metal-insulator-semiconductor structure characterized by capacitance-frequency-temperature mapping", The 73th Autumn Meeting of Japan Society of Applied Physics, Matsuyama, September 11-14, 11a-PA5-10 (2012). Poster presentation

7. H.-A. Shih, T. Q. Nguyen, M. Kudo, and T. Suzuki: "Interface state density, gate-control efficiency, and intrinsic transconductance of AlN/AlGaN/GaN metal-insulator-semiconductor devices", The 61th Spring Meeting of Japan Society of Ap-plied Physics, Kanagawa, March 17-20, 19p-D8-12 (2014). Oral presentation

Award

1. **AWAD2014 Young Researcher Award** for

   T. Q. Nguyen, T. Ui, M. Kudo, H.-A. Shih, N. Hashimoto, and T. Suzuki: "Temperature-dependent characteristics of AlTiO/AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistors", 2014 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD2014), Kanazawa, Japan, July 1–3, 7A-3 (2014). Oral presentation