Steiner Routing Based on Elmore Delay Model for Minimizing Maximum Propagation Delay

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Research and development for increasing the computation power per unit area has been done intensively, and recent progress of device and fabrication technologies realize higher degree of integration and shorter gate switching delay. However, the signal propagation delay due to the resistance and the capacitance of an interconnection can not take the advantage of scaling effect, and it now becomes a dominant factor for limiting the operation speed(clock frequency) of VLSIs. To take the full advantage of the scaling effects and to develop VLSIs operating with higher clock frequency, design methodologies and design tools which can control and minimize the signal propagation delay are desired.

In the physical design level, the "minimum Steiner routing" is the most common routing method for each individual net. While its major concern is to minimize the total wire length of a routing aiming to minimize a total chip area, it can minimize also the overall load capacitance driven by a source gate and can contribute to minimize gate switching delay. "Path length constraint routing"(total wire length is minimized under the constraint of maximum path length) and "Distance preserving routing"(total wire length is minimized with the constraint of no–detour from any sink terminal to a source terminal) try to minimize overall load capacitance of a source gate under a certain constraint relevant to signal propagation delay from a source to each individual terminal. Among these problems, the minimum Steiner routing is known to be NP–hard. "Distance preserving routing" is expected to be polynomial time solvable, but its computational complexity is not known. Various heuristic algorithms and stochastic search algorithms have been developed for these problems. The delay evaluation in these problems relies on the first order approximation of a distributed network, and the recent advance of deep submicron technology makes it invalid in the accuracy of delay estimation. Elmore delay model which is a second order approximation model with regarding both distributed

resistance and distributed capacitance of a net has been proposed, and it enable us to evaluate signal propagation delay more accurately.

In this research, a Steiner routing based on the Elmore delay model is studied. Especially we are considering the problem to minimize the maximum signal propagation delay of a single net. To consider the topology of a routing, we employ binary tree representation. The root of a binary tree corresponds to the source, every leaf to a sink, and every internal vertex to a steiner vertex. A routing of a net is represented by a binary tree and placements of its steiner vertices. We regard the routing problem as two parts: determining the topology of the binary tree and the placement of steiner vertices.

To characterize the routing minimizing the maximum signal propagation delay based on Elmore delay model, we first focused on the local optimality in the steiner vertex placement problem such as 3-terminal problem and 4-terminal problem. 3-terminal problem is as follows: Given a terminal, binary tree representation, an arbitrary steiner vertex s, and placement of every steiner vertex except s, compute the optimal placements of s in the plane. In this problem, we prove that an optimal place is on a segment connecting between its parent p and the vertex nearest to p in the rectilinear space spanned by the children of s and sometimes unique. In addition, we show the way to determine the place on the segment. This property implies that the optimal routing of the problem to minimize the maximum signal propagation delay based on Elmore delay model is not always on the segments and vertices of Manhattan plane induced by terminals and so, the problem is not belonging in the class of combinatorial problems with a finite solution space. 4-terminal problem is similar to 3-terminal problem. This problem is to compute the optimal placement of adjacent two steiner vertices s_1 and s_2, given the placements of other steiner vertices, under some constraint condition. We also give the algorithm to compute the optimal place of the problem and prove the optimality of the placement.

Next, we investigate the application of those characteristics to the routing problems and propose two algorithms constructing initial routing and improving the routing. The initial routing algorithm constructs small total length routing on condition of distance preserving. We also show that the initial routing satisfies the optimality of 4-terminal problem. The algorithm minimizing the maximum signal propagation delay is consisting of two operations. The one based on 4-terminal problem changes the structure of the binary tree T by replacing a subtree on T and the other based on 3-terminal problem replaces a steiner vertex in a plane.

Lastly, we give the simulation and its results of proposed algorithms. As inputs, we generated some net patterns consisting of a source and 10 sinks. Each terminals are set randomly in the grid. Since the optimal solution cannot be computed, we compare our solution with a trivial lower bound. The lower bound is the sum of the products of driver resistance with the capacitance of the wire equivalent to the half of the perimeter of the bounding box containing all terminals and the maximum of resistance of a wire equivalent to a distance from the source to a sink with sink capacitance. It is clear that the optimal solution is greater than the lower bound. In the experimental results, the ratio to the lower bound, is 159% in maxinum and 125% in minimum.