Title	ソフトウェア制御によるキャッシュ参照ウェイ限定手法の研究
Author(s)	小林，智弘
Citation	
Issue Date	2015-03
Type	Thesis or Dissertation
Text version	author
URL	http://hdl.handle.net/10119/12670
Rights	
Description	Supervisor: 田中 清史，情報科学研究科，修士

Study on Accessing Way Predicted by Software Control

Tomohiro Kobayashi (1310025)

School of Information Science,
Japan Advanced Institute of Science and Technology

February 12, 2015

Keywords: Reducing energy, Way-prediction.

1 Introduction

Most of current processors adopt set-associative cache to reduce miss rates. A conventional set-associative cache accesses all the data ways in parallel with the tag lookup to minimize access time. However, probing all the data ways is wasteful because matching way is only one. There are previously proposed techniques to solve this problem. These techniques reduce the wasted energy by using way-prediction accesses, but require substantial, additional hardware or complicated cache structure. This paper proposes TracePC Way prediction(TracePC) and Simple-Counter Way prediction(SC) schemes. These schemes use way-prediction access without substantial, additional hardware or complicated cache structure.

2 Related works

As way prediction access scheme, Predictive Sequential Associative Cache(PSA)[1], was proposed. PSA is the first study of way prediction accesses by using hardware tables. PSA was proposed to improve set-associative cache access latency. Unlike a conventional set-associative cache , PSA probes only one way by using way prediction. This technique reduces data access time

compared to a conventional set-associative cache. As another study of way prediction , Reactive Associative Caches(R-A Cache)[2] was proposed to improve set-associative cache access times. R-A Cache has high accuracy of way prediction by isolating conflicting blocks from no conflicting. Related work[3] applies PSA and R-A Cache to reduce cache energy. This study exploits the cache structure that accesses only one way for reducing cache energy. In addition, this work applies way prediction for not only d-cache but also i-cache to achieve cache energy saving.

3 Proposed method

In this paper, we propose TracePC Way Prediction(TracePC) and Simple-Counter Way prediction(SC) , which are way prediction schemes. TracePC statically determines accessed ways by using memory access traces obtained in advance. Memory access instructions' PC values and accessed ways by the instructions are traced. The most accessed way with each PC value is determined as a way to be accessed. SC dynamically determines a way to be accessed by using small counters. A counter is required for each way and it counts the number of accesses to the way in program execution divided into phases.

4 Evaluation

We evaluate effectiveness of proposed schemes in reducing data access energy by using simulator(developed as a C program). We evaluate way prediction accuracy of PSA, R-A Cache and proposed schemes. SPEC2000 benchmark programs are used in the evaluation and programs' inputs are "ref". TracePCs' traces are generated using "train" as programs' input. In this evaluation, L1 d-cache adopts a 4-way set-associative cache which accesses only a predicted way. L2 cache adopts a conventional 4-way set-associative cache. Average way prediction accuracies of comparative schemes are 69%(PSA) and 96%(R-A Cache). Our average way prediction accuracies are 36%(TracePC), 43%(SC). Relative access energy savings to a conventional set-associative cache are 33.5%(PSA), 15.6%(R-A Cache), 30.0%(TracePC) and 31.1%(SC).

5 Conclusion

In this paper, we proposed TracePC Way prediction(TracePC) and Simple-Counter Way prediction(SC) schemes. These schemes don't require substantial, additional hardware or complicated cache structure. We evaluated data access energy and way prediction accuracies of our schemes by using SPEC2000 benchmark programs. TracePCs' average way prediction accuracy is 36%, but it has high accuracy in programs which memory access instructions' PC values are strongly related to accessed ways. SC has average way prediction accuracy of 43% without substantial, additional hardware. Relative access energy savings to a conventional set-associative cache are 30.0%(TracePC) and 31.1%(SC).

References

[1] B. Calder, D. Grunwald, and J. Emer. Predictive sequen- tial associative cache. In Proceedings of the Second IEEE Symposium on High-Performance Computer Architec- ture, Feb. 1996.

[2] B.Batson and T. N. Vijaykumar. Reactive associative caches. In proceedings of International Conference on parallel Architecutures and Compiliation, 2001.

[3] Michael D. Powell, Amit Agarwal, T. N. Vijaykumar, Babak Falsafi and Kaushik Roy, “Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping” 2001.

[4] SimpleScalar <http://www.simplescalar.com/> (accessed 2015/02/09)

[5] SPEC2000 <http://www.spec2000.com/> (accessed 2015/02/09)