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PAPER *Special Section on Fundamentals and Applications of Advanced Semiconductor Devices*

Tunable Threshold Voltage of Organic CMOS Inverter Circuits by Electron Trapping in Bilayer Gate Dielectrics

Toan Thanh DAO[†a)], ***Member and*** **Hideyuki MURATA**[††b)], ***Nonmember***

SUMMARY We have demonstrated tunable *n*-channel fullerene and *p*-channel pentacene OFETs and CMOS inverter circuit based on a bilayer-dielectric structure of CYTOP (poly(perfluoroalkenyl vinyl ether)) electret and SiO_2. For both OFET types, the V_{th} can be electrically tuned thanks to the charge-trapping at the interface of CYTOP and SiO_2. The stability of the shifted V_{th} was investigated through monitoring a change in transistor current. The measured transistor current versus time after programming fitted very well with a stretched-exponential distribution with a long time constant up to 10^6 s. For organic CMOS inverter, after applying the program gate voltages for *n*-channel fullerene or *p*-channel pentacene elements, the voltage transfer characteristics were shifted toward more positive values, resulting in a modulation of the noise margin. We realized that at a program gate voltage of 60 V for *p*-channel OFET, the circuit switched at 4, 8 V, that is close to half supply voltage V_{DD}, leading to the maximum electrical noise immunity of the inverter circuit.
key words: *controllable threshold voltage, stretch-exponential equation, noise margin enhancement, organic CMOS inverter*

1. Introduction

In recent years, organic transistor circuits has been rapidly emerging since their attractive features including low-cost, low-temperature manufacturing, and mechanical flexibility, which are relatively difficult to be realized from Si-based counterparts [1]–[4]. In particular, tunable threshold voltage (V_{th}) of organic field-effect transistor (OFET) is very crucial for organic integrated circuit construction. This is due to the V_{th} shifting to a lower value results in a decrease in power consumption of the transistor circuit while holding a high speed circuit operation [5]. On the other hand, controllable V_{th} allows the switching voltage of each OFET device to be modified, which can help to minimize manufacturing variation. Moreover, in complementary metal-oxide-semiconductor (CMOS) technology, due to a difference in the V_{th} and the other electrical parameters between the *p*-channel and *n*-channel OFETs, the switching voltage of inverter may be close to either the ground voltage or the power supply. This results in a small noise margin, which in turn leads to the inverter is very susceptible to electrical noise. Thus, it is necessary to place the switching voltage of the circuit at half power supply voltage by controlling the V_{th} of the transistor elements in order to achieve the maximum noise immunity of the CMOS inverter [5], [6].

Several approaches have been recently introduced to tune the V_{th} in organic transistor circuit. The V_{th} tuning can be obtained by varying a doping concentration of Au nanoparticles (NPs) [7] or using polar self-assembled monolayers (SAMs) [8], [9] in a gate dielectric. Although the V_{th} is well controlled with those techniques, the V_{th} is only defined at manufacturing step [7]–[9]. To dynamically control the V_{th} after fabrication, a number of methods have been developed. The tunability of the V_{th} results from using space charge polarization [10] or charge-trapping polymer [11] or ferroelectric gate dielectrics [12], or Al floating-gate [13], [14]. However, the limitations of such methods are required long switching time and large switching voltage [10], [11] due to gradual formation of space charge polarization [10] or poor device performance resulting from the rough surface of ferroelectric materials [13] or instability of the shifted V_{th} because the trapped charges easily leak through a SAM blocking-layer [13].

In our recent works [15], we have demonstrated highly stable transistor memories based on a double gate dielectric structure of poly(perfluoroalkenyl vinyl ether) (CYTOP) and SiO_2. The V_{th} can be modulated thanks to electron trapping at the interface between CYTOP and SiO_2. Taking the advantage of that, we have focused on the memory functionality by using the different levels of the V_{th} to present the binary values. The resulting memory transistors exhibit high performance with a large on/off ratio and excellent retention stability of data storage [15], [16].

In this work, we extend the findings to construct electrically tunable CMOS inverter circuits with a bilayer-dielectric structure of CYTOP and SiO_2. We firstly, in both *n*-channel fullerene and *p*-channel pentacene OFET elements, examined the tunability of V_{th} and its stability after tuning through a current measurement. We found that a change in the drain current of the OFETs followed a stretched-exponential distribution with a long time constant of 10^6 s. In the latter part of this report, we describe additional experiments on control of the CMOS inverter circuit. The voltage transfer characteristic of the inverter was positively shifted after applying the program gate voltages for both transistor types. At a program gate voltage of 60 V for *p*-channel OFET, the inverting voltage of 4.8 V was realized, which approximates the half supply voltage. This brings about the maximum immunity of the circuits against

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[†]The author is with University of Transport and Communications, No. 3, Cau Giay Street, Lang Thuong, Dong Da, Hanoi, Vietnam.
[††]The author is with Japan Advanced Institute of Science and Technology, 1-1 Asahidai, Nomi, Ishikawa, 923-1292, Japan.
a) E-mail: daotoan@utc.edu.vn
b) E-mail: murata-h@jaist.ac.jp
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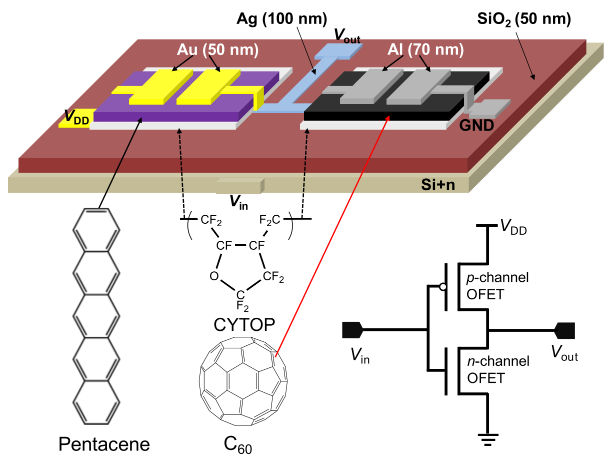

Fig. 1 Illustration of OFET and CMOS inverter circuit layout and chemical structures of materials utilized in our experiments together with equivalent circuit of inverter.

the effect of electrical noise.

2. Experimental Procedure

Figure 1 presents the schematic illustration of the inverter and the chemical structures of the used materials together with the equivalent circuit of the CMOS inverter. The transistor circuit was fabricated on a heavily doped Si (n+Si, resistivity: 1–100 Ω cm) gate electrode coated with a SiO_2 (50 nm) dielectric layer. The silicon wafer was cleaned by ultrasonication (in acetone for 5 min, in detergent for 10 min, twice in pure water for 5 min, and in IPA for 10 min) and subjected to UV-O_3 treatment. A CYTOP electron-trapping layer (CTL-809 M, Asahi Glass) was spin-coated onto the gate dielectric at 2000 rpm for 60 s using a 0.5 wt% CYTOP solution (CT-Solv. 180) and dried at 100°C for 2 h. The CYTOP thickness of 10 nm was the optimized value as presented in our earlier work [15]. Fullerene (C_{60}, Nanom purple SUH, purity: 99.9%) and pentacene (Sigma-Aldrich Company) were thermally deposited through shadow masks onto the CYTOP layer to form the 40-nm-thick semiconductor layers for the *n*-channel and *p*-channel OFETs, respectively. To produce transistor configuration, 70-nm-thick Al and 50-nm-thick Au source-drain electrodes were formed on C_{60} and pentacene layers by thermal evaporation through shadow masks. The L and W of the OFETs were set at 75 and 5000 μm, respectively. Finally, to complete the inverter circuit, a 100-nm-thick Ag interconnection line was vacuum-deposited through a shadow mask. The base pressure during the vacuum deposition was of 2×10^{-6} torr. Electrical characteristics of the OFETs and CMOS inverter were measured with a Keithley 4200 semiconductor parameter analyzer in a dry nitrogen atmosphere at room temperature in a dark probe station.

3. Results and Discussion

Figure 2 shows the output characteristics of the OFETs. The drain current (I_D) was monitored while the drain voltage

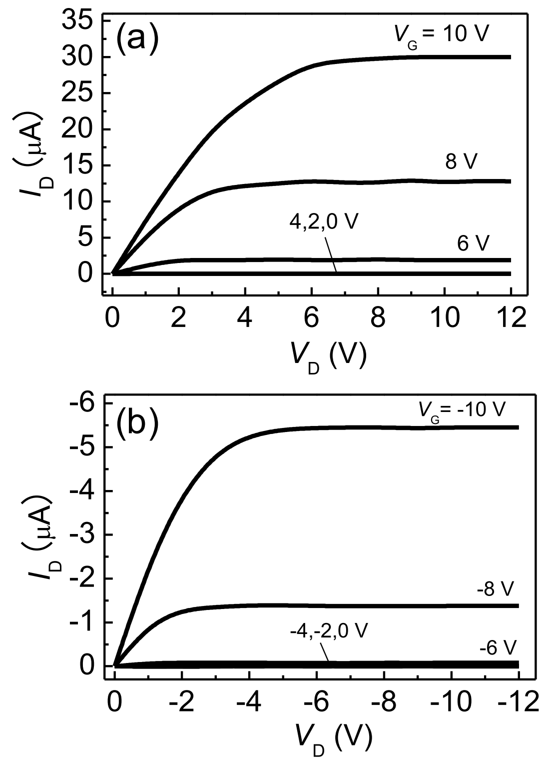

Fig. 2 Output characteristics of (a) *n*-channel and (b) *p*-channel OFET elements.

Table 1 OFET parameters.

OFET type	μ ($cm^2\ V^{-1}\ s^{-1}$)	V_{th} (V)	On/off ratio
n-channel	0.4	2.8	5.5×10^4
p-channel	0.3	−4.4	2.2×10^4

(V_D) was varied at the different gate voltage (V_G). In a low V_D region, a linear relationship between V_D and I_D was realized, suggesting efficient electron or hole injections at interfaces of C_{60}/Al or pentacene/Au. The I_D saturated at a high V_D because the conducting channels were pinched-off. These results indicate that the as-fabricated organic transistors exhibit standard *n*/*p*-channel field-effect operations. Table 1 presents the initial FET parameters in this study, where the field-effect mobility (μ) and the V_{th} were extracted by fitting the curves with the standard equation for I_D in the saturation regime. The estimated μ and other parameters obtained in our experiments are typical values in OFETs using C_{60} or pentacene as the semiconducting layers [11], [15], [16].

Figure 3 shows the transfer characteristics of OFETs recorded after application of a positive program gate voltage. In all processes, the pulse width of the program voltage is 1 s and the source-drain electrodes were grounded [16]. As can be seen in Fig. 3, the transfer curves positively shifted in both types of OFETs. Indeed, upon application of a high positive program voltage to a gate electrode, electrons are injected from the source-drain electrodes through the semiconducting and CYTOP layers and subsequently trapped at the interface of CYTOP and SiO_2. The interfa-

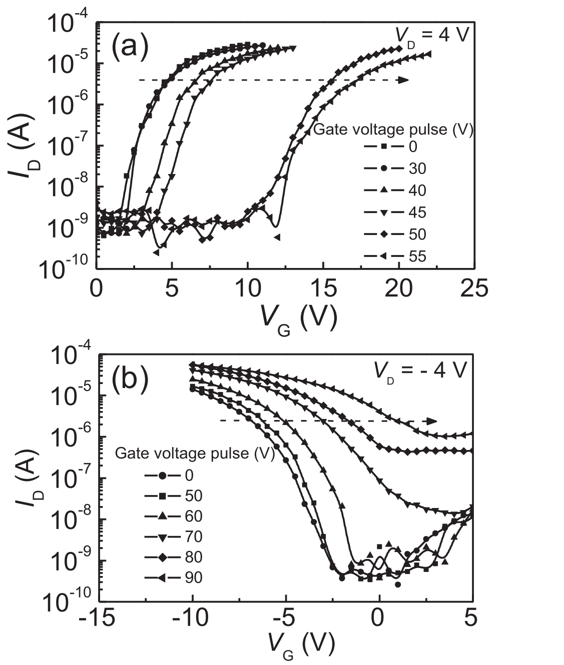

Fig. 3 Transfer characteristics of (a) *n*-channel and (b) *p*-channel OFETs measured after applying various program gate voltages.

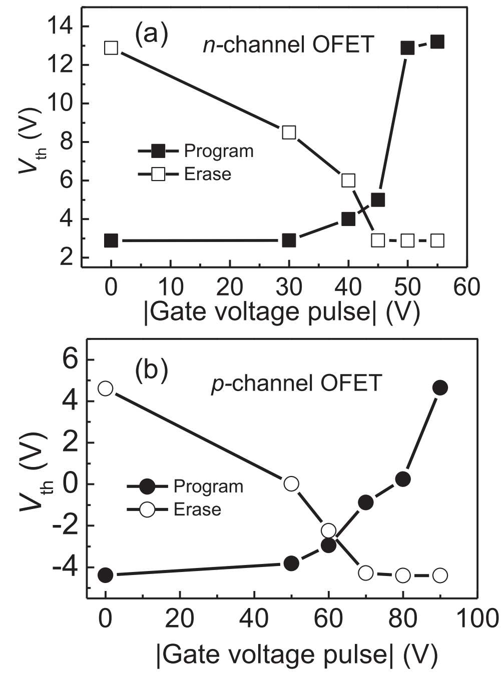

Fig. 4 Relationships between V_{th} and gate voltage pulse in (a) *n*-channel and (b) *p*-channel OFET elements. OFETs were programmed/erased by changing magnitude of gate voltage pulse while source-drain electrodes were grounded. Width of each pulse was about 1 s.

cial trapping can be understood due to the electrets property of CYTOP material [17] and has been discussed in detail in our previous works [15], [16]. The trapped electrons then deplete electrons in the *n*-channel C_{60} or induce additional holes in *p*-channel pentacene, leading to the V_{th} was shifted to more positive voltage. Note that, the trapped electrons at CYTOP/SiO_2 interface remain there without the need for any applied voltage, resulting in a built-in electric field. During the measurements of transfer characteristics, for *n*-channel C_{60} OFET, when the applied electric field between the gate electrode and the semiconductor compensates the built-in electric field, the transistor operated similarly to the its initial state. Thus, the off-current of the device is almost unchanged (Fig. 3(a)). Meanwhile, in *p*-channel OFET, the built-in electric field leads to an increase in the number of holes accumulated in the pentacene channel that is the possible reason for an increase in the off-current (Fig. 3(b)).

We would like to confirm that the control of the V_{th} is a reversible phenomenon. After applying a negative erase gate voltage, the trapped electrons were removed from the interface, the V_{th} completely returns to the initial position. Figure 4 presents the characteristics of the reversible shifts in the V_{th}. The change of the V_{th} increased as the gate voltage pulse was increasing. Under applications of program/erase gate voltage pulses between 0 and ±55 V (for the *n*-channel OFET device) and between 0 and ±90 V (for the *p*-channel OFET device), the V_{th} was reversely controlled, from +2.8 to +12.8 V for the *n*-channel OFET and from −4.4 to +4.6 V for the *p*-channel OFET. The required program voltage for *p*-channel device is larger than that for *n*-channel one (Fig. 4) because the facts that the larger injection barrier at the interfaces of Au/pentacene and electron transport through lower electron-mobility of pentacene [16].

Once the V_{th} can be controlled, its stability is the other important factor. In subsequent experiments, we studied the stability of the V_{th} after tuning to the new value. It was reported that an investigation of the change in the V_{th} of an OFET device can be converted to observation of the change in the I_D, and the relationship between the drain currents at initial $I_D(0)$ and at the waiting time t I_D (t) can be expressed by a stretched-exponential equation [18]:

$$\frac{I_D(t)}{I_D(0)} = \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right], \tag{1}$$

where τ is the time constant and β is the dispersion parameter. To apply that knowledge for our devices, after programming, I_D was continuously measured over 10^5 s at V_G = ±10 V and V_D = ±4 V for *n*-channel and *p*-channel OFETs (Inset of Fig. 5). The μ was found to slightly decrease from 0.40 to 0.35 cm^2 V^{-1} s^{-1} for the *n*-channel OFET and from 0.30 to 0.27 cm^2 V^{-1} s^{-1} for the *p*-channel OFET, this is due to a decrease in the I_D. Then, the $I_D(t)/I_D(0)$ versus the waiting time were subsequently estimated. As can be seen in Fig. 5, the experimental data fit very well to the calculated results obtained with Eq. (1). The extracted τ and β were shown in Table 2 where the τ obtained from *p*-channel device is higher than that of *n*-channel OFET. This is probably due to, during bias process, the trapped electrons penetrate from the trap site through the pentacene layer slower than through the C_{60} layer because of lower electron-mobility of pentacene material. Significantly, the obtained τ is almost one order of the magnitude larger than that in a normal OFET [18], suggesting a highly stable V_{th} obtained in our

Table 2 Parameters for stretched-exponential equation.

OFET type	τ(s)	β
n-channel	0.5×10^6	0.5
p-channel	3.6×10^6	0.3

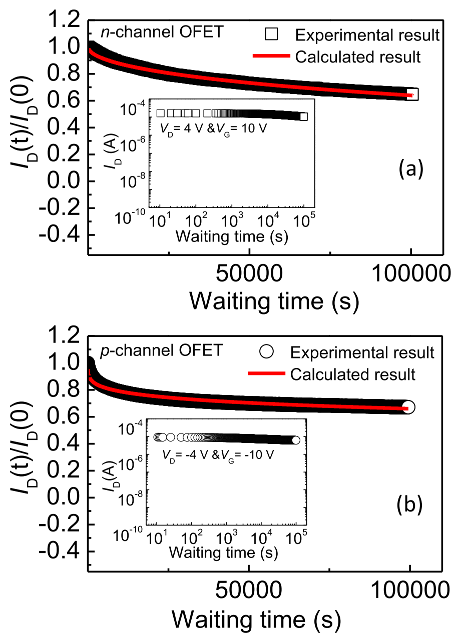

Fig. 5 $I_D(t)/I_D(0)$ change as function of time during continuous bias voltages of (a) *n*-channel and (b) *p*-channel OFETs. Squares or circles represent experimental results, and solid curves represent calculated results obtained using stretched-exponential equation.

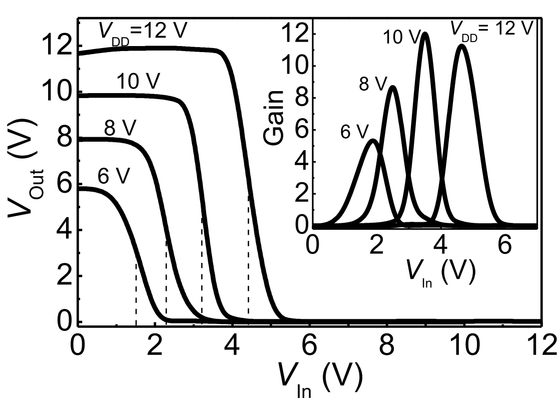

Fig. 6 Voltage transfer characteristics and corresponding voltage gains (Inset) of CMOS inverter circuit at various V_{DD}. Dotted lines indicate V_{ins} positions.

devices even after tuning to the new value.

In organic CMOS technology, the changeable V_{th} results in tunable switching voltage of inverter (V_{ins}), which in turn help to adjust the noise margin, avoiding the inadvertent switching of the circuit [5], [9]. To verify that hypothesis, we further studied on a CMOS inverter configuration constructed of *p*-channel pentacene and *n*-channel fullerene devices as discussed above. Figure 6 shows the voltage transfer characteristics and corresponding voltage gain of the organic CMOS inverter at various drain–drain voltages (V_{DD}). For each curve, when an input voltage (V_{In}) was varied from 0 to supply voltage V_{DD}, the output voltage (V_{Out}) swings from V_{DD} to 0 V, indicating a typical inverting operation. The voltage gain, estimated by $-dV_{Out}/dV_{In}$, increased with increasing the V_{DD}. This trend is similar to that in other circuit systems [14], [19]. The obtained gain can be comparable to that of previous organic inverters [7], [8].

It knows that the V_{ins} occurs when both *n*-channel and *p*-channel devices are saturated and the V_{ins} can approximately be given by the following equation [19]:

$$V_{ins} = \frac{V_{DD} - |V_{th,p}| + V_{th,n}\sqrt{\dfrac{K_n}{K_p}}}{1 + \sqrt{\dfrac{K_n}{K_p}}}, \qquad (2)$$

where $V_{th,n}$ and $V_{th,p}$ are the threshold voltages for *n*-channel and *p*-channel OFETs, respectively; $K_n = (W/L)\mu_n C_i$; $K_p = (W/L)\mu_p C_i$, in which C_i is the capacitance per unit area of the gate dielectric. Since the V_{th} and the μ parameters of the *n*-channel device were different from those of the *p*-channel one as presented in Table 1, our initial inverter did not switch at the theoretical point of $1/2V_{DD}$ as evidently shown in Fig. 6. Thus, the voltage transfer characteristic should be relocated.

The controllable characteristics of the organic inverter circuit at V_{DD} of 10 V are shown in Fig. 7, where each V_{Out}–V_{In} relationship was taken after applying a program gate voltage for the *n*-channel or *p*-channel OFETs. The positive shift of V_{th} in both transistor types caused the switching voltage of inverter V_{ins} tunes also to more positive voltage value. We would like to note that when applying a program voltage of 50 V for *n*-channel device (shifted $V_{th} = \sim 10$ V, Fig. 4), the V_{ins} cannot be observed since it is actually larger than the V_{DD}. The changes in the V_{ins} as a function of the gate voltage pulse at V_{DD}=10 V are shown in Fig. 8 (opened curves). The V_{ins} was tuned over a wide range, from 3.3 to more than 10 V after programming the *n*-channel OFET (Fig. 8(a)) and from 3.3 to 6.6 V after programming the *p*-channel OFET (Fig. 8(b)). Interestingly, we found that, at the program voltage of 60 V, the V_{th} of *p*-channel OFET was placed at -2.9 V (Fig. 4(b)), nearly equal to that of the initial *n*-channel device (2.8 V). This leads to the inverter was switched at a voltage of 4.8 V, which is close to the ideal value (1/2 V_{DD}). On the other hand, to compare with the measured values, the V_{ins} of the organic CMOS inverter was theoretically calculated using Eq. (2) and plotted as filled curves in Fig. 8. As can be seen in Fig. 8(a) and (b), the experimental data tend to follow the calculated results with a relatively small error.

An electrical noise immunity of a digital CMOS circuit is quantified as the noise margin (*NM*) which is the maximum noise signal that can be superimposed on a digital signal without changing the function of the circuit [19]. In order to examine effect of the V_{th} on the *NM*, in Fig. 9, we have estimated the *NM* at the high (NM_H) and low (NM_L)

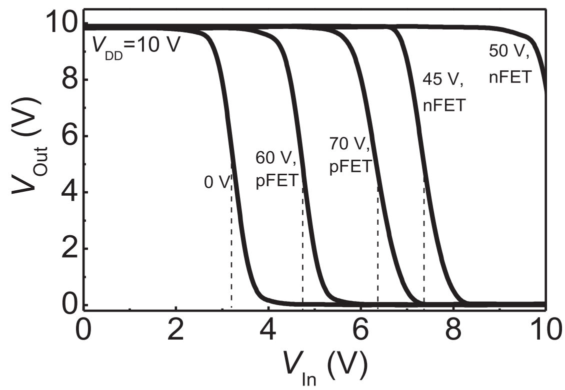

Fig. 7 Voltage transfer characteristics of CMOS inverter circuit measured after applying program gate voltage. pFET and nFET in figures are same definitions with *p*-channel OFET and *n*-channel OFET, respectively.

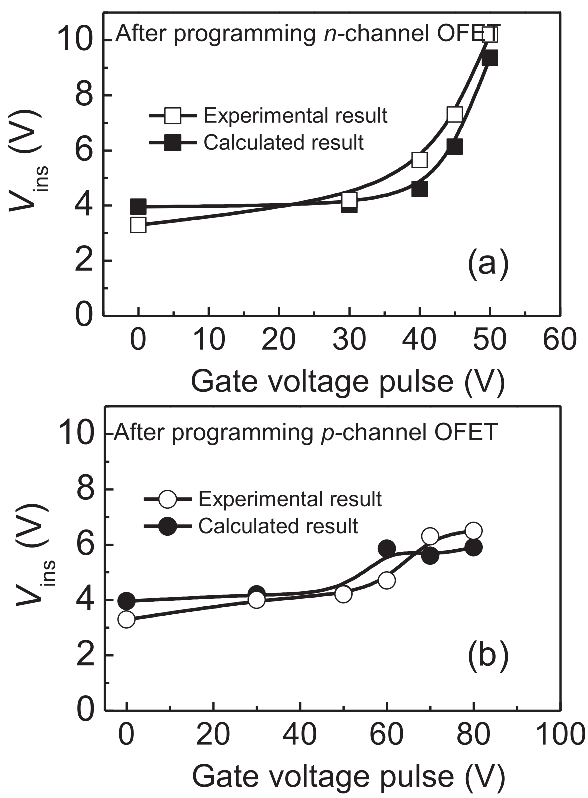

Fig. 8 Change of V_{ins} as function of gate voltage pulse after programming (a) *n*-channel or (b) *p*-channel OFETs at V_{DD}=10 V. Here, when OFET element of CMOS inverter was programmed, its complement was kept at initial state. Opened curves represent experimental results, and filled curves represent calculated results obtained using Eq. (2) with the $V_{th,n}$ and $V_{th,p}$ taken from Fig. 4.

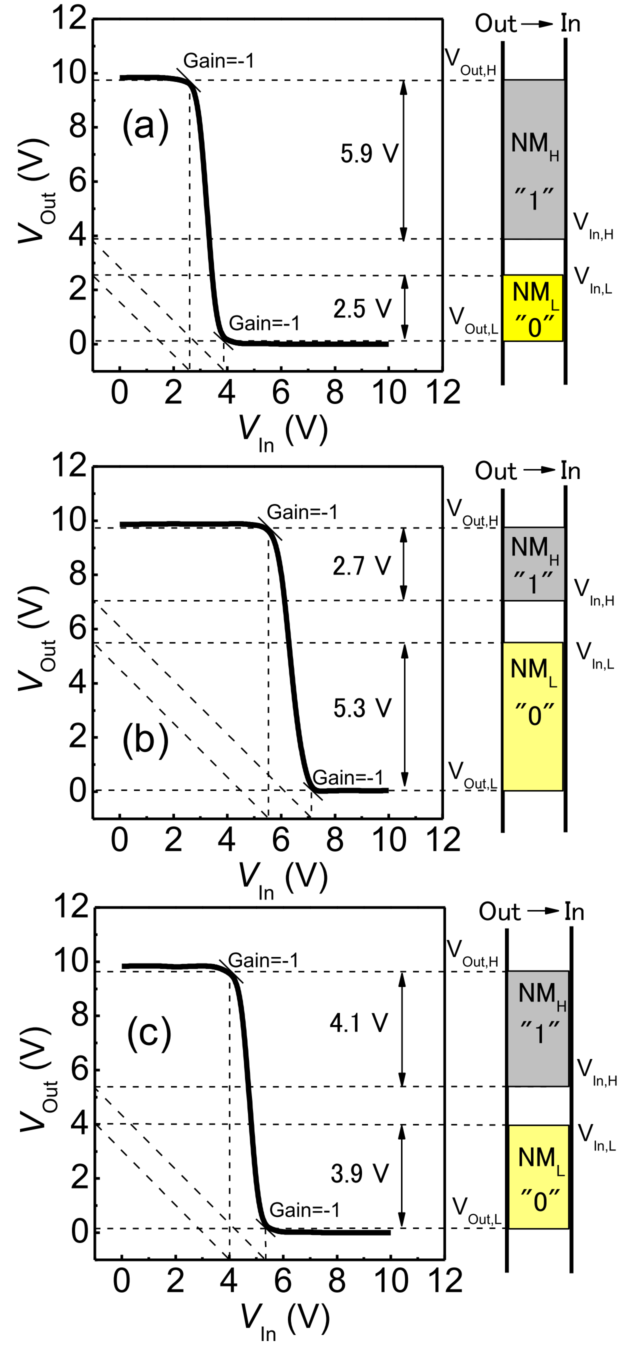

Fig. 9 Noise margins of CMOS inverter estimated at (a) initial and after applications of program voltages of (b) 70 V and (c) 60 V for *p*-channel OFET. Gap between NM_L and NM_H is undefined region.

logic levels from the selected voltage transfer characteristics at V_{DD}=10 V using the following equations [19]:

$$NM_H = V_{Out,H} - V_{In,H} \tag{3}$$

$$NM_L = V_{In,L} - V_{Out,L} \tag{4}$$

where $V_{In,L}$ and $V_{In,H}$ are the input low and high voltages, $V_{Out,H}$ and $V_{Out,L}$ are the output high and low voltages. The $V_{In,L}$ and $V_{In,H}$ are extracted at the points where the gain = −1 while the $V_{Out,H}$ and $V_{Out,L}$ are the output voltages for V_{In} = 0 V and V_{DD}, respectively [20]. As can be seen in Fig. 9(a) and 9(b), there is no balance between the NM_L and the NM_H. The NM_L (2.5 V, obtained at initial state) and NM_H (2.7 V, obtained after applying the program voltage of 70 V for *p*-channel device) are both narrow and close to the ground potential and the supply voltage V_{DD}, respectively. This may cause a failure of the logic functionality since the inverter is quite susceptible to electrical noise. However, at the program gate voltage of 60 V for *p*-channel device, the balance between the NM_L (3.9 V) and the NM_H (4.1 V) is significantly improved as shown in Fig. 9(c). This results in a greater noise immunity [5], [9], i.e., the circuit can operate more reliably.

We would like to stress here that, to balance between the NM_L and the NM_H at a certain V_{DD}, it is necessary to choose a suitable program gate voltage for *n*-channel or *p*-channel OFETs based on the tendency documented in Fig. 4 in order that results in a symmetrical V_{th} for both transistor types.

4. Conclusion

In summary, we have demonstrated tunable threshold voltage OFETs and CMOS inverter circuit based on pentacene/C_{60} and a bilayer-dielectric structure of CYTOP and SiO_2. The V_{th} of OFETs can be electrically switched thanks to electron trapping at the interface of CYTOP and SiO_2 layers. The stability of the V_{th} after programming was examined through an investigation of the change in transistor current, which fitted very well with a stretched-exponential equation with a time constant up to 10^6 s. For organic CMOS inverter circuit, the voltage transfer characteristic was positively shifted after applying the program gate voltages for *n*-channel or *p*-channel elements. The noise margin *NM* of the inverter was found to be strongly depended on the V_{th}. Significantly, at a program gate voltage of 60 V, the V_{th} of *p*-channel OFET was set to be nearly equal to that of the initial *n*-channel device, which provides an excellent balancing between the NM_L and the NM_H at supply voltage V_{DD} of 10 V. This in turn results in the maximum electrical noise immunity of the circuits. The experimental data suggest that the organic transistor and inverter based on a bilayer-dielectric structure of CYTOP and SiO_2 can be used to fabricate reconfigurable complex organic CMOS integrated circuits.

Acknowledgments

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Toan Thanh Dao received the M.S. degree in Electronics Engineering from University of Transport and Communications (UTC), Vietnam, in 2007 and Ph.D in Nano Science and Technology in 2012 from Japan Advanced Institute of Science and Technology (JAIST). From 2012 through 2013, he worked as a postdoctoral researcher in JAIST. Currently, he is with Faculty of Electrical-Electronic Engineering, UTC. His research interest is emerging electronics such as memory transistor, memristor, CMOS ICs using organic semiconductor. He is a member of the Institute of Electronics, Information and Communication Engineers.

Hideyuki Murata received his Ph.D. in materials science at Kyushu University, Japan in 1992. He joined Mitsui Petrochemical Industries as a research scientist. In 1996, he moved to Naval Research Laboratory, USA, as a research contractor. He was appointed as senior lecturer in the Department of Chemistry, Imperial College London, UK in 2001. He returned to Japan as an associate professor at Japan Adanced Institute of Science and Technology in 2002 and was promoted to professor in 2009. Murata's research focuses on the molecular electronic materials and their application to electronic devices, including OLEDs, organic photovoltaics, organic field effect transistors and organic memories.