ABSTRACT OF DOCTORAL DISSERTATION

To realize all solution-process self-aligned oxide semiconductor thin film transistor (TFT), we have developed a novel diffusion method to dope the oxide semiconductor source and drain regions (S/D regions). Since the self-aligned structure exhibits a low parasitic capacitance and an ability to scale down the size of the device, the TFT with this structure was studied in this dissertation. We studied the ZrInZnO as an oxide semiconductor because of its ability in improving the TFT performance and bias-stress ability.

In our diffusion method, a doping solution, i.e. Sn:PPC solution which is a mixture of a Sn solution and polypropylene carbonate (PPC) solution was prepared. The Sn:PPC solution was coated on the ZrInZnO S/D regions and then the sample was annealed to allow Sn atoms diffuse into the ZrInZnO. Because PPC can be decomposed completely into CO_2 and HO_2 at temperature below 300 ^oC, the utilization of PPC helps to prevent the formation of the SnO_x film, derived from the Sn solution, between S/D regions of the self-aligned structure.

The first work of this study involves the preparation and characterization of the Sn:PPC solution. TG/DTA, FT-IR, DLS and mass spectrometry methods were used to characterized the Sn:PPC solution. The results show that the solute in the Sn:PPC solution was in an configuration with coordination of large PPC molecules with Sn clusters. The Sn cluster was in a configuration of coordinated PrA ligand, water and oxygen around the Sn atom. The size of the Sn clusters was about 1.6 nm, while PPC molecules in solution was about 1.9 nm, 5.5 nm, 37.6 nm and 721 nm.

In the second work, the Sn:PPC solution was employed to fabricate high conductivity ZrInZnO for S/D regions of self-aligned TFT. The Sn:PPC solution was coated and annealed to make Sn diffuse into the ZrInZnO film. It was confirmed by AUS method that Sn diffused into ZrInZnO film to a depth of 22 nm. Sn acts as a donor in ZrInZnO, which results in an increase in the conductivity of the ZrInZnO film. Resistivity of the Sn-diffused ZrInZnO was reduced from 4×10^3 Ω cm to 1.8×10^{-2} Ω cm at annealing temperature of 300 ^oC under N_2 ambience when the Sn:PPC solution was used. The increase in resistivity of the sample annealed at temperature over 500 ^oC was due to the change in structure characteristic of the ZrInZnO film. To make high conductive ZrInZnO the ambience including oxygen should be avoided.

The third work concentrated to fabrication of self-aligned ZrInZnO TFT. The source and drain region of the TFT was doped by using the Sn:PPC solution. The self-aligned ZrInZnO TFT exhibited a mobility of 20 $cm^2 V^{-1} s^{-1}$, a threshold voltage of 1 V, a subthreshold swing of 0.2 V/decade, and an ON/OFF ratio of 7. These results indicate that the solution-based doping could provide an alternative way to substitute the ion implantation or plasma treatment which are conducted under vacuum for fabrication of the self-aligned oxide semiconductor TFT.

Because the purpose of this study is to realize all-solution-processed self-aligned oxide semiconductor TFT, the last work reports a high quality gate insulator fabricated by the solution process. Here I presented the investigation of a polysilazane-derived SiO_2 gate insulator prepared using a wet-annealing method. The leakage current density of the wet-annealing SiO_2 film was 2.2×10^{-9} A/cm^2 at 1 MV/cm, which was more than one order of magnitude smaller than that of dry-annealed SiO_2 films. The solution-processed ZrInZnO TFT with both reserve staggered and self-aligned structures prepared using the wet-annealed SiO_2 film as the gate insulator exhibited a rather small gate leakage current of less than 7×10^{-11} A/cm^2 at 15 V. The off current was also dramatically decreased owing to the good performance of the wet-annealed SiO_2 gate insulator.

Generally, the present thesis exposes that all-solution-processed self-aligned oxide semiconductor TFT can be realized in order to reduce the total fabrication cost and production energy that are important factor in electronic device manufacturing and in our modern life.

Key words: *self-aligned thin film transistor, oxide semiconductor, solution process, polypropylene carbonate, Sn diffusion.*