Study on a label switch architecture for multimedia telecommunication

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Abstract

A label switch architecture which can support high-speed switching process for variable-length frames is proposed. For treating multimedia traffic in the integrated service network, although variable-length mode has advantages of adapting the properties of various type of traffic dynamically, it relies on software processing generally because of the complexity of its protocols and switching process. So that processing speed is the big handicap of variable-length mode. In the proposed switch the processing throughput can be improved by simplification of processing algorithm and reduction of the percentage of software processing, and by using advanced processor techniques. This paper shows the composition, processing algorithm and the feasibility of this label switch architecture.

1 Introduction

An integrated telecommunication network which can treat multimedia traffic is in great demand in recent years. And multiplexing and switching techniques for the network are also required. As the most fundamental techniques of data communication, merits and demerits of fixed-length mode and variable-length mode have been discussed for a long time. From the view point of multiplexing, a system treating variable-length packets is more flexible than one treating fixed-length packets in dealing with multimedia traffic of various characteristics. However, the switching process of variable-length packets is more difficult because of the complexity of its protocols and switching process. In general, it

relies on software processing; for this reason, processing speed is a big handicap in the variable-length mode.

However, because the quality of telecommunication channels has improved remarkably in recent years, the low-layer protocol has been simplified and it is now sufficient to carry out high-speed processing. Furthermore, remarkable chip technology progress is producing processors and memories with high speed and high throughput one after another. They support today's high-speed routers and switches.

In this research, based on a review of the literature on the multiplexing and switching modes, an variable-length frame format is proposed, and then an architecture design suitable for high-speed switching of variable-length frames is studied.

2 Proposal of AFFTM format

AFFTM (Asynchronous Fast Frame Transfer Mode) is proposed based on the idea that taking advantages of the existing modes as possible as we can to avoid redesign of high-layer protocols. So that the most functions of AFFTM refered from ATM (Asynchronous Transfer Mode).

AFFTM frame format consists of 2Byte flag, 7Byte header and variable-length user payload field from 48Byte to 5KByte. the difference between AFFTM frame header and ATM cell header is that delay-priority field and payload-size field are introduced in AFFTM frame header. For audio traffic the multiplexing delay of AFFTM is same as ATM since the minimal payload size is same as ATM, but in the case of shared frame by several users, AFFTM is more flexible than ATM, because the number of users who share one frame are variable. On the other hand, For data traffic the multiplexing overhead of AFFTM is very small since the maximum payload size is 5KByte. especially, since the payload size is variable, LAN (Local Area Network) packets can be loaded on AFFTM frames directly without segment. So that the quantity of switching process in middle node decrease drastically. By the way, in AFFTM the QoS parameter can be set to each frame, it means that more convenient functions of QoS control can be provided to high-layer whatever the high-layer connection is connection oriented mode or connection less mode.

3 Label switch architecture

A switch treating asynchronous variable-length frames requires to be equipped with the functions of header processing, routing and buffing. The proposed switch processes the headers of frames coming from all input ports in one shared memory, at the same time stores the bodies of those frames at one common memory area which is called the frame yard. A switch label is pasted in front of each header processed in the switching stage, so the frames can go to appropriate output buffers automatically in the output stage, which can be called automatic routing. The output part of the switch is a cross-point output buffer array, and output order is decided here based on the priority and the waiting time of the frames.

Thus, the ideal switching which has no internal collision can be realized by combining output buffer and shared memory, and the percentage of software processing can be reduced by using cross-point output buffer array that is performed by hardware. Furthermore, the application of a multi-thread processor, not only enhance the throughput of software processing, but keep the order of header processing and the order of body saving strictly as well. therefore, all of the bodies of frames which come from all input ports and have different lengthes can be saved in one frame yard. The memory occupency rate of the frame yard is high because it performs as circle buffer mode. Output priority control can be performed by hardware because of utilizing the label technique, so that QoS control becomes easy and efficient. The proposed switch can also regulate output policy between priority and fairness with an arbitration logic. By the way, the switch structure can also support multicast service very easily because of utilizing the label technique. Moreover, input buffering must be carried out since input frames are in different lengths. In the proposed switch, a threshold is set up as a processing unit, and different input approaches are taken according to frame length. This method will reduce the difference of the input time of frames and shorten frame wating time. In the switch architecture constituted from such an idea, the switching process algorithm is very simple, and the quantity of buffers is not very large either. The structure of both the hardware and software of this switch can be easily implemated.

4 Simulation for verifying the switch function

Three simulations are performed to verify the function of the switching process algorithm and to examine the feasibility of the proposed switch architecture.

In the simulation about basic processing performance, the switch processing program based on MIPS processor is run on a software simulator named SPIM[1], and processing throughput of the switch is evaluated by the number of execution steps on the assembly language level. The improvement of header process efficiency of multi-thread mode is verified by comparing with single-thread mode and plural-thread sequential execution mode.

In the simulation about input buffering, at first, the threshold is examined through evaluation of two input transmission method, the I/O processor direct control mode for small frames whitch are shorter than threshold and DMA (Direct Memory Access) control mode for large frames which are longer than threshold. Then, the queue-length in the input buffer and the waiting time of frames are examined by simulation.

In the simulation about output buffering, problems such as the operation of output priority control mechanism, delay caused in the switch, and buffer size, are examined by a event-driven simulation program.

According to the results of these simulations, when the proposed switch is constituted using the present high performance MIPS processors, it is possible to satisfy the requirements in both speed and throughput of basic interface of B-ISDN (Broadband Integrated

[1]SIPM is a free software simulator written by professor James R.Larus of Wisconsin University, which is used to simulate the MIPS R2000/R3000 processor architecture.

Service Digital Network).

5 Conclusion

this paper proposed a label switch architecture which can support high-speed switching process for variable-length frames, and verified the feasibility of it by simulation.

Although asynchronous variable-length mode is inferior than fixed-length mode regarding processing speed, it is also attractive because it is more flexible with various multimedia traffic. In switching process treating variable-length frames, it is thought that simplifying the processing algorithm and reducing the percentage of software processing will be effective approaches in order to enhance processing speed.

References

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