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Characterization of spin-orbit coupling in gated wire structures using $Al_2O_3/In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ inverted heterojunctions

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Gated parallel wire structures obtained from inverted-modulation-doped heterojunctions made of high-In-content metamorphic InGaAs/InAlAs were investigated. The narrowest wire width was found to be ~190 nm made using electron beam lithography and reactive ion etching. Magneto-transport was measured at low temperatures. Weak anti-localization and suppression with applied negative gate voltages were observed in low-mobility wide wires (1360 nm), which were considered for a two-dimensional system. The dependence on the gate voltage of spin-orbit coupling parameters was also obtained by fitting. The parameters decreased as the negative gate voltages increased. The trend might originate not from the electron system at the InGaAs/InAlAs interface but from the other electron system accumulated at the Al_2O_3/InGaAs interface, which can also contribute to conductivity. In high-mobility narrow wires (190 nm), which are close to a one-dimensional system, weak anti-localization peaks were still observed, indicating strong spin-orbit coupling. In addition, the critical widths of wires corresponding to zero conductance were estimated to be <100 nm. Therefore, our metamorphic modulation doped heterojunctions seem suitable for smaller spin-FETs. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4963752]

I. INTRODUCTION

Much attention has been paid to semiconductor spintronics[1] from the viewpoints of their fundamental physics and of their future device applications. Even though dilute magnetic semiconductors[2,3] are the typical base materials, obtaining high-purity materials is usually not possible due to the magnetic impurities. To obtain base materials with high-purity, non-magnetic semiconductor heterojunctions without any magnetic impurities have also been studied. In particular, narrow-gap III–V semiconductor modulation-doped heterojunctions (MDHs) including InAs- and InSb-based materials have been intensively studied[4–10] because they exhibit high electron mobility and large Rashba spin-orbit coupling (SOC) induced by structure-inversion asymmetry (SIA).[11] The Rashba SOC performs an important role in Datta-Das spin field effect transistors (spin-FETs),[12] which are one of the target devices in non-magnetic semiconductor spintronics. Fabrication and characterization of one-dimensional (1D) channels from the MDHs are very important to establish the fundamental techniques for the spin-FETs. This is because the spin relaxation caused by the combination of the Rashba SOC and the elastic scattering is expected to be suppressed in the 1D channels due to the restriction of trajectories. Because the suppression of spin relaxation is very important for the spin-FET applications, some groups have reported an increase in the spin-orbit relaxation time due to a reduction in the effective wire width[13] or the creation of a persistent spin helix[14] in wire structures using pseudomorphic InGaAs MDHs on InP (001), which show a strong Rashba SOC.

In this study, we chose metamorphic InGaAs MDHs on GaAs(001) as starting materials that also show a strong Rashba SOC.[15] Using electron beam lithography (EBL) and reactive ion etching (RIE), we fabricated parallel wire structures from the MDHs. Later, we formed an Al_2O_3 gate insulator on the parallel wire structures using atomic layer deposition (ALD) followed by the gate electrode formation. We electrically measured the magneto-transport of the gated parallel wire structures at low temperatures.

II. SAMPLE PREPARATION AND MEASUREMENT SETUP

The inverted high-In-content InGaAs MDHs were metamorphic grown on a semi-insulating GaAs (001) substrate using conventional molecular beam epitaxy with the InAlAs step graded buffers (SGBs)[15] as shown in Fig. 1. The MDHs typically consist of a 60-nm-thick InGaAs channel (top), a 20-nm-thick InAlAs spacer, a Si delta-doping layer, a 200-nm-thick InAlAs barrier, and InAlAs SGBs (bottom). The nominal In-content is 0.75 for active layers (channel, spacer, and barrier). In this study, we used two different wafers showing relatively high electron mobility (HM) and low electron mobility (LM).

On the wafers, we first prepared Ti masks having parallel wire structure patterns using EBL and lift-off. Then, we utilized inductive-coupled-plasma RIE with CH_4/H_2 to transfer the patterns to the wafers. Later, the Ti masks were completely removed by diluted HF dipping. Figure 2(a) shows a scanning electron microscope (SEM) image of a

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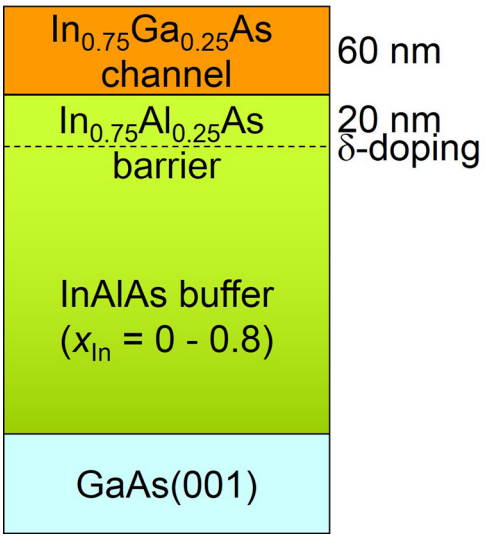

FIG. 1. Schematic layer structure of inverted modulation-doped-heterojunctions made of high-In-content metamorphic InGaAs/InAlAs. In content of active layers was ~75%.

fabricated wire having ~190 nm width just after the Ti removal. The smooth top surface of the wire can be seen. The wire width ranged from 190 to 1360 nm. The number and length of parallel wires were 25 and 100 μm, respectively. The reason which we prepared parallel and significantly long wires is to suppress conductance fluctuations and ballistic effects which can be seen in single quantum wires. After the AuGeNi Ohmic electrode formation using EBL and lift-off and annealing with Ar/H_2, we utilized ALD of ~30-nm-thick Al_2O_3 with trimethylaluminum and water to form a gate insulator followed by the Ti/Au gate electrode formation using EBL and lift-off. Finally, we carried out the Ti/Au pad formation by using photolithography and lift-off. Figure 2(b) shows a schematic cross-section of a completed wire structure following the fabrication process.

Electrical measurements were performed in a ^{4}He cryostat with a superconducting magnet and standard AC lock-in amplifiers. Typical current levels were from ~100 nA to ~1 μA. The applied magnetic field was perpendicular and up to 8 T. The typical measurement temperature was ~1.7 K.

III. RESULTS AND DISCUSSION

First, we discuss the LM wide wire case. Figure 3 shows the magneto-conductivity curves of 1360 nm wires with applied gate voltages from −1 to −5 V. The estimated mean

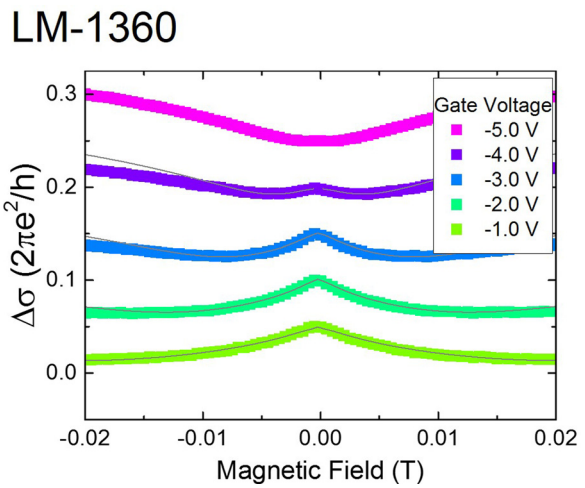

FIG. 3. Magneto-conductivity curves of LM-1360 with various applied gate voltages. Gray curves are fitting results.

free path from the sheet electron density and the mobility by the magneto-resistance oscillation is 280 nm at 0 V, which is significantly shorter than the wire width. Therefore, this case can be considered to be a two-dimensional (2D) system case. Conductivity peaks at zero magnetic field, which are so called weak anti-localization (WAL) peaks, can be seen clearly at small negative gate voltages. As negative gate voltages increase, the WAL peaks are suppressed, and finally no WAL peaks can be found. The WAL peaks are considered to be the evidence of SOC. To fit the WAL curves using a model for a 2D system,[16] we estimated the SOC parameters, as shown in Fig. 4. The dependency of the SOC on the gate voltages can be seen clearly, and the estimated SOC parameters around 10^{-11}–10^{-12} eVm are typical in the InGaAs MDHs. However, the trend is unlike 2D systems in inverted MDHs that have doping on the substrate side; instead, it seems like 2D systems in normal MDHs that have doping on the surface side.[17] Although this layer structure is an inverted MDH, the narrow-gap InGaAs channel directly faces a wide-gap Al_2O_3 gate insulator. Therefore, if the wide-gap Al_2O_3 gate insulator is doped negatively, conductive electron accumulation can take place at the Al_2O_3/InGaAs interface. Interstitial Al atoms and dangling bonds of Al in Al_2O_3 have been predicted to act as donors.[18] Figure 5 shows the simulated band profiles and distributions of electrons for various gate voltages with the assumed donor densities of 3.0×10^{12} and 1.5×10^{12} cm^{-2} in Al_2O_3 and InAlAs, respectively. In the simulation, the surface barrier height of Al_2O_3 is 5.75 eV,

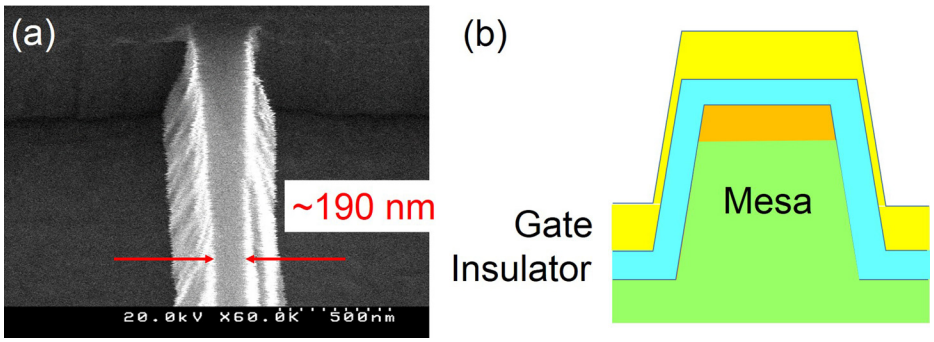

FIG. 2. (a) Scanning electron microscope image of the narrowest wire structure. (b) Schematic cross-section of wire structure.

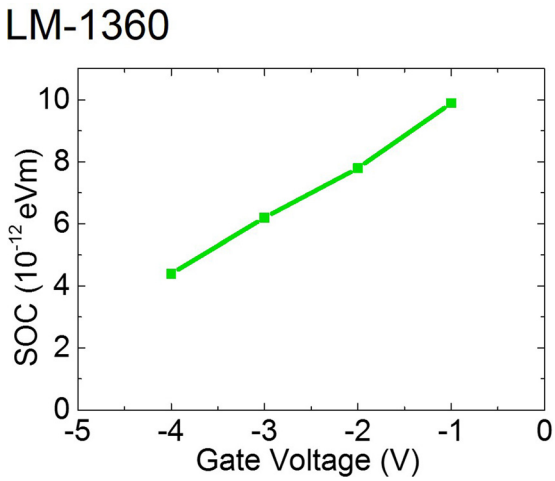

FIG. 4. Spin-orbit coupling parameters in LM-1360 as a function of gate voltages estimated from fitting of weak anti-localization behaviors.

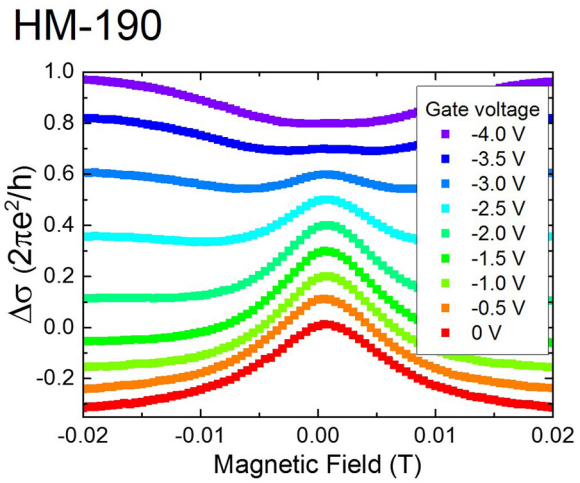

FIG. 6. Magneto-conductivity curves of HM-190 with various applied gate voltages.

and the range of gate voltages is from 0 to −3 V. In the figure, the direction of the electric field, i.e., SIA at the Al_2O_3/InGaAs interface, seems opposite to that at the InGaAs/InAlAs interface. Thus, the SIA at the Al_2O_3/InGaAs interface becomes similar to not the inverted but the normal MDHs. If the electron accumulation at the Al_2O_3/InGaAs interface contributes substantially to conductivity, this trend in the SOC parameters against gate voltage seems reasonable. We need further analysis especially around the interface to clarify the electron accumulation experimentally.

Next, we discuss the HM narrow wire case. Figure 6 shows the magneto-conductivity curves of 190 nm wires with the applied gate voltages from 0 to −4 V. The estimated mean free path is 350 nm at 0 V, which is longer than the wire width. Therefore, the system is different from a 2D system and close to a 1D system. The WAL peaks still can be seen clearly at small negative gate voltages, and the amplitudes are relatively larger than those in the LM wide wire case. The behavior is unlike the previous reports using the pseudomorphic InGaAs MDHs on InP (001),[13,14] and we can simply mention that the SOC of the HM narrow wire seems significantly strong. In addition, similar to the LM wide wire case, the WAL peaks are suppressed more as the negative gate voltages increase, and finally no WAL peaks could be found. Similar WAL dependence on gate voltages has been found in 1D InAs nanowires.[19] Because the InAs surface can have an electron accumulation layer,[20] the SIA at the 1D InAs nanowire side surface[19,21] can be similar to that not at the InGaAs/InAlAs interface but at the Al_2O_3/InGaAs interface. The similarity also supports the possibility of electron accumulation at the Al_2O_3/InGaAs interface.

Finally, we plotted normalized conductance values as a function of wire width in Fig. 7. On considering the discussion in Fig. 5, no depletion region was expected; however, we obtained non-zero critical widths of wires. The critical widths of wires corresponding to zero conductance were estimated to be 36 and 98 nm at gate voltages of 0 and −4 V, respectively. The results indicate some RIE damages in the side walls of wire mesas, which induce electron traps and result in the compensation of electrons provided from Al_2O_3 by the traps. These widths are relatively smaller than those in the previous reports using the pseudomorphic InGaAs MDHs on InP (001).[13,14] Therefore, we can emphasize that our metamorphic InGaAs MDHs on GaAs (001) are suitable

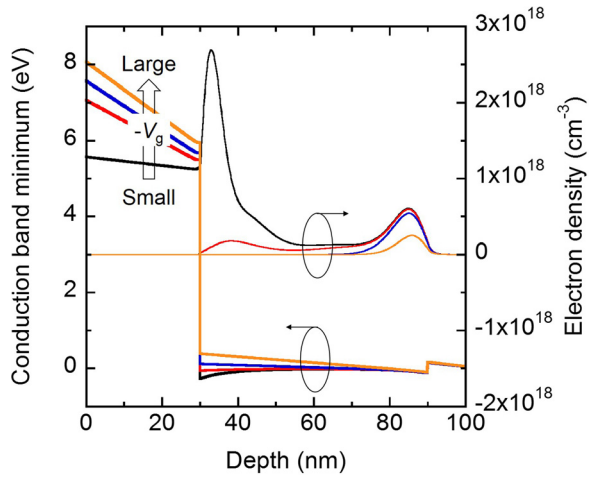

FIG. 5. Simulated conduction band profiles and curves of electron distribution with assumed interface donors in Al_2O_3.

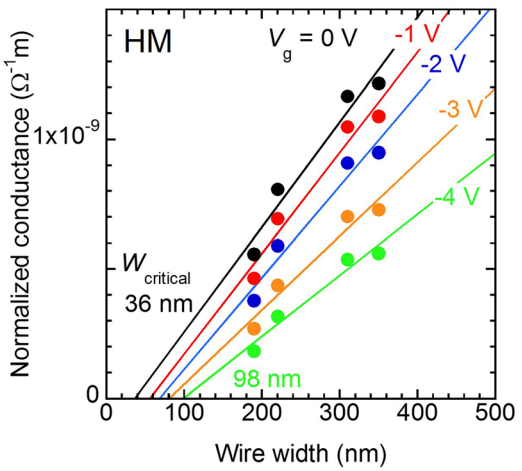

FIG. 7. Normalized conductance values from the HM wafer as a function of wire width.

for spin-FETs with smaller sizes because of strong SOC and small critical width.

IV. SUMMARY

We fabricated gated parallel wire structures having widths ranging from 190 to 1360 nm in the inverted MDHs made of high-In-content metamorphic InGaAs/InAlAs using EBL, RIE, and ALD. The narrowest wire width was found using SEM. We measured the magneto-transport of these gated parallel wire structures at low temperatures. In the LM wide wire case, which can be considered to be a 2D system case, the WAL peaks and their suppression were clearly observed with applied negative gate voltages. By fitting the WAL curves, the SOC parameters were estimated, and they decreased as negative gate voltages increased monotonically. This trend against gate voltage might originate from electron accumulation at the Al_2O_3/InGaAs interface. In an HM narrow wire case, which is different from 2D and close to 1D, WAL peaks were still clearly observed, indicating strong SOC. In addition, the critical widths of wires corresponding to zero conductance were estimated to be <100 nm. Therefore, our metamorphic InGaAs MDHs on GaAs (001) seem suitable for spin-FETs with smaller sizes because of the strong SOC and small critical width.

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