氏　　　　　　　名	CUADROS ROMERO Francisco Javier
学　位　の　種　類	博士(情報科学)
学　位　記　番　号	博情第 356 号
学 位 授 与 年 月 日	平成 29 年 3 月 24 日
論　　文　　題　　目	Mapping Functions That Maximize Mutual Information for Decoding LDPC Codes
論 文 審 査 委 員	主査　Brian M. Kurkoski　JAIST　Associate Professor
	Tadashi Matsumoto　JAIST　Professor
	Mineko Kaneko　JAIST　Professor
	Hideki Yagi　Univ. Elect. Comm.　Associate Professor
	Dirk Wübben　Univ. of Bremen　Senior Researcher

論文の内容の要旨

Low-density parity-check (LDPC) codes have been reported to perform close to the channel capacity. LDPC decoders and channel quantization algorithms are usually implemented using floating point simulations in Matlab/C or another programming languages. Once these algorithms are carefully optimized, the next step is to carry out their corresponding hardware implementation in a very-large-scale integrated (VLSI) circuit. In such implementation, LDPC decoders and channel quantization algorithms are converted to a fixed-point representation. For example, the offset min-sum (OMS) algorithm for decoding LDPC codes uses real-valued operations: addition, min. But the channel and decoder messages are usually quantized to a bit width of 4 to 7 bits, depending on the performance/complexity tradeoff. In this research, floating-point algorithms are not used. Instead, the central method is “direct design” of VLSI circuits for LDPC decoders and channel quantizers.

The objective of this research is to design LDPC decoder schemes and channel quantizers that can be implemented in VLSI circuits. For LDPC decoders, the goal is designs that achieve high throughput (a few iterations) and low gate count (a few bits per message). For channel quantization, the goal is to find an optimal quantization scheme, for a fixed bit width, even when the error distribution model is based only on sample data.

In this dissertation, we have developed a technique where the LDPC decoders and channel quantization implementations, including quantization of messages, are designed using only the

probability distribution from the channel. Given a probability distribution, our method designs a lookup table (LUT) that maximizes mutual information, and LUTs are implemented directly in VLSI circuits. This is the “max-LUT method”.

The proposed lookup tables are sometimes referred as mapping functions. The mapping functions we propose are used for channel quantization and for message-passing decoding of LDPC codes. These mapping functions are not derived from belief-propagation decoding or one of its approximations, instead, the decoding mapping functions are based on a channel quantizer that maximizes mutual information. More precisely, the construction technique is a systematic method, which uses an optimal quantizer at each step of density evolution to generate message-passing decoding mappings.

In a simple manner, the design of LDPC decoders by maximization of mutual information is analogous to finding non-uniform quantization schemes where the quantization can vary with each iteration.

The proposed decoding mapping functions are particularly well suited for data storage applications, because they can be designed from non-parametric and irregular noise distributions. Though finite-length simulations show that the proposed decoding mappings functions present good performance for a variety of code rates.

Numerical results show that using 4 bits per message and a few iterations (10—20 iterations) are sufficient to approach the error-rate decoding performance of full (without quantization) sum-product algorithm (SPA), less than 5--7 bits per message typically needed to perform around 1 dB away from the error-rate decoding performance of full SPA.

Another result of this research is that the construction technique for the mapping functions is flexible since it can generate maps for arbitrary number of bits per message, and can be applied to arbitrary binary-input memoryless channels.

Keywords: LDPC decoding, mapping functions, lookup tables, quantization, sum-product algorithm.

論文審査の結果の要旨

This dissertation describes a method for quantizing channels by maximizing mutual information. This is applied to the quantization of messages in belief-propagation decoders for low-density parity-check (LDPC) codes. Bit-error rates obtained using 4 bits per message was similar to, or in some cases exceeded, that of floating-point belief-propagation. LDPC codes are a type of error-correcting code which is now widely used in a variety of communication systems, and are typically implemented in VLSI. Javier's work should influence VLSI implementations, because the proposed method demonstrates that the number of bits per message can be reduced below current methods. A possible consequence is reduced power consumption for battery-powered radio receivers found in smartphones.

The committee judged the dissertation to be solid, to be of high academic level, and to posses a high degree of novelty. It has a theoretical component, yet has the possibly to impact error-correcting codes in practice. It led to a published IEEE journal paper and a top-level conference publication.

All of the committee members evaluated "A" and there was strong agreement that the quality of the dissertation was excellent, and approved awarding the doctoral degree to Francisco Javier Cuadros Romero.