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Description	

Japan Advanced Institute of Science and Technology

Controllable threshold voltage in organic complementary logic circuits with an electron-trapping polymer and a photoactive gate dielectric layer

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ABSTRACT

We present controllable, highly stable complementary organic transistor circuits on a PET substrate, using a photoactive dielectric layer of 6-[4'-(*N*,*N*-diphenylamino)phenyl]-3-ethoxycarbonylcoumarin (DPA-CM) doped into poly(methyl methacrylate) (PMMA) and an an electron-trapping layer of poly(perfluoroalkenyl vinyl ether) (Cytop). Cu was used for a source/drain electrode in both the *p*-channel and the *n*-channel transistors. The threshold voltage of the transistors and the inverting voltage of the circuits were reversibly controlled over a wide range under a program voltage of less than 10 V and under UV light irradiation. At a program voltage of −2 V, the inverting voltage of the circuits was tuned to be at nearly half of the supply voltage of the circuit. Consequently, an excellent balance between the high and low noise margins (NM) was produced (64% of NM_H and 68% of NM_L), resulting in the maximum noise immunity. Furthermore, the programmed circuits showed high stability such as a retention time over 10^5 s for the inverter switching voltage.

KEYWORDS: organic field-effect transistors, controllable threshold voltage, organic complementary circuit, CMOS, long retention time, low program voltage.

Introduction

Organic transistor circuit technology is crucial for various lost-cost, large-area flexible–applications including logic gates, nonvolatile memories, analog-to-digital converters, radio frequency identifier tags, active sensors, signal amplifier, and microprocessors.[1–7] To construct integrated circuits using organic thin-film transistors (OTFTs), it is very important to control the transistor threshold voltage (V_{th}). A change in the V_{th}, to a lower value, leads to a decrease in power consumption.[8] Furthermore, the control of the V_{th} permits adjusting the switching voltage of each device in the circuits and minimizes manufacturing variation.[6] In the complementary metal-oxide-semiconductor (CMOS) circuit, the switching voltage of an inverter (V_M) may be close to either the ground or the voltage supply, due to a difference in the V_{th} and the field-effect mobility (μ) parameters between the *p*-channel OTFT (pOTFT) and *n*-channel OTFT (nOTFT). The V_M then causes the high and low noise margins of the inverter to become unbalanced. When the V_M is tuned to exactly half of the voltage supply, the circuits provide the maximum noise immunity and work more reliably.[9–11] Thus, achieving a controllable V_M in the complementary circuit is a key to realize a robust organic digital circuit, which can be accomplished by means of tuning the V_{th}.[9]

A number of methods have been demonstrated to control the V_M in an organic transistor circuit, such as varying a doping concentration of Au nanoparticles (NPs)[12], inserting polar self-assembled monolayers (SAMs)[10,11,13], modifying the gate electrode[14], or the UV/ozone treatment of the dielectric layer.[15] However, the V_M shift by the above-mentioned method can be accomplished through the fabrication processes i.e., the V_M cannot be tuned after the circuit fabrication.[10−15] Dynamic control of the V_M, after the circuit fabrication, can be achieved by introducing floating-gate structures with a program voltage below 10 V.[6,16,17] Such a low-program voltage, however, was achieved with the expense of that the programmed V_M readily shifted back to its initial value[6] because the stored charge in the floating-gate leaks away.

We have recently demonstrated the controllable V_M in organic CMOS circuits, based upon the electron-trapping at the interface between Cytop (poly(perfluoroalkenyl vinyl ether)) and SiO_2.[8,18,19] Although, the interfacial electron-trapping at the double gate dielectric is highly promising, for the long-term stability of the tunable organic CMOS circuits, high voltage, up to 80 V, is required to control the V_M. The reduction of the switching program voltage is still necessary for practical applications. Recently, we have produced a low-voltage tunable V_{th} of OTFTs using a photoactive gate dielectric layer, which is composed of the layers of 6-[4'-(*N*,*N*-diphenylamino)phenyl]-3- ethoxycarbonylcoumarin (DPA-CM) doped into poly(methyl methacrylate) (PMMA) and an electron-trapping polymer of Cytop.[20] In these OTFTs, the programming voltage to tune the V_{th} can be reduced to less than 10 V.

Furthermore, in order to fabricate an organic complementary circuit, the pOTFT and the nOTFT are required to be embedded onto one substrate. For the transistor element operations, the high work-function metal for pOTFTs and the low work-function metal for nOTFTs are employed as a source/drain electrode for lowering the charge injection barrier. However, the complexity of the electrode patterning of the two metals onto one substrate limits the development of the organic complementary circuits, which may be one of the reasons for the pseudo-CMOS configuration that is widely used in the organic transistor circuit.[12–15] Recently, it has been reported that the use of Cu as a source/drain electrode can improve the performance of both pOTFTs and nOTFTs.[21–23] Despite the development of such high-performance OTFTs using a Cu electrode, the application of the Cu electrode to the complementary circuit has not been tested.

In this work, we realize low-program voltage, highly stable and a controllable V_M in complementary organic logic circuits on a flexible polyethyleneterephthalate (PET) substrate. By using Cu as source/drain electrodes, we can fabricate organic complementary circuits based upon pOTFTs and nOTFTs. By introducing a photoactive gate dielectric layer, composed of the layers of DPA-CM doped into PMMA, and an electron-trapping polymer of Cytop, the V_{th} in both of the pOTFTs and nOTFTs can be reversibly controlled over a wide range at a program voltage of less than 10 V. As a result, the V_M was tuned from 6.2 to 16.9 and 19.5 V after programming the pOTFTs and nOTFTs, respectively. Nearly an ideal value of the V_M, and the resulting maximum noise immunity was observed at program voltages of −2 V for the pOTFTs. In addition, the tuned V_M continued to be stable after 10^5 s.

Experimental Section

The chemical structures of Cytop and DPA-CM and the schematic illustration of the organic inverter circuit are shown in Figure 1a. PET substrates coated with a patterned 150-nm gate electrode layer of indium tin oxide (ITO) were cleaned by ultrasonication (in acetone for 5 min, in detergent for 10 min, twice in pure water for 5 min, and in isopropanol for 10 min) and subjected to a UV-O_3 treatment. PMMA (Aldrich, Mw = 97,000) and DPA-CM[24] (synthesized in our lab), with a 10:1 molar ratio of a monomer unit of PMMA to DPA-CM, were dissolved in chloroform (the concentration of PMMA was 2 wt%). A 330-nm-thick layer of the PMMA:DPA-CM composite was prepared onto the ITO by spin-coating of the solution at 1500 rpm for 60 s, and dried on a hot plate at 70°C for 60 min to remove the residual solvent. A 10-nm-thick Cytop layer (CTX-809 AP2, Asahi Glass) was then spin-coated onto the PMMA:DPA-CM layer at 1000 rpm for 60 s using a 0.5 wt% Cytop solution (CT-Solv. 180), and heated at 70°C for 60 min.

A fullerene (C_{60}) layer (50 nm) for the nOTFTs and a pentacene layer (50 nm) for the pOTFTs were thermally deposited through shadow masks onto the Cytop layer at a pressure of 1.2 × 10^{-6} Torr. Finally, a 50-nm-thick layer of Cu was vacuum-deposited through a shadow mask, at a base pressure of 2 × 10^{-5} Torr, to form the source-drain electrodes (Channel length L = 50 μm, channel width W = 2000 μm) and interconnects.

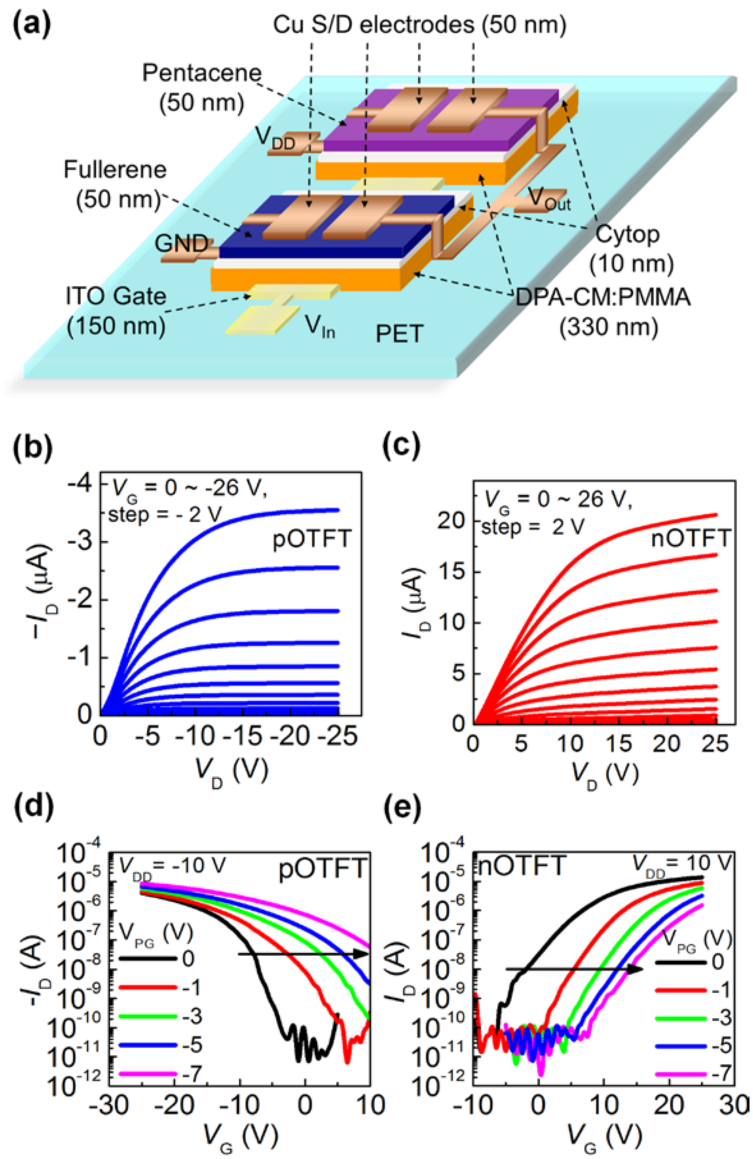

Figure 1. (a) Chemical structures of DPA-CM and Cytop and schematic layout of organic circuit. Output characteristics of (b) pOTFT or (c) nOTFT. Transfer curves of (d) pOTFT or (e) nOTFT measured at initial and after programming. V_G means gate voltage. Programming operations

were done by applying V_{PG} for 1 s under UV light intensity of 3.94 mW/cm^2 while source and drain electrodes were grounded.

Electrical measurements of the OTFTs and complementary inverters were carried out with a Keithley 4200 semiconductor characterization system in a dry nitrogen atmosphere at room temperature. During the programming and erasing, UV light (365 nm) was irradiated from the PET substrate with an Omron ZUV UV irradiator. The UV light intensity was measured by a Coherent FieldMax II-TO laser power meter.

Results and Discussion

The drain current (I_D) and the drain voltage (V_D) characteristics of the pOTFTs and nOTFTs are shown in Figures 1b and 1c, respectively. The pentacene pOTFTs exhibit a hole effect-field mobility of 0.18 cm^2 V^{-1} s^{-1} and a V_{th} of −7.4 V. The C_{60} nOTFTs show an electron effect-field mobility of 0.73 cm^2 V^{-1} s^{-1} and a V_{th} of 1.7 V. The obtained hole or electron mobilities in our circuit devices with a Cu source/drain electrode are similar to those in the pentacene OTFT with an Au source/drain electrode, or in the C_{60} OTFT with an Al source/drain electrode,[25] suggesting efficient electron and hole injections at the interfaces of the pentacene/Cu or the C_{60}/Cu.

Figures 1d and e show the transfer characteristics of the pOTFT and the nOTFT elements measured after applying a program gate voltage (V_{PG}) for 1 s, under UV light intensity of 3.94 mW/cm^2. The UV absorption spectra of the PMMA:DPA-CM composite layer and pentacene has been previously reported, where the strong UV absorption of DPA-CM are shown.[26] In the paper, we have also confirmed that the UV light irradiation was negligible influence on the device performance. To explain the operation mechanism of programming and erasing, schematic representation of program and erase treatments are shown in Figure 2. Under the UV light irradiation, singlet and triplet states of DPA-CM are generated and then converted into a charge-separation state.[24] When an external electric field is applied to the DPA-CM:PMMA photoactive layer under the UV light irradiation, the charge-separation states of the DPA-CM molecules are converted into free electrons and holes.[26] Under the application of the negative V_{PG} (denoted as programming), the free electrons migrate and are subsequently trapped at the Cytop/DPA-CM:PMMA interface (Figure 2a). The interfacial trapping originates from the electret property of the Cytop material[27,28] as discussed in our previous reports.[8,18] The trapped electrons induce additional holes in the *p*-channel or deplete the electrons in the *n*-channel, leading to the positive shifts of transfer curves in both devices as shown in Figures 1c and 1d. Conversely, when the positive V_{PG} is applied (denoted as erasing), the free holes migrate to the Cytop/DPA-CM:PMMA interface (Figure 2b). The trapped electrons at the interface were removed and/or neutralized by the holes. As a result, the V_{th} has completely returned to the initial position.

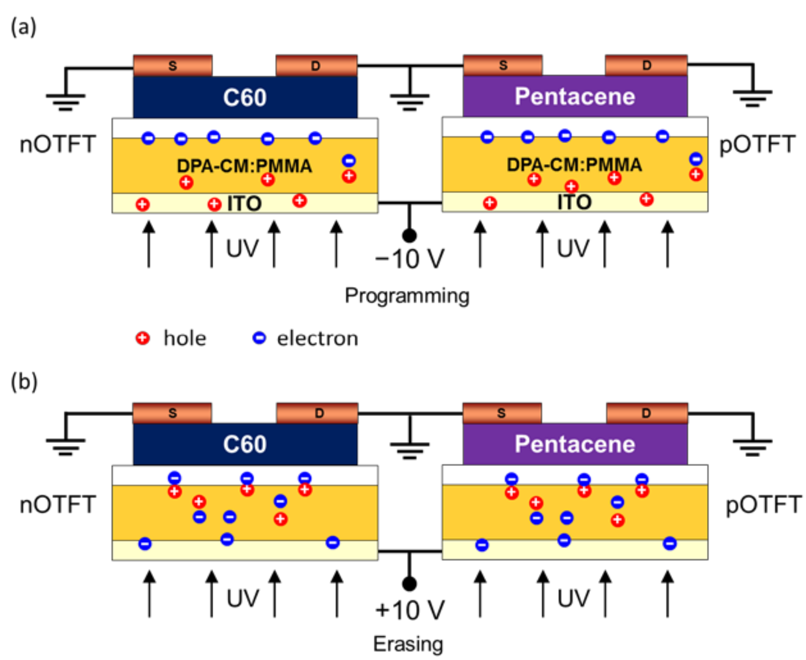

Figure 2. Schematic representation of program and erase state, the holes and electrons migrate in opposite direction according to the electric field. (a)In the programming treatment, the negative

gate voltage is applied to the gate electrode under the UV light irradiation. (b) In the erasing state, the positive gate voltage is applied to the gate electrode under the UV light irradiation.

The reversible shifts in the V_{th} as functions of the V_{PG} voltage are presented in Figure 3. The V_{th} was reversely controlled from −7.4 to +16.7 V for the pOTFTs and from +1.7 to +30.6 V for the nOTFTs. In addition, the changes in the V_{th} as functions of the UV light intensity and the applied time of V_{PG} are investigated (Figure S1). The experimental conditions to obtain the program/erase state were optimized by the dependence of V_{th} on each condition such as the V_{PG} voltage, the UV light intensity, and the applied time. Based on the dependencies in Figures 3 and S1, we define the experimental conditions as the application of a V_{PG} of −10/+10 V for 1 s under a light intensity of 3.94 mW/cm^2. Without the photoactive layer, the electrons have to be injected into the interfacial Cytop/SiO_2 trap site from organic semiconductors, which required large program voltages.[8,18] By replacing the SiO_2 layer with a photoactive dielectric layer of DPA-CM:PMMA, the electrons were internally provided the trap site from the photoactive dielectric, resulting in the significant reduction of program voltages.

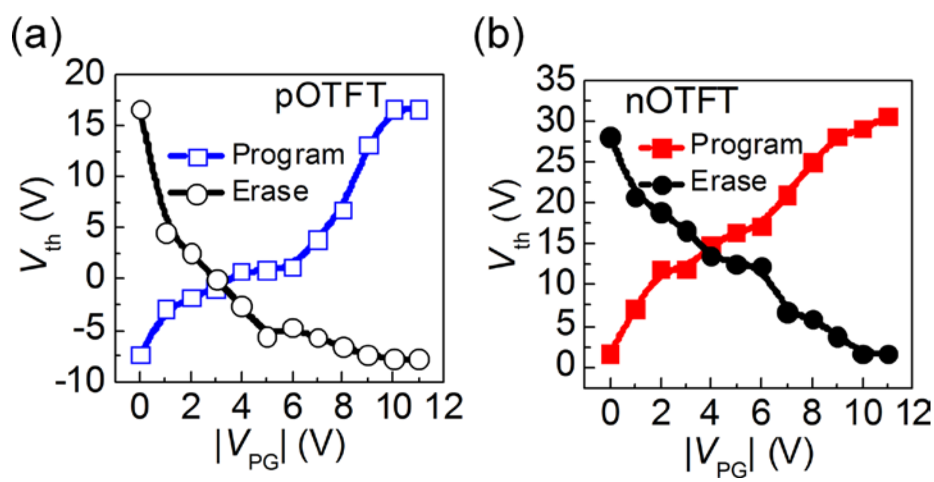

Figure 3. V_{th} change of (a) pOFET or (b) nOFET as function of V_{PG} with applied time of 1 s under UV light intensity of 3.94 mW/cm^2. V_D values were set to be −10 V for pOFET and 10 V for nOFET in all transfer curve measurements.

In other controllable organic inverter systems,[12–15] the circuits were mainly built from unipolar pOFETs. However, the complementary circuit, which consists of both the pOTFT and nOTFT, have many advantages over the unipolar circuit configuration i.e., a simpler circuit design, better noise margins, and lower power consumption.[9,16] The V_{th} controlling achieved in the pOTFT and nOTFT elements allows us the construction of a high performance complementary logic circuit. Figure 4 shows the electrical characteristics of the initial complementary inverter. For each voltage transfer characteristic (*VTC*) curve, when an input voltage (V_{In}) was varied from 0 to the supply voltage V_{DD}, the output voltage (V_{Out}) swings from V_{DD} to 0 V, indicating an obvious inverting operation.[8–16] The voltage gain, defined as $-dV_{Out}/dV_{In}$, is summarized in Figure 3b. The obtained maximum gain at a certain V_{DD} is similar to that of previous organic inverters.[2,3,12,15,29] The V_M values were estimated to be 3.4, 5, 6.2, 7.5 and 10.3 V from a V_{DD} of 15, 18, 20, 22, and 25 V, respectively. The V_M of the initial logic circuit did not appear at the theoretical point of ½V_{DD}, because the circuit devices have differences in the V_{th} and the μ parameters of the pOTFT and nOTFT. As mentioned above, the V_M at exactly a half that of the voltage supply, is ideal for a reliable operation of the circuit.

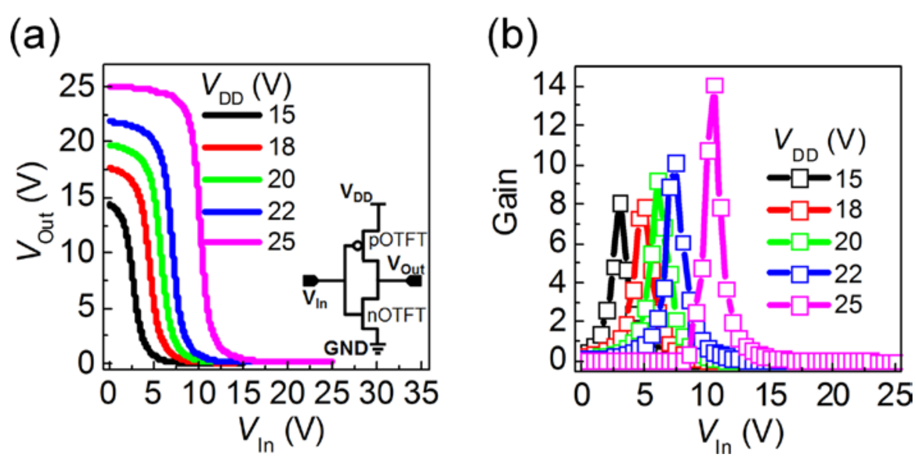

Figure 4. (a) *VTC* and (b) corresponding gain of initial circuit at various V_{DD} values. Inset of (a) presents equivalent circuit of organic complementary inverter.

The tunable behaviors of the organic inverter circuit at V_{DD} = 20 V are shown in Figure 4. Each *VTC* curve was taken after programming the pOTFT (Figure 5a) or the nOTFT (Figure 5b). When one of the circuit devices was programmed, its complementary device was kept at the initial state. As shown in Figure 5, the application of a negative V_{PG} caused the systematic shift of the V_M to a positive direction. The V_M was tuned over a wide range from 6.2 to 16.9 V after programming the pOTFT (Figure 5c), and from 6.2 to more than 19.5 V after programming the nOTFT (Figure 5d). By choosing a V_{PG} of –2 V for the pOTFT or the nOTFT, we achieved a V_M of 9.8 V in both cases, which is very close to ½ V_{DD} = 10 V. Hereafter, we employed the programming of the pOTFT with the V_{PG} of –2 V for the logic circuit because of lower V_{th} values in both of the pOTFT (−1.8 V) and nOTFT (1.7 V), as shown in Figures 3a and b.

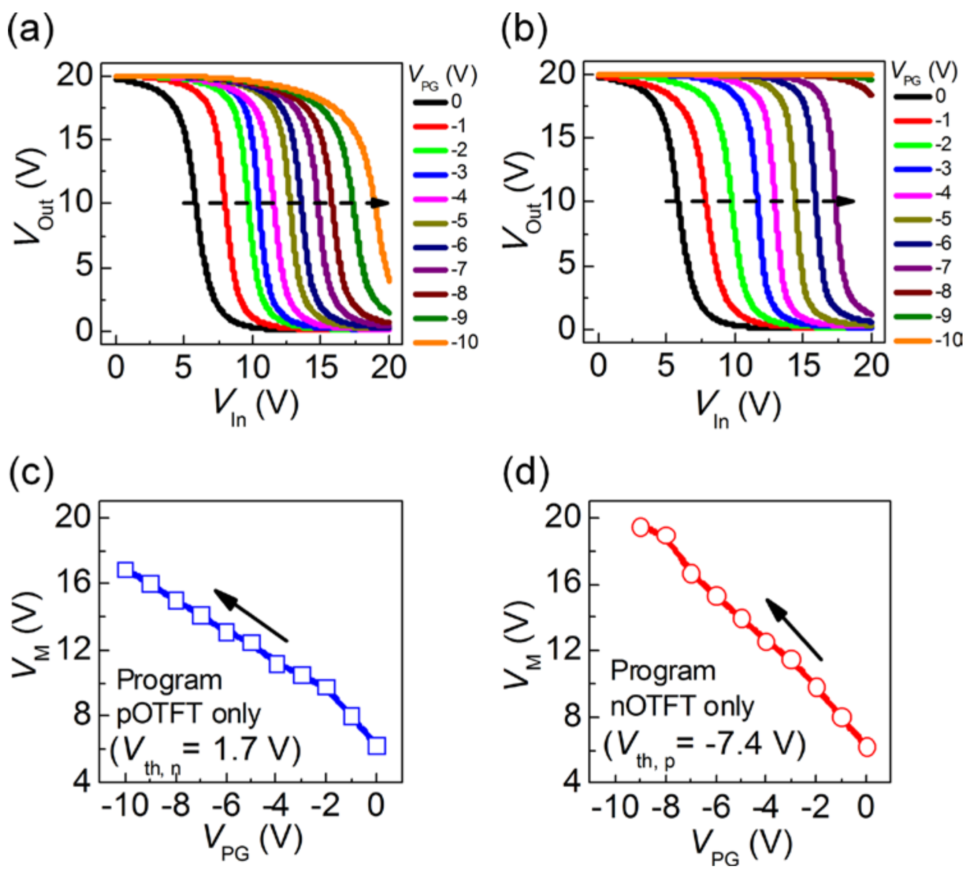

Figure 5. Tunable *VTC* of circuit after programming (a) pOTFT and (b) nOTFT. Changes of V_M of circuit as function of V_{PG} voltage for (c) pOFET and (d) nOFET.

An electrical noise immunity of a digital logic circuit is measured as the noise margin (*NM*), which is the maximum noise signal that can be superimposed onto a digital signal without changing the function of the circuit.[15] Figure 6 shows the analyses of the *NM* at high (NM_H) and low (NM_L) logic levels, from initial and programmed *VTC*s, where the *NM* was determined by the maximum slide length of a square that fits between the *VTC* and its inverse.[9,10] In the initial state of the circuit, there was no balance between the NM_L and the NM_H, where the NM_L (3.1 V = 31% of ½ V_{DD}) and the NM_H (8.4 V = 84% of ½ V_{DD}) were observed. In addition, a NM_L of 3.1 V was narrow and close to the ground potential (Figure 6a). This may cause a failure of the logic functionality if the inverter works under electrical noise condition.[10] After programming, the balance between the NM_L (6.8 V = 68% of ½ V_{DD}) and the NM_H (6.4 V=64% of ½ V_{DD}) was significantly improved as shown in Figure 6b. This improvement consequently leads to a better tolerance of the circuit against the effect of electrical noise.

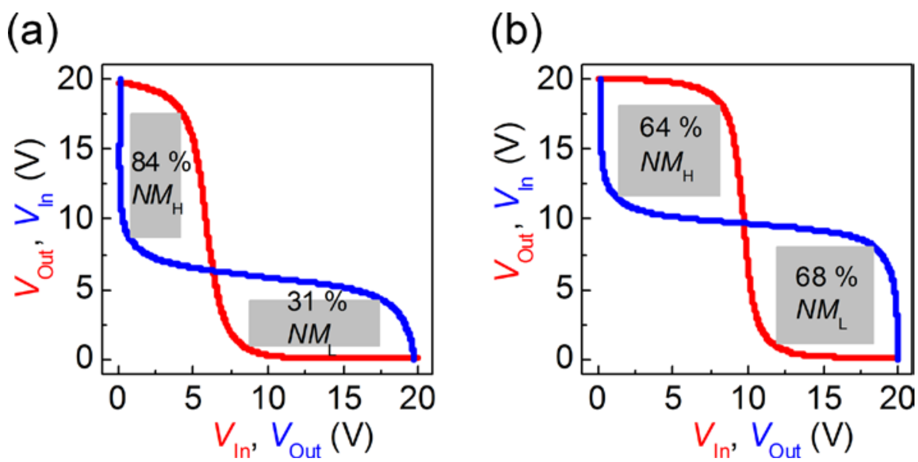

Figure 6. *NM* analyses from *VTC* curves measured at (a) initial state and (b) after programming with V_{PG} of −2 V.

Besides the low-program voltage, stability of a tuned circuit state is another important parameter. As mentioned above, the purpose for the development of tunable V_M in the complementary circuit is to develop a key technology for achieving a robust organic digital circuit, and have the longer retention time of the tuned state. The retention characteristic of the V_M at 9.8 V is shown in Figure 7. The programmed *VTC* and extracted V_M were nearly unchanged after 10^5 s, which is the best result ever reported in literature.[6,17] The obtained high-stability of the V_M indicates that our circuit can work reliably after programming.

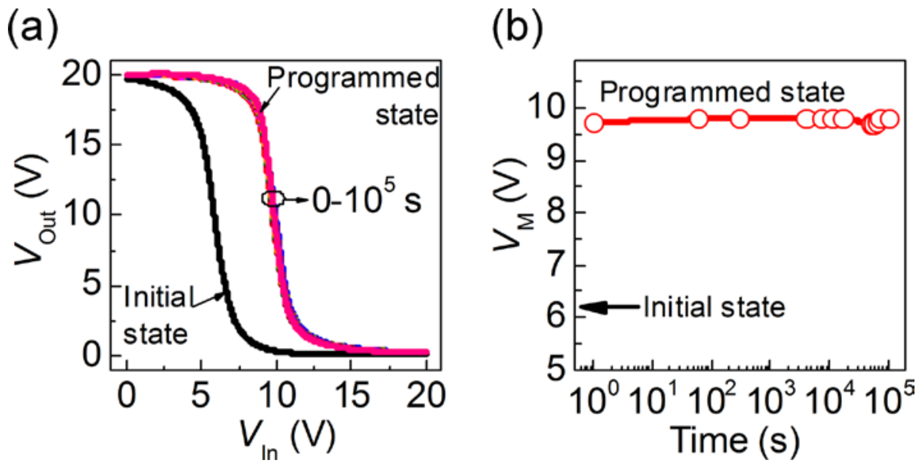

Figure 7. Retention time characteristics of (a) *VTC* and (b) V_M obtained after programming circuit.

Conclusions

In conclusion, we have demonstrated the controllable complementary organic circuits with a photoactive gate dielectric of DPA-CM:PMMA, the electron-trapping effect of Cytop, and use of Cu for a source/drain electrode. The V_{th} or V_M was tuned over a wide range by a V_{PG} application at less than 10 V and under UV light irradiation. At a V_{DD} of 20 V, and under a low V_{PG} of −2 V and UV light irradiation, the V_M can be at nearly half of the V_{DD} (V_{DD} = 9.8 V), resulting in an excellent balance between the NM_L (6.8 V = 68% of ½ V_{DD}) and the NM_H (6.4 V = 64% of ½ V_{DD}). In addition, the programmed circuit exhibited high stability and the programmed V_M was virtually unchanged after 10^5 s. We would like to emphasize here that the transistor circuit programming was performed under the UV light irradiation, however, the programming operation was required only at the initial stage, and the programmed state was kept for more than 10^5. Thus, the above-mentioned transistor circuits are very promising in developing high-performance complex organic logic integrated circuits.

Supporting Information

Schematic representation of program and erase state, V_{th} shift of as functions of UV light intensity and applied time. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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ABBREVIATIONS

OTFTs, organic thin-film transistors; V_{th}, threshold voltage; CMOS, complementary metal-oxide-semiconductor; V_M, switching voltage of inverter; μ, the field-effect mobility; pOTFT, p-channel OTFT; nOTFT, n-channel OTFT; NPs, Au nanoparticles; SAM, polar self-assembled monolayers; Cytop, poly(perfluoroalkenyl vinyl ether); DPA-CM, 6-[4'-(N,N-diphenylamino)phenyl]-3- ethoxycarbonylcoumarin; PMMA, poly(methyl methacrylate); PET, polyethyleneterephthalate; ITO, indium tin oxide; C_{60}, fullerene; L, channel length; W, channel width; I_D, drain current; V_D, drain voltage; V_{PG}, program gate voltage; VTC, voltage transfer characteristic; V_{In}, input voltage; V_{Out}, output voltage; NM, noise margin; NM_H, noise margin at high level; NM_L noise margin at low level.

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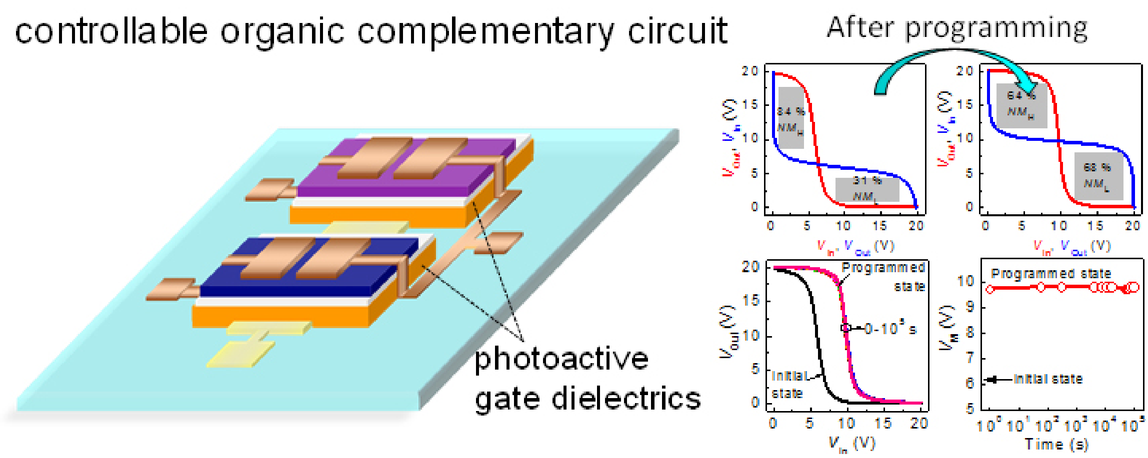
Graphical abstract



14

Supporting Information

Controllable threshold voltage in organic complementary logic circuits with an electron-trapping polymer and a photoactive gate dielectric layer

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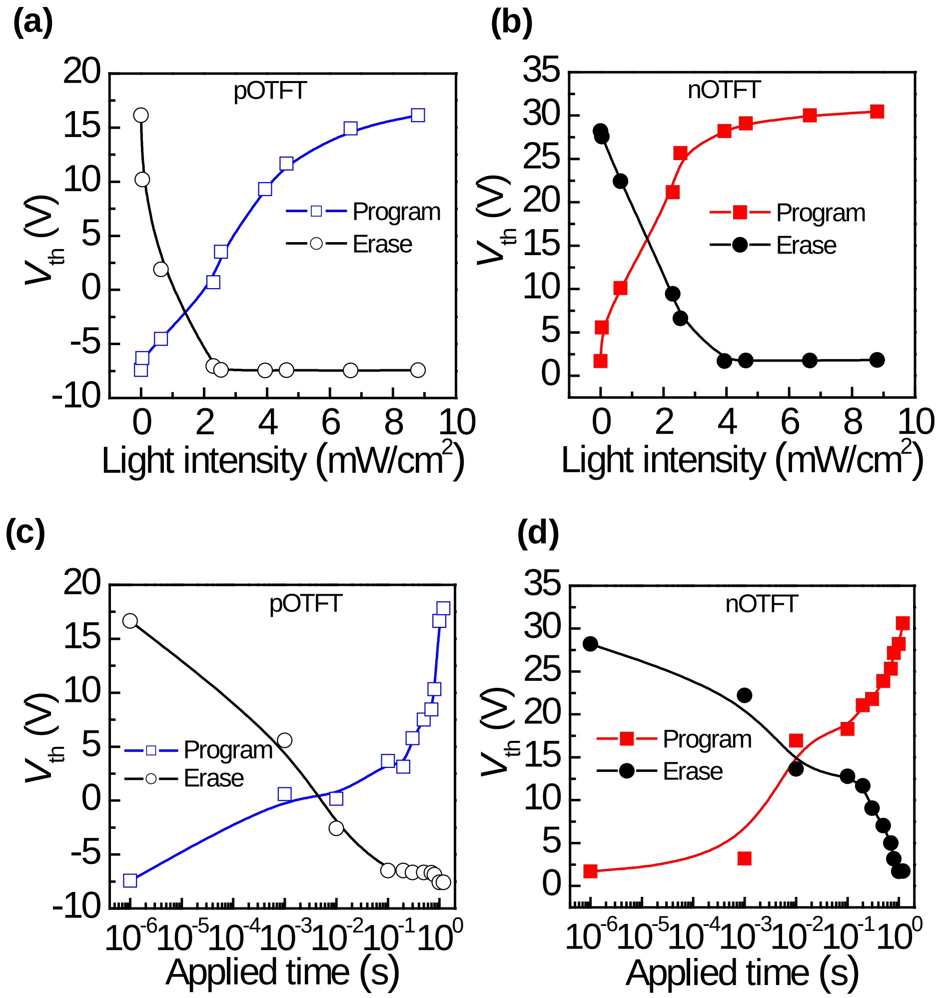

Figure S1. V_{th} shift of (a) pOTFT or (b) nOTFT as function of UV light intensity with V_{PG} of −10/10 V and applied time of 1 s. Change in V_{th} of (c) pOTFT or (d) nOTFT as function of applied time with V_{PG} of−10/10 V and UV light intensity of 3.94 mW/cm^2. V_{DD} values were set to be −10 V for pOTFT and 10 V for nOTFT in all transfer curve measurements.

The reversible shifts in the V_{th} as functions of the UV light intensity are investigated. (Figures S1(a) and (b)) The V_{th} was reversely controlled from –7.4 to +16.7 V for the pOTFTs, and from +1.7 to +30.6 V for the nOTFTs, respectively. At the programming state of pOTFTs, V_{th} gradually increased with the increase in the UV light intensity and nearly unchanged at UV light intensity higher than 6.6 mW/cm^2. Meanwhile, at the erasing state, the decrease in V_{th} saturated at the UV light intensities higher than 2.30 mW/cm^2. On the other hand, at the programming or erasing state of nOTFTs, the changes in V_{th} almost saturated at the UV light intensity of 3.94

mW/cm^2. Based on V_{th} changes versus UV light intensities in both circuit devices, we chosen a UV light intensity of 3.94 mW/cm^2 for programming and erasing the organic complementary circuit.

The reversible shifts in the V_{th} as functions of the applied time for V_{PG} are investigated. (Figures S1(c) and (d)). At the programming/erasing state of both pOTFTs and nOTFTs, V_{th} gradually shifted with the increase in the applied time of V_{PG}. In both pOTFT and nOTFT, the large V_{th} shift of c.a. 30 V for the 1 s duration of V_{PG} application is enough large to obtain the programming/erasing state. The applied time is similar to that in previous work.[1]

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