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Optimization of wave pipelining by the stage division

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Abstract

Pipelining has been studied for the purpose of processing throughput improvement of instruction execution. Cycle of wave pipelining is shorter than conventional one, and each stage of it operates at separate timing. Therefore, wave pipelining can be expecteal a higher throughput than conventional one. The performance of processors by the wave pipelining depends on the maximum difference of the maximum delay and minimum delay of each stage. If this delay difference is reduced, processor performance will improve.

In this paper, in order to apply the wave pipelining to a processor, the an efficient tequnique for shortening delay difference is proposed. Effectiveness and the validity of it is confirmed.

1 Introduction

Pipelining which overlaps execution of two or more instructions, and execute concurrently in order to speed up of processor has been studied. Pipelining accomplishes n times speed up by dividing an instruction execution to n pipeline stages.

The authores has been carrying out, researches about the wave pipelining which is one of the pipelining.

In order to adopt the wave pipelining for a processor, this paper proposes the method of performing stage division and delay balancing. The proposed method suppresses increase of amount of hardwares, the area, and power consumption. At a result, it achieves higher performance.

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2 Wave pipelining

Wave pipelining can be expected high throughput by operating with a faster clock than conventional pipelining. Clock cycle times of conventional pipelining is determined by the maximum delay of stages where delay is lowgest. However, the processor performance with wave pipelining depends on the maximum time of delay differences of each stage. Therefore, the performance upgrade overcoming limitations of conventional pipelining is attained by shortening the delay differences.

3 Delay balancing by stage division

The purpose of the delay ballancing by the stage division is upgrade of processor, reduction of hours of design, and restrain increase of the area by delay buffer insertion and the power consumption compared with upgrade.

The delay ballancing by the delay buffer insertion was reduced of delay difference by was equiponderated the minimum delay to the maximum delay of stage.

The delay ballancing by the stage division proposed in this paper counts the number of circuit element in a stage, while measures the minimum delay and the maximum delay of each stage. It is determined whether it divides a stage by the delay difference and divides in the place where the number of circuit element in a stage is half. Therefore, Although a number of pipeline's stages increases, the maximum delay can become small and can reduce a delay difference.

Whether it is n times of the target delay difference or not are the conditions which divide a stage. The value of n is set up optimum value by the result of the maximum delay difference in each stage and design intention.

It estimates about the amount of calculation immediately concerned with the hours of design in each delay ballancing. Consequently, the amount of delay calculation of the delay ballancing by the stage division decreases far compared with the case where stage division is not performed.

4 Design

First, it is necessary to decide about the processor organization as object of wave pipelining.

Then, To use delay ballancing by the proposed stage division, and the delay buffer insertion, it have to measure the delay information in a stage. Therefore, it is necessary to decide each element and wire delay paramater beforehand from delay model.

5 Evaluation

The delay ballancing by the stage division proposed in this paper is evaluated. The delay ballancing by only the buffer insertion, and the stage division are performed respectively,

for the stage of a processor. And the amount of hardwares, area, and delay difference are evaluated.

6 Consideration

It considers from the result which evaluated the wave pipelined processor. It ask for the rate of upgrade, and the rate of increased area in each of the delay ballancing by only the delay insertion, and the stage division, and the validity is considered.

Thereby, the effect in the delay ballancing by the stage division is large.

7 Conclusion

In this paper, the delay ballancing by the stage division was proposed as the delay ballancing which determined the performance, in the processor design which used the wave pipelining. And It compared with the performance of the delay ballancing by only the delay buffer insertion or conventional pipelining, and the validly is confirmed.

First, the advantage was described, comparing with conventional pipelining about based wave pipelining in this paper.

Second, it was described about the delay ballancing by the stage division.

Third, the processor organization which performs wave pipelining and delay paramater required in order to use the delay ballancing by the stage division was shown.

As a result, It was shown that the effect by dividing a stage is large.

Since a stage will be finely divided when stage division is performed repeatedly, the number of latches will increase. But the number of inserted buffers is few because the delay difference of devided stage is little. Conversely, since the number of stage division can be restrained when seldom performing stage division, the number of latches is few. But the number of delay buffers becomes huge by wave pipelining. Therefore, chip area and power consumption will increase.

It is important to set up optimum value by design intention in consideration of these trade-off.