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A Study on Low Power Processor Design Using Wave-pipelining

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Abstract

Recent years, improvement of processor performance makes power larger and larger. The PDA and mobile cellular phones need high performance and low power processor. In this paper, the author proposes a new method to reduce power consumption which introduces a novel circuit design technique without adding voltage control circuit or installing control software. Although using this circuit design technique increases circuit delay and makes low frequency processor, the author prevents lowering performance of the low power circuit introducing wave-pipelining which operates in the cycle time of difference between maximum delay and minimum delay of pipeline stage The author shows validity of the method reducing power consumption without lowering performance.

1 Introduction

The power consumption of processor becomes larger and larger as its performance improves. There are three conventional ways to reduce power, which is running processor with low voltage, operating processor with low frequency and to stop voltage supply for no operating blocks. In these ways, processor becomes low performance or requires additional control circuit which makes processor complex. To solve this problem, we need new ways to reduce power without performance lowering. To realize this objective, the author takes

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the smallest transistor in circuit design. As a result, though total delay of processor is larger, using wave-pipelining for pipeline stages, we shows that low power and high speed is realize.

2 The designing method for low power processor

The power consumption of processor is product of total capacitance of transistors and wiring C, operating frequency f and square of operating voltage V^2. To accomplish low power with reducing frequency or voltage causes processor slow. The capacitance of a gate node of transistor is proportional to width of the transistor, but on state resistance of the transistor is proportional to inverse of width of transistor. The small size of transistor is small gate capacitance and large on state resistance of transistor. The product of on state resistance of the transistor and gate capacitance is invariant, but product of wire resistance and gate capacitance becomes larger. Total delay increases. We introduce wave-pipelining to get high frequency. The wave-pipelining operates in the cycle time of difference between maximum delay and minimum delay of pipeline stage.

3 The design

To decide process rule, the author takes $0.1\mu m$ process rules. The simulation for deciding process rule is current-voltage property of nMOS and pMOS transistors. The logic circuit is simulated by HSPICE. Also, delay of wiring and gate are simulated. The condition for simulation is under 0.1 micrometer process with smallest width of transistor. Then the author designed processor for simulation.

4 Evaluation

In this chapter, we measured total delay and total power of processor. The power of processor is depend on input signal vectors. To evaluate power, we prepared 2 circuits, which are 4-bit carry lookahead adder(CLA) with 0.5 micrometer width transistor and smallest width transistor. The power of 4-bit CLA which is installed wave-pipeline with smallest transistor is half of 0.5 micrometer transistors. The power of processer is proportional to capacitance, so we count total amount of capacitance which changes output value of gate circuit at every clock cycle. Total of power is sum of power of simulaton period. There are two ways to evaluate power, one is power of 1 seconds and the other is power of 1 clock cycle. We evaluate power with 1 clock period.

5 Consideration

The processor without wave-pipeline operates at 500MHz frequency. The wave-pipelined processor with delay balanced could operate same frequency.

6 Conclusion

The author explained operation principle of MOS transistor in chapter 2. Then the author introduced parameters for designing processors in chapter 3. In chapter 4, The author simulated power of two 4-bit CLAs. The power of smallest transistor with delay-balanced 4bit CLA is about half of power using 0.5μ transistors.