Studies on multi-level per cell memories based on organic field effect transistors

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Electric memory plays an important role in the operation of many electronic systems such as mobile phones, personal computers, cameras. Organic memory, which was based on carbon-based material has been intensively researched because of their mechanical flexibility, low-cost, and suitability for large area fabrication. An organic memory could be fabricated based on a capacitor, a resistor or an organic field effect transistor (OFET). Among of them, the OFET-based memory has used widely because the capacitor- and resistor-based memories need an external circuit for operation.

The data stored in a single-bit memory is limited because there is only one ON state and one OFF state. To solve this issue, a development of multi-level cell (MLC) memory has been carried out, in which more bits of data could be stored in the same structure of memory. The MLC device should exhibit several ON states. In addition, the replication of ON states should be obtained after a programming/erasing repetition.

In this dissertation, we focused on the organic memory based on a structure of an OFET. In **chapter 2**, we improved the performance of the OFET before applying for a memory application. We found that the mobility (μ) of the OFET could be enhanced significantly when the copper source/drain electrodes were fabricated under high background pressure of 2.5×10^{-5} Torr. This simple technique was applied in our study.

In **chapter 3**, we fabricated a MLC memory using poly (vinyl cinnamate) (PVCN) as the charge trapping layer. The memory OFET showed four logic states with a retention time of 11,000 seconds. The trapped holes at the interface between the PVCN and the silicon dioxide layer were supposed to be the origin of the memory effect in this device. However, this memory exhibited the write-once-read-many characteristics, in which the stored data could not be erased.

In **chapter 4**, a MLC memory OFET was fabricated using Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as the charge trapping layer. The memory OFETs with a structure of $Si^{++}/SiO_2/Li^+@C_{60}$/Cytop/Pentacene/Cu exhibited a performance of p-type transistor with a threshold voltage (V_{th}) of -5.98 V and a μ of 0.84 $cm^2\ V^{-1}\ s^{-1}$. The MLC memory OFETs exhibited a memory window (ΔV_{th}) of approximate 10 V, 16 V, and 32 V under a programming gate voltage of 150 V for 0.5 s, 5 s, and 50 s, and an erasing gate voltage of -150 V for 0.17 s, 1.7 s, and 17 s, respectively. Four logic states were clearly distinguishable in our MLC memory, and its data could be programmed or erased many times. The origin of MLC memory effect in this memory OFET is the trap of electrons in $Li^+@C_{60}$ layer.

In **chapter 5**, the operation mechanism of the MLC memory OFET using $Li^+@C_{60}$ material was discussed. The origin of the memory effect in our OFETs is supposed to be 2 mechanisms. The first mechanism is the electron trapping at the $Li^+@C_{60}$ molecules, which caused by the programming voltage with short duration. An ultraviolet-visible spectroscopy measurement was carried out for an evidence of electrons trapping in the $Li^+@C_{60}$ molecules. On the other hand, under longer duration of programming voltage, the $Li^+@C_{60}$ molecules could migrate into and ionize the pentacene layer. As the result, the drain current of the OFET increase, which corresponds to the memory effect of the devices

In conclusion, the extremely studies on the charge trapping MLC memory OFET have been carried out. From the experimental data, we conduce that our memories have high potential applications for flexible storage, where the silicon wafer could be replaced by a plastic substrate.

Keyword: *multi-level cell, memory OFET, Thin film transistor, Lithium-ion-encapsulated fullerene, charge trapping memory.*