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Contents

List of Symbols

Symbols	Meaning
μ	Mobility
ΔV_{th}	Memory window
ΔG_{et}	The driving force of electron transfer
A	Area if capacitor device
d	Thickness of insulator in a capacitor
e	Elementary charge
I_{D}	Drain current
$I_{\mathrm{D,sat}}$	Saturation drain current
I_{G}	Gate current
J	Current density
L	Channel length
N	Number of trapped electron
P	Number of trapped hole
P/E	Programming/Erasing
V	Voltage
V_{D}	Drain voltage
V_{G}	Gate voltage
V_{th}	Threshold voltage
W	Channel width

List of Abbreviations

Abbreviations	Meaning
AFM	Atomic force microscopy
CD	Compact disc
CNT	Carbon nanotube
CPU	Central processing unit
CuPc	Copper phthalocyaine
CYTOP	Poly-perfluoro-alkenyl vinyl ether
D	Drain electrode
DRAM	Dynamic Random Access Memory
EPROM	Electrically programmable Read Only Memory
EEPROM	Electrically erasable programmable Read Only Memory
F8BT	Poly(9,9-di-n-octylfluorene-alt-benzothiadiazole)
FeRAM	Ferroelectric Random Access Memory
G	Gate electrode
HOMO	Highest occupied molecular orbital
IPA	Isopropyl alcohol
ITO	Indium tin oxide
LUMO	Lowest unoccupied molecular orbital
MIM	Metal/Insulator/Metal
MIS	Metal/Insulator/Semiconductor
MLC	Multi-level cell
NPs	Nanoparticles
OFET	Organic field effect transistor
OLED	Organic light-emitting diode
P4MS	Poly (4-methyl styrene)
PMMA	Poly (methyl methacrylate)
PS	Polystyrene
PVA	Poly (vinyl alcohol)

P(VDF-TrFE)	poly (vinylidene fluoride-co-trifluoroethylene)
PVN	Poly (2-vinyl naphthalene)
PVP	Poly (4-vinyl phenol)
PVPyr	Poly (2-vinnyl pyridine)
PQ	Poly quinoline
PαMS	Poly (α-methylstyrene)
RAM	Random access memory
ROM	Read only memory
S	Source electrode
SAM	Self-assembled monolayer
SCS 4200	Keithley 4200 semiconductor characterization
SLC	Single-level cell
SRAM	Static Random Access Memory
star-PTPMA	star-shaped poly((4-diphenylamino) benzyl methacrylate
UPS	Ultraviolet photoelectron spectroscopy
UV-Vis	Ultraviolet-visible spectroscopy
UV-O_3	Ultra-violet ozone surface treatment
WORM	Write-once-read-many
XPS	X-ray photoelectron spectroscopy

CHAPTER 1 || INTRODUCTION

1.1. Electrical memory

An electronic memory plays an important role in the operation of electronic devices such as mobile phones, personal computers, camera, music players. The memory or the storage is defined as a component or device that retains retrievable digital data over a time interval.[1] For the operation, the memory is connected to a central processing unit (CPU). Then data stored in the memory can be read or written by the CPU. Memory can be classified based on a method to connect to CPU and a response. A cache memory integrated inside the CPU has the highest access speed. The cache memory is used as a buffer to transfer data from/to an internal memory. The internal memory, which is connected to the CPU via system bus with high speed, stores all the data of the system for its operation. External memories such as floppy disk, hard disk, compact disc (CD) or a digital versatile disc or digital video disc (DVD) are portable storages, which can be used whenever they are connected. To enhance the performance of the electronic systems, a development of memories is essential.

Electrical memories also can be divided into non-volatile and volatile memories based on the duration of stored data when an electric supply power is turned off. The data stored in non-volatile memories could be remained for a certain time, while it stored in volatile memories would loss immediately. Further classification of electrical memories was reported[2-3], which is shown in Fig.1.1. ROM (Read Only Memory) including EPROM (Electrically Programmable ROM)[4] and WORM[3-5] (Write-once-read-many) could hold the data permanently after being written only

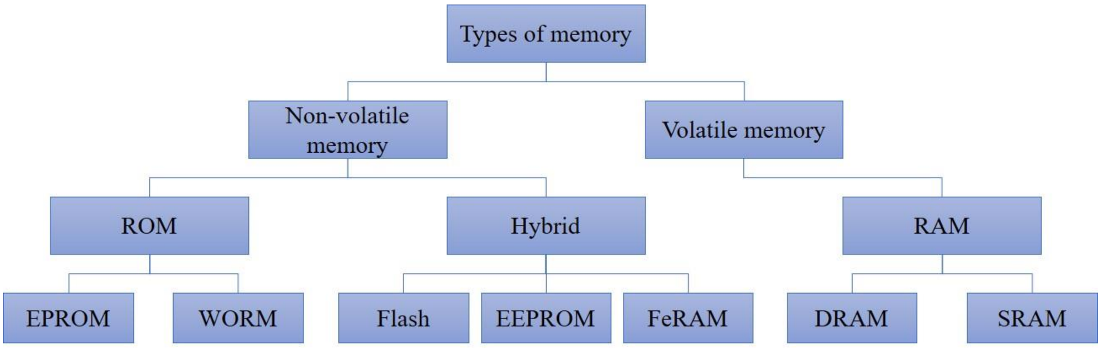

Fig.1.1. Classification of electrical memories

once and the stored data cannot be modified. Thus, this type of memory is often used to store the passive data in which the data are kept and made it available for the long-term use, such as Bios program in a computer. The flash, EEPROM (Electrically erasable programmable ROM) and FeRAM (Ferroelectric Random Access Memory) keep the data for a long time, and the data stored in them can be programmed or erased many times[3,6-10]. These memories are non-volatile and rewritable. These can be used for portable devices, for instance a portable music player and an USB (Universal Serial Bus) disk. The last forms of memory, RAM (Random Access Memory) including DRAM (Dynamic RAM) and SRAM (Static RAM) are often used for the memory of the computer system. The data in RAM can be programmed/erased many times with a high access speed. However, the data are lost when no electrical power is supplied.

1.2. Organic memory

The organic memory consists of carbon-based materials, including small molecules and polymers. There are many researches on the organic memory due to its advantages such as low temperature fabrication process, solution process ability or printability, a flexibility of devices, and low cost. Those are suitable for large area fabrication[2-10].

A classification of organic memories is based on a typical structure of the memory devices, of which organic memories can be divided into capacitor-, resistor- and transistor-based memory.

1.2.1. Capacitor-based memories

A capacitor-based memory has a structure of an insulator layer sandwiched between two electrodes. Based on the material for electrodes, there are two structures of capacitor-based memories: Metal/Insulator/metal (MIM) structure, and Metal/Insulator/Semiconductor (MIS) structure.

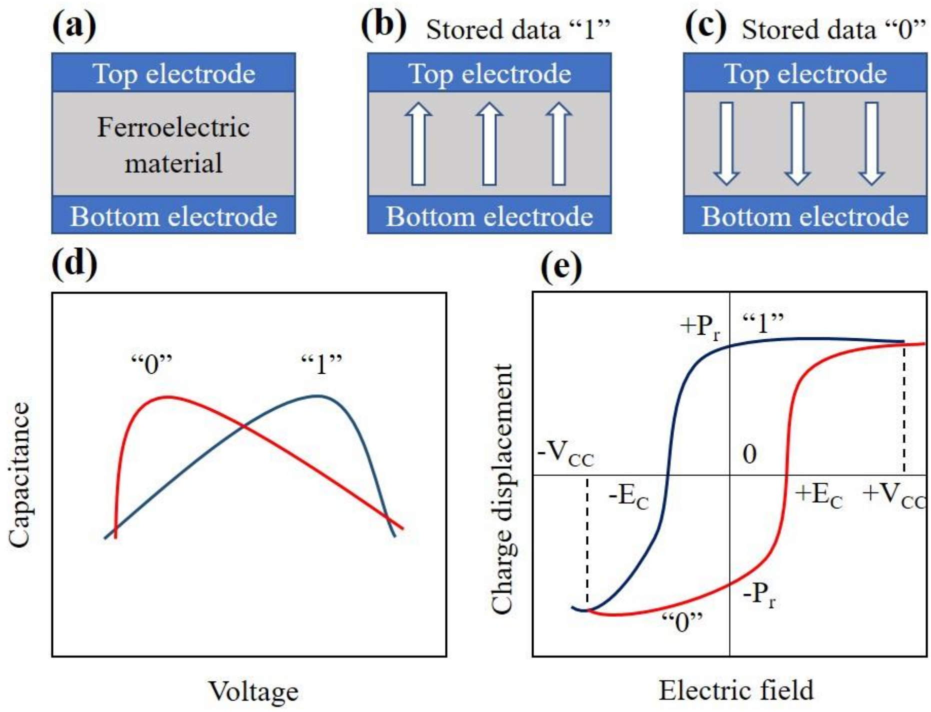

Fig.1.2. (a) Device structure, (b) polarization, (c) de-polarization, (d) capacitance-voltage, (e) charge displacement of a MIM memory

In the MIM memory as shown in Fig.1.2 (a), both electrodes are made from metals while the insulator is ferroelectric material[11]. By applying an external bias voltage, the ferroelectric layer is polarized (Fig.1.2 (b)) or depolarized (Fig.1.2 (c)) causing a hysteresis in a capacitance-voltage curve (Fig.1.2 (d)) or a charge displacement-electric field curve (Fig.1.2 (e))[12-14]. To program or write the data into the MIM memory, a required voltage of $+V_{CC}$ or $-V_{CC}$ is applied between electrodes, resulting in two stable states of the device, where upward polarization and downward polarization could be defined as a signal of "1" and "0", respectively[13]. To read the data in the MIM memory, a nearly zero voltage is applied. Electric field caused the polarization (depolarization) of ferroelectric layer, would increase (decrease) the bias voltage between the electrodes. This is detected and referred to the signal of "1" ("0")[15].

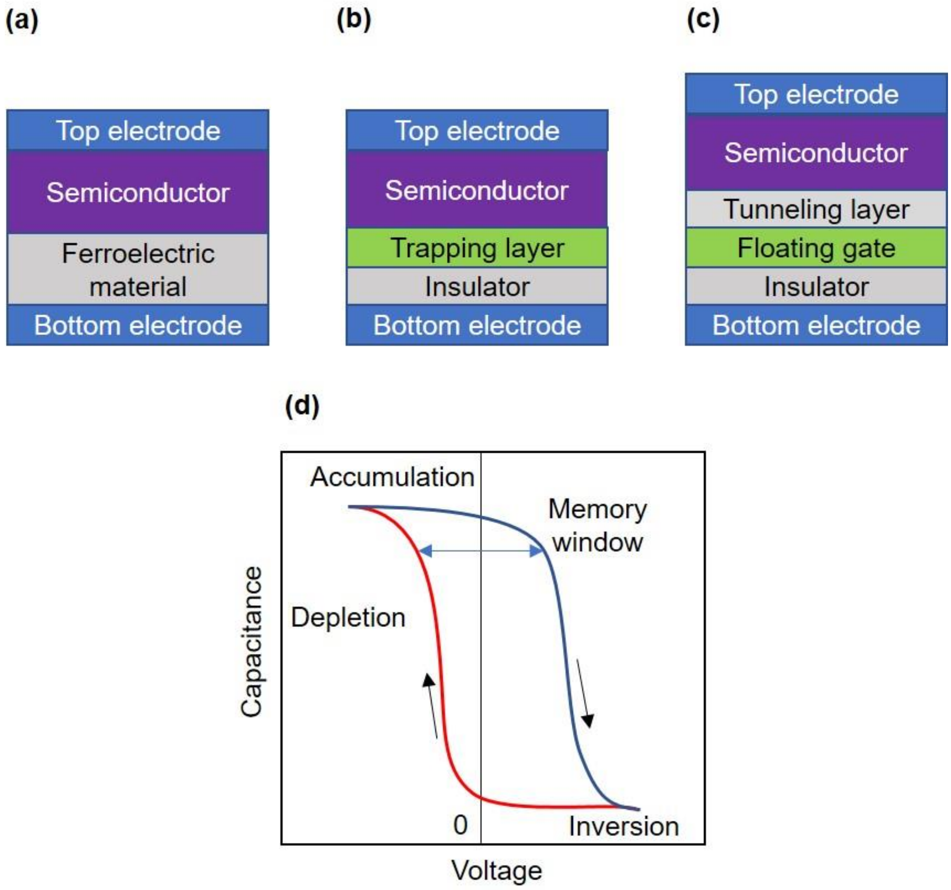

Fig.1.3. (a) Ferroelectric, (b) charge trapping, (c) floating gate structure, (d) capacitance-voltage curve of a p-type MIS memory.

The structure of the MIS memory is shown in Fig. 1.3 (a)-(c). When a high voltage is applied between electrodes, charges are injected from the top electrode, and then accumulated in a semiconductor layer. When a negative voltage is applied to the bottom electrode of a p-type MIS capacitor which is shown in Fig. 1.3b, the capacitor is in the accumulation case. The holes are increased at the surface of the semiconductor, and somehow could be trapped at the trapping layer. When the voltage is sweeping to small positive voltage, the MIS capacitor is not in the depletion case because the applied electric field is still smaller than that caused by the trapped holes. To get into to the depletion case and the inversion case, the MIS capacitor required higher applied voltage compared with the device without trapping layer. As the results, the capacitance-voltage (C-V) curve shifts to the positive region of applied voltage (the blue line in Fig. 1.3d). At high applied positive voltage, the trapped holes could be de-trapped. In addition, the electrons could be trapped at the charge trapping layer due to the high density of electrons at the semiconductor surface. In the case of reversed curve, because of the trapped electrons, the MIS memory will get into depletion case at negative applied voltage. And higher negative voltage is required to get into the accumulation case. Thus, the C-V curve shifts to the negative region (the red line in Fig. 1.3d). When high positive voltage is applied, the trapped electrons will be de-trapped and then holes will be trapped. The trapped holes make the C-V curve shift to positive region while the trapped electrons make it shift to the negative region. The hysteresis of the C-V curve of the MIS capacitor caused by the charge trapping relates to the memory effect of the device. The memory window of the MIS memory is calculated to be the difference of the flat-band between the forward and the reversed C-V curves. The difference capacitance of the MIS in the forward and backward curves refers to the logic signal of “1” or “0” of the stored data. The data can be lost when the memory is set in the depletion state.

1.2.2. Resistor-based memories

A memory based on resistor simply consists of an active layer between two electrodes (MIM structure) on a supporting substrate of plastics, glass metal foil (Fig. 1.4 (a)). Electrodes are mostly made from aluminum (Al), gold (Au), copper (Cu), or

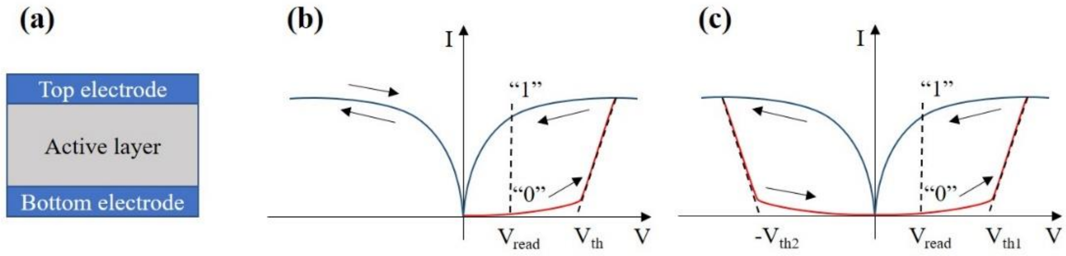

Fig.1.4. (a) A typical structure of a resistor memory, and the I-V curve of (b) a WORM or (c) a rewritable memory.

n-doped silicon (n-doped Si) and indium tin oxide (ITO). For the active layer, materials are small molecules, polymers, composite of polymer and molecules, nanoparticles (NPs) or some biomacromolucules[16-19]. Fig. 1.4 (b) and (c) show the current-voltage (I-V) curves of a WORM and the rewritable resistor-based memory. The operation of the memory devices is based on the change of the conductivity of the active layer corresponding to the applied voltage. At a programming voltage of V_{th} (or $+V_{\mathrm{th1}}$), the current changes from low to high, corresponding to the data of “1”, which is distinguished from the data of “0”. In the rewritable device, the stored data can be erased when a negative voltage of $-V_{\mathrm{th2}}$ is applied.

There are many operation mechanisms to explain the switching of the conductivity in the resistor memory. These mechanisms can be explained by the thermal, electronic, and electrochemical effects[16,20]. For the thermal effect, the crystalline state or the amorphous state at different temperatures determines the conductivity of the active layer, resulting in the change of the states of the memory[21,22]. On the other hand, the conductivity switching could be occurred by the electronic effect. Under a high electric field, charges are injected by Fowler-Nordheim tunneling and trapped at defects or metal nanoparticles in the insulator, resulting in the change in the resistance of the active layer[23-26]. Or electronic injected charges can act like a dopant which causes to an insulator-metal transition in perovskite-type oxides, correlates to the switching[27-29]. The third group of switching mechanism is based on the electrochemical effect, in which the migrations of cations[30] or anions[31] from electrodes to the active layer occur. These migrations correspond to the change of conductivity of the active layer.

1.2.3. Transistor-based memories

Both the capacitor- and the resistor-based organic memories require an external transistor for their operations while an organic field effect transistor (OFET)-based memory does not require[3,4,16]. Because of this advantage, this study focuses only on the OFET memory. Fig. 1.5 shows typical structures of the OFET memory including a ferroelectric transistor memory, a floating gate transistor memory, and a charge trapping transistor memory.

The ferroelectric transistor memory (Figure 1.5. (a)), which was proposed in the 1950s[32]. The ON and OFF states of the memory are obtained by a polarization or depolarization of the ferroelectric gate layer[32-35]. A material commonly used for the ferroelectric layer is poly (vinylidene fluoride-co-trifluoro ethylene) (P(VDF-TrFE)) because of its wide bandgap. As the result, the memory using P(VDF-TrFE) does not require another gate insulator[33]. Based on this material, Naber et al, reported a ferroelectric transistor memory with an ON/OFF ratio of 10^5, a retention characteristic up to one week, high programming cycle endurance of 1000 cycles, a short programming time of 0.5 ms, and the programming/erasing voltages of ±35 V[34,35]. To improve the performance of the ferroelectric transistor memory, the reduction in the operation voltages, and the short programming duration, as well as the long retention characteristics are significant.

Reported by Kahng and Sze in 1967, a floating gate transistor could be used as a non-volatile memory[36]. By applying a voltage to the gate, charges were injected from the source/drain (S/D) electrodes and then trapped in the floating gate. These trapped charges affect to the charge carriers in the channel, causing the change in the drain current (I_D) and the shift of the threshold voltage (V_{th}) of the OFETs (Fig. 1.5. (b)). Since the trapped charges in the floating gate are blocked by the insulator, the change in the I_D and the shift of the V_{th} will remain unchanged, corresponding to the memory effect. For erasing the memory, a reversed voltage is applied to the gate, removing the charges from the floating gate. The floating gate could be made from a thin layer of metal such as aluminum[37,38]. These memories exhibited excellent memory characteristics with an operation voltage of lower than 6 V, a large memory window (ΔV_{th}) of 2.4 V, retention time of 10^5 seconds and a stable V_{th} after 10^3 program-erase cycles. However, a fabrication process of this memory transistor

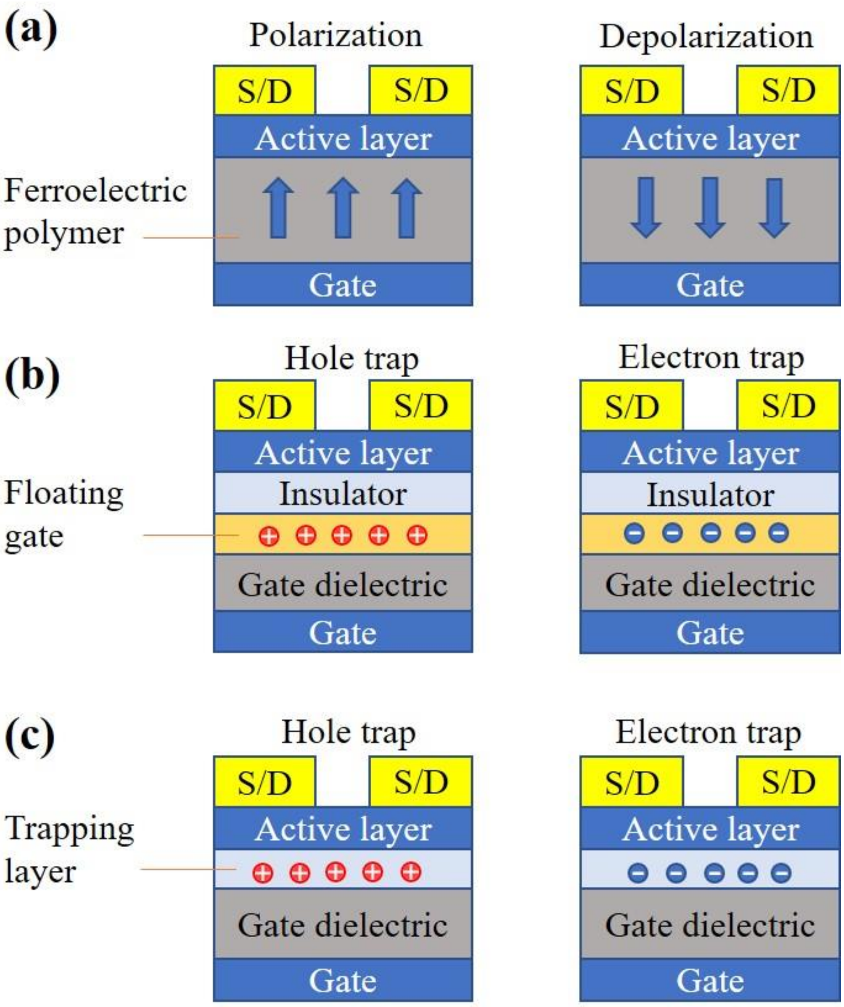

Fig.1.5. A typical structure of (a) a ferroelectric transistor memory (b) a floating gate transistor memory, and (c) a charge trapping transistor memory.

required complicated technique. Another method for a floating gate fabrication is using nanoparticles. In 2003, Kolliopoulou et al. reported a memory transistor using gold nanoparticles (AuNP) as the floating gate separated from the Al gate electrode by an insulator, which was made by Langmuir-Blodget technique[39]. The excellent characteristics of the memory were observed with the low operation and programming/erasing voltages of 6 V. Up to now, many efforts to make the fabrication process of Au NP-floating gate memory more simply were reported by Z. Liu et al.[40], W. Wang et al, S.-J. Kim et al.[41], and K.-J. Baeg et al.[42]

The operation of a charge trapping memory transistor is similar to that of the floating gate memory, of which the charges are injected from the S/D electrodes and trapped at the dielectric layer (Fig. 1.5 (c)). The trapped charges affect to charge

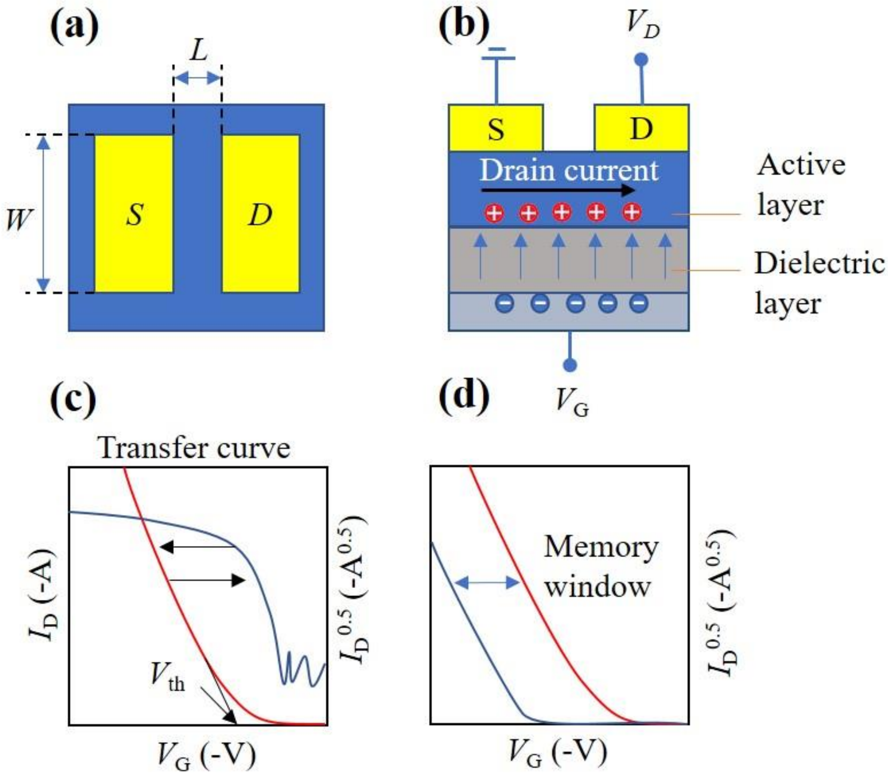

Fig.1.6. (a) the top view, (b) cross section of top-contact p-channel OFET and (c) its typical transfer and (d) the ΔV_{th} definition of the memory.

carriers in the channel of the OFETs causing the change in the I_D and the shift of the V_{th}, which is related to the memory effect. The first charge trapping memory OFET was reported in 2002 by H.E. Katz et al.[43], and then many other research groups started to focus on this topic. Baeg et al. reported a pentacene-based memory OFET using poly(α-methylstyrene) (PαMS) as a charge trapping layer fabricated on a layer of SiO_2 [44]. This memory showed a large ΔV_{th} of 90 V as well as a long retention time up to 100 h, but it required high programming/erasing voltages of 200/-100 V. Beside the use of PαMS for charge trapping layer[44,49], some other materials were used such as polystyrene (PS)[45], poly (4-methyl styrene) (P4MS)[45], poly (2-vinyl naphthalene) (PVN)[45], poly (4-vinyl phenol) (PVP)[45], poly (2-vinnyl pyridine) (PVPyr)[45], poly (vinyl alcohol) (PVA)[45,46], poly(methyl methalcrylate) (PMMA)[47], and poly (perfluoroalkenyl vinyl ether) (CYTOP)[48]. The charge trapping memory OFETs have an advantage of the simple structure and facile fabrication process. Therefore, we utilized this structure to fabricate our devices.

Basic parameters of the OFET memory

Technical parameters of an organic field effect transistor were described in the IEEE Standard 1620-2004[50] and the IEEE Standard 1005-1998[51], which were summarized in Fig. 1.6, the table 1.1, and 1.2 as bellows:

Table 1.1. Definitions

Definition	**Meaning**
W	The width of the channel (Fig. 1.6 a)
L	The length of the channel (Fig. 1.6 a)
I_{DS} (I_D)	The current flow measured through the drain electrode
I_{GS} (I_G)	The current flow through the gate dielectric, leakage current
V_{DS} (V_D)	The voltage applied to the drain electrode
V_{GS} (V_G)	The driven voltage applied to the gate electrode
Transfer curve	Measurement where I_D is measured as a V_G swept from a start voltage to a stop voltage (Fig. 1.6 c)
Output curve	I_D vs. V_{DS} for a fixed V_{GS}
μ	Mobility is the majority carrier mobility of semiconductor material derived through transfer curve
V_{th} (V_T)	Threshold voltage is the minimum gate voltage required to induce the channel (Fig. 1.6 c)
On/off ratio	The maximum I_D value divided by the minimum I_D value, obtained from the transfer curve
Program/erase voltages	The voltages applied to the gate to make the states of the memory change
Switching time	The duration of program/erase voltages
ΔV_{th}	Memory window is defined by the difference in V_{th} between the programmed and erased states (Fig. 1.6 d)
Retention	Time from data storage to the time at which a veritable error is detected from any cause.
Endurance	Number of program/read/erase/read cycles

Table 1.2. Device structure

Definition	**Meaning**
Bottom-contact	An OFET structure where the S and D electrodes are located closer to the substrate than the semiconductor.
Bottom-gate	An OFET structure where the gate electrodes are located closer to the substrate than the semiconductor.

1.3. Organic multi-level cell memories

Along with the development of electronic devices, both the size and the mass of them are needed to reduce. Moreover, their operation should be stronger with a lower power consumption. The memory, which is an essential part of the computer system, also should be smaller with high volume. Thus, an increase in the capacity of storage has been attractive attentions, resulting in the development of a multi-level cell (MLC) memory. A MLC memory or a MLC per cell storage differentiate from a single-bit memory or a single level cell storage (SLC) at the capacity of storage. R. Michelroni et al, showed his definition of a SLC memory and a MLC memory in his textbook.[52] A SLC memory distinguishes between “1” and “0” by having no charge or charge present on the floating gate of the memory cell. By increasing the number of charge in the floating gate or V_{th} levels, more than 1 bit of data per cell may be stored

MLC requires accurate placement of the V_{th} level so that the charge distribution do not over-lap. Another requirement for the accurate sensing of the different charge level. These requirements ensure the replication of the logic states after the programming/erasing repetition. To satisfy requirements above, the polarization of the ferroelectric layer in the ferroelectric memory or the quantity of the trapped charges in NPs or the trapping layer must be controlled perfectly. Thus, a few of researches on the MLC organic memory have been published [53-61].

Despite containing several states, a structure of the MLC memory is not different from that of the single-bit memory. It means that the MLC memory structure is also based on a resistor[53,54], a capacitor[55,56], or a transistor[57-61]. The MLC memory based on a resistor was reported by Hwang et al in 2012 using doped-carbon nanotubes (CNTs) as an electron trapping material combined with PS. Excellent memory characteristics were observed in the devices under a low operation voltage of -1 V. Recently in 2016, Lee et al. reported another MLC resistor memory using a mix of Poly(9,9-di-n-octylfluorene-alt-benzothiadiazole) (F8BT) and P(VDF-TrFE) as a main part of an active layer[54]. Although this memory exhibited 4 logic states, it had a poor retention time of only 1,000 seconds and a low on/off ratio of about 10^2. The ferroelectric material of P(VDF-TrFE) was used not only for the capacitor-based[55,56] but also for the transistor-based MLC memories[57,58]. The capacitor-based memory reported by Kim et al.[55] exhibited an excellent performance with an operation voltage of lower than 20 V, expected retention time of 10 years, and showed 1,800 cycles of endurance measurement. Moreover, a model of the capacitor-based memory was given by Khikhlovskyi et al. could store 3 bits of data[56]. In terms of the transistor-based memory, ferroelectric MLC devices were introduced by Tripathi et al. in 2011[57], Khan et al. in 2015[58]. Common characteristics of P(VDF-TrFE)-based memory OFET were a low operation and programming voltages of lower than 30 V, but the retention time was only 10^4 seconds.

Regarding to the concept of the charge trapping memory, Guo et al. reported a MLC OFET using pentacene or copper phthalocyaline (CuPc) as an active material and PS or PMMA as a charge trapping layer[59]. Under a drain voltage (V_D) of -60 V, the memory OFET showed several ON states after programming by applied voltages of 80 V with an assisted-light resource. This disadvantaged feature would limit applications of this device, although it exhibited a high on/off ratio and long retention characteristics compared with the ferroelectric MLC memory OFETs. In 2013, Chiu et al. reported a charge trapping MLC memory OFET, which used a material of a star-shaped poly((4-diphenylamino) benzyl methacrylate (star-PTPMA) for the charge storage and N,N'-bis(2-phenylethyl)perylene-3,4,9,10-bis(dicarbonximide) for a n-type channel[60]. This device operated with a high programming voltage of 200 V, and exhibited a write-once-read-many memory, of which those data could not be erased. Recently, in 2016, another MLC memory OFET was introduced using a new material of polyquinoline (PQ). The layer of PQ is ascribed to trap electrons, which causes the hysteresis in the transfer curve, corresponds to the MLC effect in this OFET[61]. In spite of some limitation such as high operation and programming voltages, disability to erase the stored data, this result was still a positive sign for the application of the new material in the MLC memory OFET.

To deeply understand about the MLC memory organic devices, some issues of them were listed and summarized in the next section in this chapter.

1.4. Summary of current issues of the MLC organic memory

Based on a few researches on the MLC organic memory, some current issues are summarized and shown in the table 1.3. The most significant issue of the organic MLC memory is the shortage of desired materials. Almost memory devices were fabricated using P(VDF-TrFE). These memories exhibited an excellent performance. In the case of the charge trapping MLC memory OFETs, only polymers of PS and PMMA were used. It inspires us to investigate different polymers as the charge trapping layer for the devices. In addition, the use of a new material for charge trapping layer is expected to open a new trend of the research in these kinds of the devices.

Table 1.3. Summary of current issues in the organic MLC memory

Characteristics	Resistor-based memory	Capacitor-based memory	Transistor-based memory	
			Ferroelectric	Charge trapping
Structure	1T-1R	1T-1C	1T	1T
Key material	P(VDF-TrFE) Doped- CNT	P(VDF-TrFE)	P(VDF-TrFE)	PS, PMMA, star-PTPMA, PQ
Operation voltage	< 20 V -1 V	< 20 V	< 30 V	60 V 100 V
Programming conditions	18.5 V 3 V	8 V	30 V, or	80 V with light, 200 V, 100 V
Retention	1,000 s	Up to 10 years	3,500 seconds	20,000 seconds

1.5. Aims of study

Because the MLC memory using P(VDF-TrFE) exhibited an excellent performance, subjects of this dissertation are to focus on the charge trapping structure of devices with a semiconductor of pentacene. Because of the high programming and operation voltages in the charge trapping memory OFETs, I proposed the aims of this study are:

- A method to increase a performance (mobility) of the OFET, which could be applied to the memory OFET.
- Reduction of operation voltage
- Reduction of programming voltage

To archive these aims, I applied the new material of poly (vinyl cinnamate) and Lithium-ion-encapsulated fullerene as the charge trapping layer. Fig. 1.7 shows the structure of this dissertation, which main achievements were summarized as follows:

The first achievement is a simple method to increase the mobility of an OFET using pentacene as an active layer and copper electrodes. The OFET with S/D electrodes deposited at a high background pressure of 2.5×10^{-5} Torr exhibited a threefold higher mobility (μ) and a lower threshold voltage (V_{th}) than that of the OFETs with gold or copper electrodes fabricated at a low pressure of 1.6×10^{-6} Torr. The increase in μ was investigated to be a reduction of contact resistance due to a penetration of oxygen into the pentacene layer. This content will be presented in chapter 2.

The second achievement is a write-once-read-many memory OFET using poly (vinyl cinnamate) as the charge trapping layer (Chapter 3). This memory OFETs exhibited V_{th} shifts of approximately 9, 18, 28 V after the programming voltages of -160, -180 and -200 V, respectively. Although the programming voltages were high, this memory showed a high stability of logic states with a long retention time. In the later of the chapter 3, the proposed operation mechanism was discussed.

Chapter 4 introduces the main part of this dissertation, where a multi-level memory OFET was fabricated using Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as a charge trapping material. The memory OFETs with a structure of

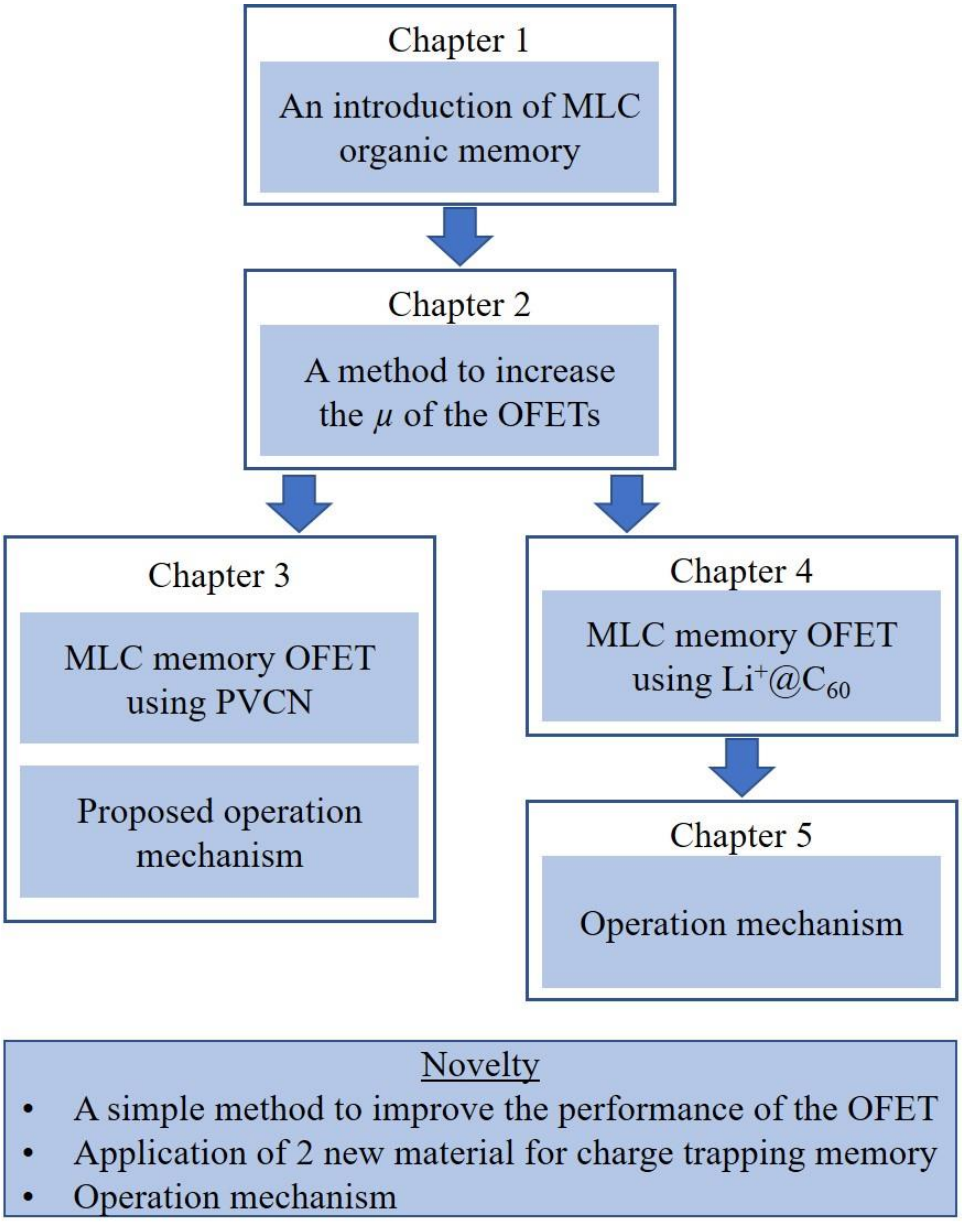

Fig.1.7. Structure of the dissertation

$Si^{++}/SiO_2/Li^+@C_{60}$/Cytop/Pentacene/Cu exhibited a performance of the p-type transistor with a V_{th} of -5.98 V and a μ of 0.84 $cm^2\ V^{-1}\ s^{-1}$. The multi-level memory OFETs exhibited the ΔV_{th} of approximate 10 V, 16 V, and 32 V, with a programming gate voltage of 150 V for 0.5 s, 5 s, and 50 s, and an erasing gate voltage of -150 V for 0.17 s, 1.7 s, and 17 s, respectively. Four logic states were clearly distinguishable in our multi-level memory, and its data could be programmed or erased many times.

The mechanism operation of the memory OFETs using $Li^+@C_{60}$ was discussed in detail. The memory effect of the OFETs is caused by the electrons trapping at the $Li^{+}@C_{60}$. When the OFET was programmed for a short duration, the average number of trapped electrons per each $Li^{+}@C_{60}$ molecule was estimated based on the total of trapped electrons in the $Li^{+}@C_{60}$ layer over the density of $Li^{+}@C_{60}$ molecules per area. By programming for 0.5 s, the average number of trapped electrons per $Li^{+}@C_{60}$ molecule was 2.40×10^{-2}. Based on this result, we assumed that only $Li^{+}@C_{60}$ molecules at the surface of $Li^{+}@C_{60}$ domains could trap the electron. Beside the memory effect caused by the electron trapping, the $Li^{+}@C_{60}$ molecules were proposed to migrate into the pentacene layer. This migration causes the change in the I_D of the OFET, which is one origin of the memory effect in our memory device. To confirm the charge trapping in the $Li^{+}@C_{60}$ molecules by electric field, an ultraviolet-visible spectroscopy (UV-Vis) measurement was carried out to detect an evidence. This work is reported in the chapter 5.

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CHAPTER 2 || AN EFFECT OF BACKGROUND PRESSURE ON THE PERFORMANCE OF MEMORY OFETS FOR MLC DEVICES*

We demonstrated an effect of vacuum pressure on the mobility (μ) and the threshold voltage (V_{th}) of organic field effect transistor (OFETs) using copper as source/drain (S/D) electrodes. By deposited under the background pressure of 2.5 × 10^{-5} Torr, the μ of the OFETs is c.a. 2 times and 3 times c.a. greater than that of the OFETs with gold and copper electrodes fabricated under low pressure of 1.6 × 10^{-6} Torr, respectively. The reason for the increase of the μ could be due to the charge injection barrier reduction, which caused by a penetration of oxygen into pentacene layer during deposition at high pressure.

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2.1. Introduction

Owing to their advantages of low cost, low temperature processing, and mechanical flexibility, organic field effect transistors (OFETs) could be applied in many applications such as organic memories, pressure sensors[1-3]. For the wide use, an improvement of OFETs performance as well as an increase in reliability and stability are required[4]. The performance of OFETs is determined by device's parameters such as the μ, the V_{th} and the on/off ratio as well as a low operation voltages. In particular, an improvement of μ and a reduction of V_{th} have been research targets. To obtain this, an approach is an application of high-k material as the gate insulator[5]. In the case of OFETs using pentacene as semiconductor, both inorganic and organic high-k material such as barium zirconate titanate (BZT, k = 17.3, μ = 0.32 cm^2 V^{-1} s^{-1}, V_{th} = -4 V), barium strontium titanate (BTS, k = 16)[6], aluminum oxide (Al_2O_3, k = 9, μ = 0.2 cm^2 V^{-1} s^{-1}, V_{th} = -2 V)[7], tantalum oxide (Ta_2O_5, k = 23, μ = 0.8 cm^2 V^{-1} s^{-1}, V_{th} = -0.3 V)[8], and poly (4-vinylphenol) (PVP)[9], or photocross-linkable PVP[10] were used. In addition, some polymer-nanoparticle composite dielectrics were also used for low voltage organic transistors[11]. For example, Zirkl er al. reported an OFET using nanoparticles of zirconium oxide (ZrO_2) combined with poly (α-methyl styrene) (PαMS) as gate dielectric layer with a μ of 1.2 cm^2 V^{-1} s^{-1} and a V_{th} of -1.1 V[12]. Moreover, a modification of the dielectric layer could be used to enhance a semiconductor film growth and reduce a leakage current in the OFET.

Another approach to increase the μ and to reduce the V_{th} of OFETs is by a reduction of a contact resistance between the S/D electrodes and semiconductor layer[13]. As charges are injected from the S/D electrodes, the reduction in contact resistance would increase the I_D at low bias voltage applied to the gate (V_G), resulting in better μ and V_{th} of OFETs. To reduce the contact resistance, the charge injection barrier between Fermi level energy of electrodes metal and lowest unoccupied molecular orbital (LUMO) level energy (for electron injection) or highest occupied molecular orbital (HOMO) level energy (for hole injection) needs to be decrease. To obtain this target, a very thin layer of metal oxide such as Ta_2O_5[14], molybdenum trioxide (MoO_3)[15], Al_2O_3[16], or cupric oxide (CuO)[17] was inserted between S/D electrodes and the semiconductor layer. W. Gu et al. reported the use of a layer of copper sulfide (Cu_xS) instead of metal oxide. These OFETs using Cu_xS/Cu electrodes obtained the μ of 2.3 $cm^2\ V^{-1}\ s^{-1}$ and the V_{th} of -13 V as well. In this OFETs, Cu^{2+} and SO_4^{2-} were considered to be responsible for the reduction of contact resistance[18]. This result shows us the application of Cu as S/D electrodes has much potential to improve the μ of the OFETs.

In this chapter, we present an effect of background pressure during electrode deposition on its contact resistance reduction, which results in the increase of the performance of the OFETs. The OFETs with copper electrodes deposited at a pressure of 2.5×10^{-5} Torr were found to show an increase in μ as well as a reduction of V_{th} compared with those of copper and gold electrodes fabricated under lower background pressure.

2.2. Experimental

Figure 2.1 (a) and (b) show the cross structure and the illustration fabrication process of the OFETs in this work. The OFETs were fabricated on heavily doped silicon wafer (n^+Si, resistivity of 1-10 Ω·cm) coasted with a 50-nm silicon dioxide (SiO_2). These wafers were cleaned ultrasonically in acetone for 10 min, in pure water twice for 5 min each, and isopropyl alcohol (IPA) for 10 min, subsequently subjected

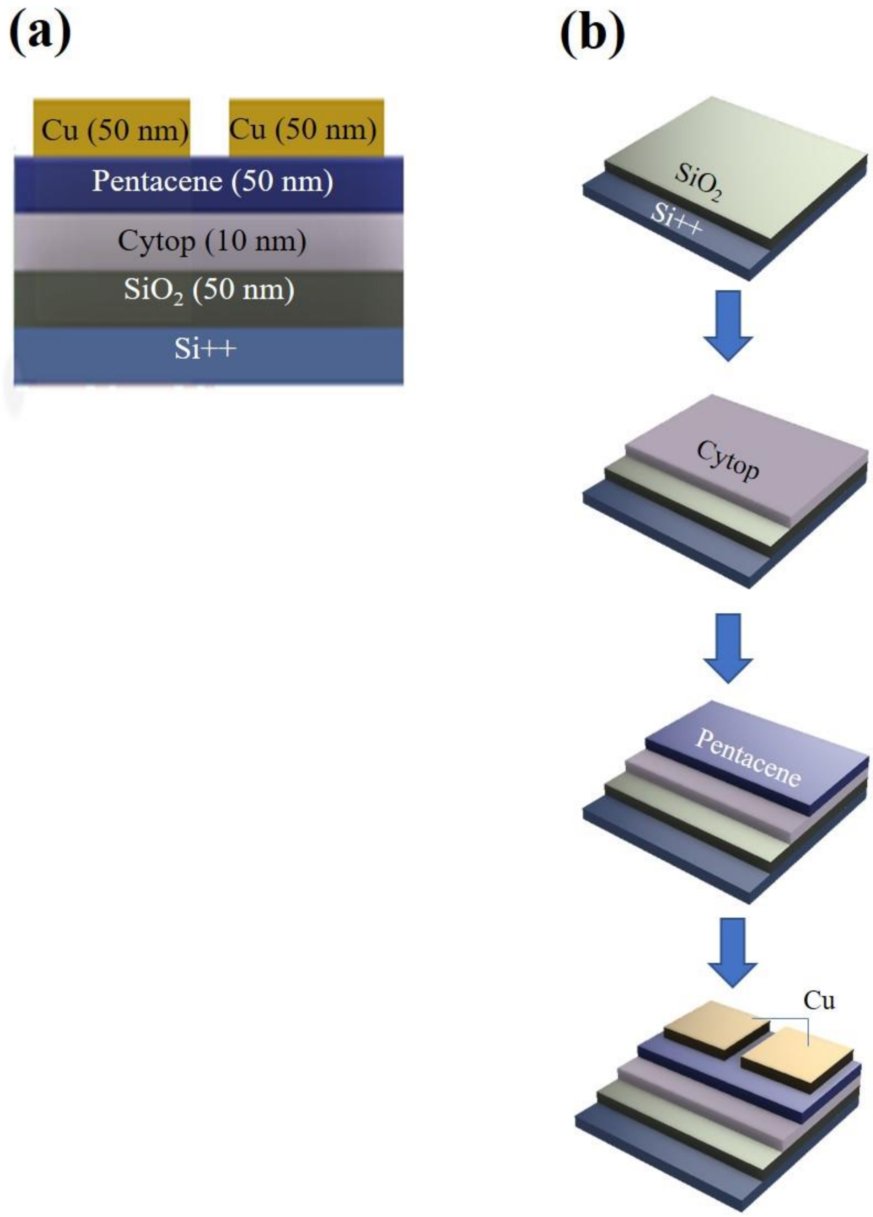

Fig.2.1. (a) A cross structure, and (b) an illustration fabrication process of OFETs

to an ultraviolet-ozone surface treatment (UV-O_3) for 30 min. All substrates in this dissertation were cleaned follows this cleaning process.

The SiO_2 surface was modified by a thin layer of Cytop (CTL-809 M, Asahi Glass). This layer was fabricated by spin-coating at 2,500 rpm for 60 seconds using a solution with a concentration of 0.5 wt%, followed by drying at 100 ºC for 2 h. The thickness of the Cytop layer was ~10 nm, measured by an atomic force microscopy (AFM, Keyence VN-8000 nanoscale hybrid microscopy).

For an active layer of OFETs, a layer of pentacene was thermally deposited under a background pressure of 1.6×10^{-6} Torr and a deposition rate of 0.3 Å/s. The copper S/D electrodes were sequentially deposited by using shadow masks at a higher pressure of 2.5×10^{-5} Torr and a deposition rate of 0.3 Å/s. The length (L) and width (W) of the channel were 50 µm and 2,000 µm, respectively. The thickness of Cu electrodes was 50 nm.

For comparison, OFETs using gold and Cu electrodes deposited under 1.6×10^{-6} Torr were fabricated.

The electrical characteristics of the OFETs were measured with a Keithley 4200 semiconductor characterization system in a dry nitrogen atmosphere at room temperature.

2.3. Basic parameters of OFETs

2.3.1. Electrical characteristics configuration

In order to determine the characteristics of OFETs, a Keithley 4200 semiconductor characterization system (SCS 4200) was used in this dissertation. The SCS 4200 consists of pre-appliers (PreAmps), current/voltage sources, ampere/voltage meters and oscilloscopes, which are integrated in a computer. For a basic characterization of OFETs such as transfer, output measurements, the SCS 4200 operated in a sweeping mode. Fig. 2.2 shows a setup for a basically electrical measurement of OFETs.

2.3.2. Electrical characteristics of OFETs

Figure 2.3 (a) shows a tantamount electric circuit which is used for output characteristics measurement. The I_D of OFET were measured while the S-D voltage (V_D) was varied from 0 to -10 V at different V_G sweeping from 0 to -10 V with a step of -2 V. As shown in Fig. 2.3 (b)-(d), the I_D of all transistors increased linearly at low V_D, and became saturated at high V_D, because the conducting channel in the pentacene layer was pinched off. All the devices exhibited the characteristics as typical p-channel OFETs. At the same V_D of -10 V and V_G of -10 V, the on-state current (-8.97 μA) of OFETs with Cu electrodes deposited at high pressure is c.a. 10 times greater than that of the OFET using gold electrodes (-0.88 μA). Within the comparison of Cu electrodes devices, high pressure brings about c.a. 64 times greater current than that of low pressure devices (-0.14 μA) (Fig. 2.3. (b)-(d)).

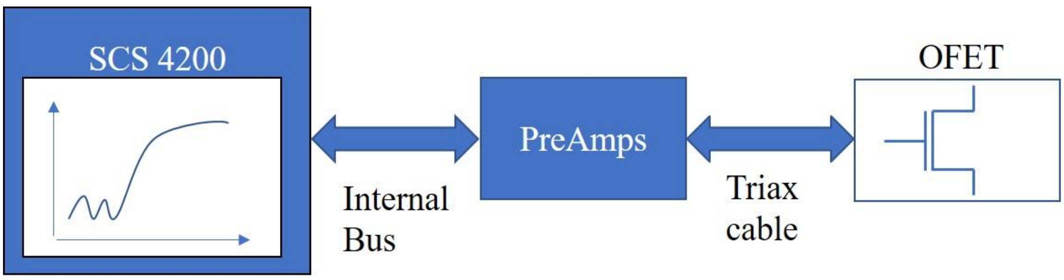

Fig.2.2. Setup for characterization of OFETs

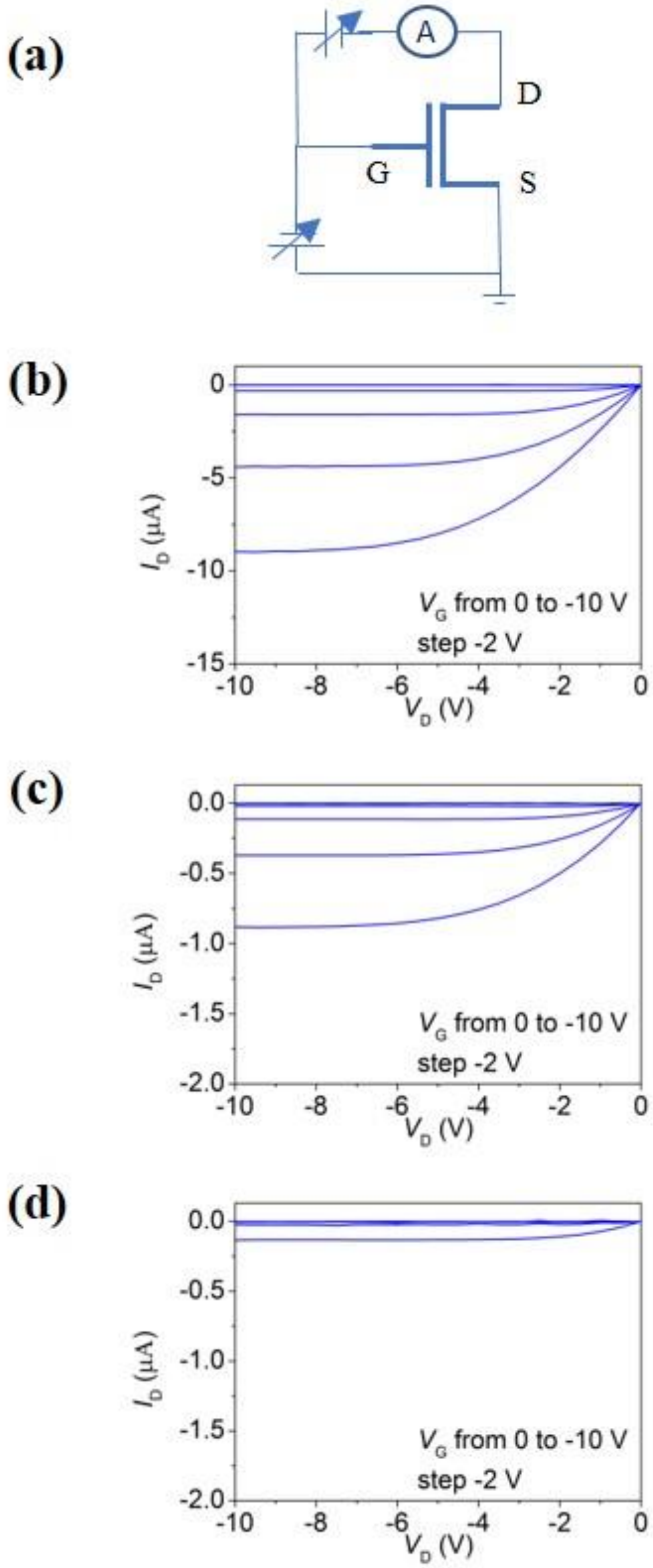

Fig.2.3. (a) Tantamount circuit for output characteristics, the output curves of OFET with (b) Cu electrodes deposited under a pressure of 2.5×10^{-5} Torr, with (c) gold and Cu (d) electrodes deposited under pressure of 1.6×10^{-6} Torr.

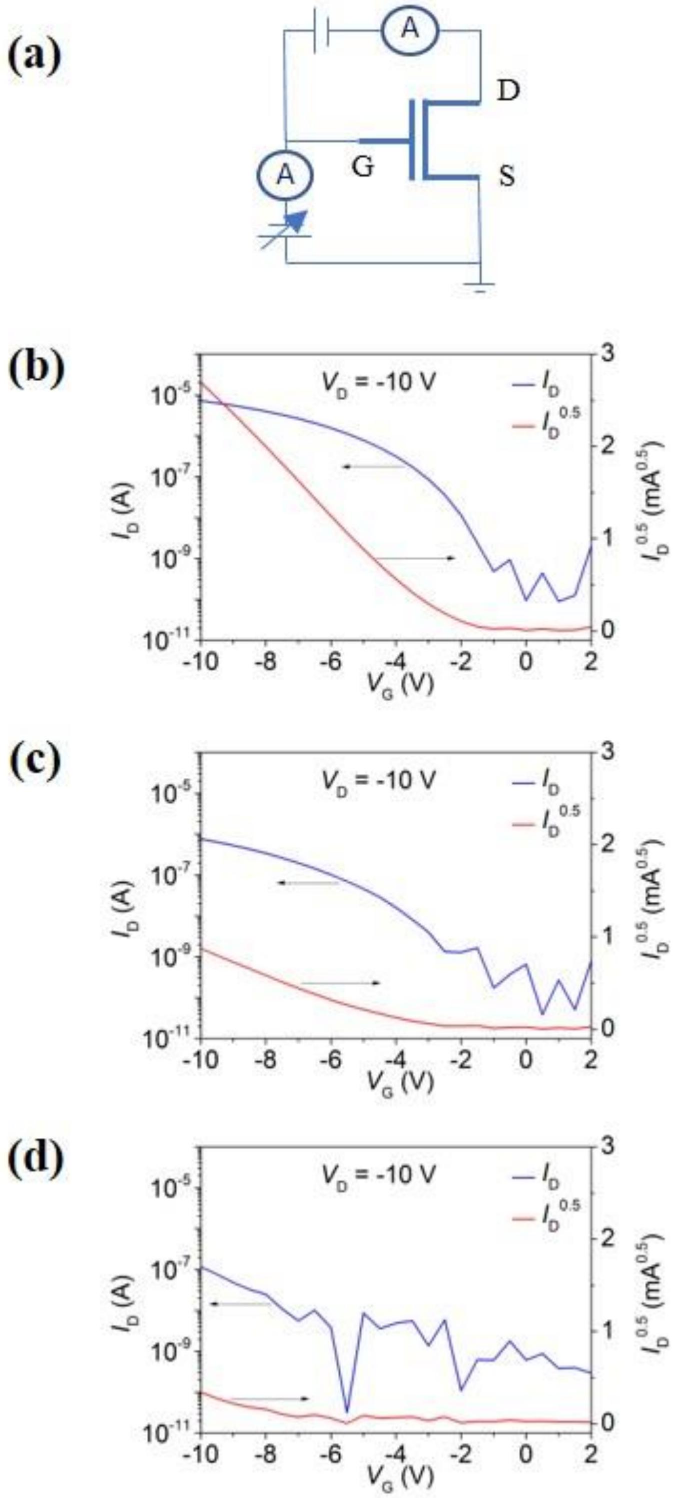

Fig.2.4. (a) Tantamount circuit for transfer characteristics, the transfer curves of OFET with (b) Cu electrodes deposited under a pressure of 2.5×10^{-5} Torr, with (c) gold and Cu (d) electrodes deposited under pressure of 1.6×10^{-6} Torr.

For a transfer characteristics measurement, a voltage sweeping from 2 to -10 V was applied to the gate with a step of -0.5 V while a voltage applied to the D electrode was kept at -10 V (Fig. 2.4. (a)). The μ of devices were calculated from the saturated regime, using the conventional metal-oxide- semiconductor equation[19]:

$$I_{D,sat} = \frac{WC_i}{2L}\mu(V_G - V_{th})^2$$

where $I_{D,sat}$ is the saturated drain current, W and L are the length and width of the channel. C_i is the capacitance per unit area of the gate dielectric. In our OFETs, the gate capacitor could be considered as the Cytop capacitor in serial connection with the SiO_2 capacitor. Thus, C_i could be estimated to be 8.25 nF/cm^2 from their thickness and the permittivity of Cytop and SiO_2. The electrical characteristics of all transistors were calculated and summarized in the table 2.1. The Cu electrode OFET fabricated under high pressure has the best electrical characteristics with the μ of 0.13 cm^2 V^{-1} s^{-1}, the V_{th} of -2.56 V and an on/off ratio of 8.13 × 10^4. The μ of this OFET is c.a. 2 times and c.a. 3 times greater than that of the OFETs with gold and Cu electrodes fabricated under low pressure, respectively. Moreover, the reduction in V_{th} of 0.75 V and 5.54 V is also observed. Thus, it is clear that the OFETs with Cu electrodes fabricated under high pressure have the best performance.

Table 2.1. OFETs parameters

Metal for electrodes	Background pressure for S/D deposition (Torr)	μ (cm^2 V^{-1} s^{-1})	V_{th} (V)	On/off ratio
Copper	2.5 × 10^{-5}	0.13	-2.56	8.13 × 10^4
Gold	1.6 × 10^{-6}	0.05	-3.31	3.76 × 10^5
Copper	1.6 × 10^{-6}	0.04	-8.10	6.05 × 10^3

2.4. Effect of background pressure on a contact resistance reduction

In the previous section, the effect of background pressure on the performance of OFETs was observed. The OFETs with Cu electrodes fabricated under high background pressure of 2.5×10^{-5} Torr exhibited the highest μ and the lowest V_{th} compared with those of OFETs with gold and Cu electrodes fabricated under low background pressure of 1.6×10^{-6} Torr. Because all the OFETs had the same fabrication process, an enhance of the OFET performance is not caused by the modification of the dielectric layer. We supposed that the change in the contact resistance (R_C) is the origin of this effect.

In order to examine the R_C of OFETs, the transmission line method (TLM) is normally used[20,21]. By this method, a relationship between the length of channel (L) and the total resistance (R_T) was determined from some the R_C of OFETs with the different L. Based on this relationship, the R_C was estimated to be $R_T/2$ corresponding to an extreme small of L. However, in our study, TLM method could not be used due to the fixed geometry of L in our devices.

Here we assume that a resistance of the channel (R_{ch}) would have an identical value, because all transistors were fabricated under the same architecture with the same L, W and the same thickness of pentacene layer. Thus, the change in R_T will corresponds to the change in the R_C[18]. Fig. 2.5 shows the total resistances of the OFETs. As can be seen, the resistance of the OFETs with Cu electrodes fabricated under high pressure showed the lowest resistance. This suggest that these OFETs would have the lowest charge injection barrier, which caused the higher μ than that of other OFETs.

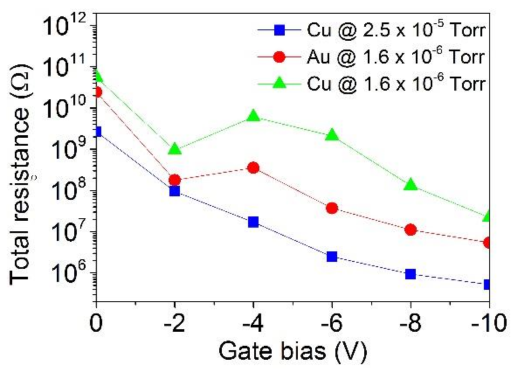

Fig.2.5. Total resistance of OFETs channel as a function of gate voltage

2.5. An origin of the reduction of contact resistance

2.5.1. The contact resistance reduction due to an existence of CuO between the pentacene layer and Cu electrodes

To deeply understand the reduction of contact resistance of OFETs, an X-ray photoelectron microscopy (XPS) was carried out to investigated an existence of CuO. In the case of Cu deposited at high background pressure, we assume that a few Cu atoms could oxidize with oxygen which remained in the chamber of the evaporation machine. These molecules of CuO would exist between the pentacene layer and Cu electrodes, resulting in the reduction of contact resistance of OFETs, which was reported in the literature[17].

The depth profile measurement of XPS for S/D electrodes and pentacene were performed, where a beam of Ar^+ ions was used to dig from the electrodes, followed by the XPS measurement. This procedure was repeated until signals of both C and Cu were obtained at the same time, which corresponds to the spectra at the interface between Cu electrodes and the pentacene layer. Fig. 2.6 shows the XPS spectra at the interface. In Fig 2.6. (a), there is no obvious shift in C 1s peak so that there is no chemical reaction of pentacene at the interface. Thus, the enhancement of μ of the OFETs using Cu electrodes does not come from a chemical reaction between Cu and pentacene. On the other hand, Fig 2.6. (b) and (c) do not show the existence of both Cu^{2+} ions and oxygen which are presented by peaks in XPS spectra at a binding energy of 963.3, 942.4, 944.6 and 530.0 eV 22. Thus, the existence of CuO could not be observed at the interface. In this case, I assume that this might be due to the weak signal to detect.

2.5.2. The contact resistance reduction due to a penetration of oxygen into the pentacene

Another possibility for the contact resistance reduction is a penetration of oxygen into the pentacene layer during deposition, which was reported by Vollmer et al. in 2005[23]. It was reported that oxygen exposure lowers the hole injection barrier at the interface between gold and pentacene. At high pressure, oxygen which remained in the chamber might penetrate into the pentacene layer. This may cause a reduction

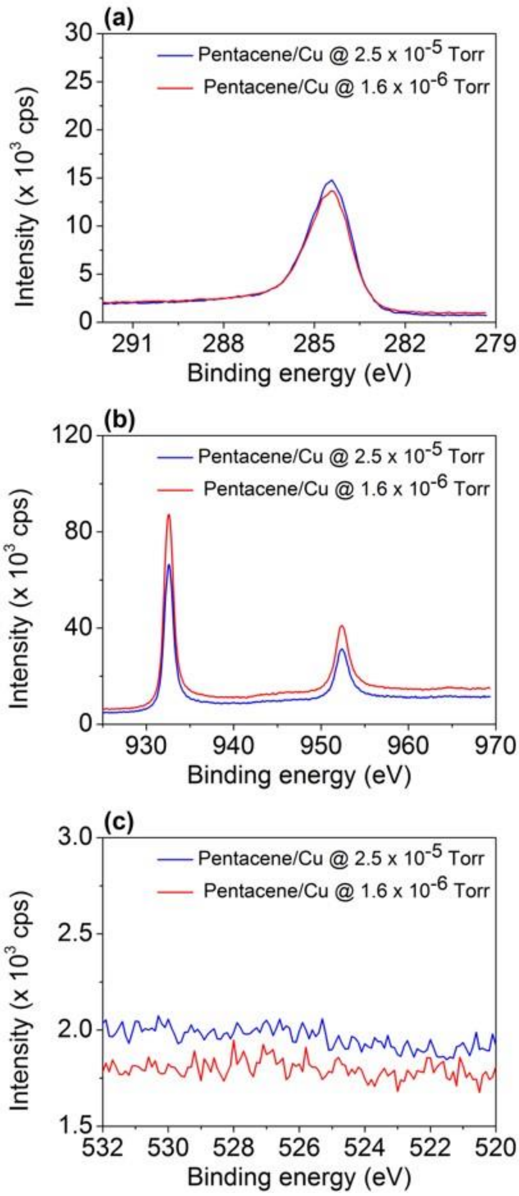

Fig.2.6. X-ray photoelectron spectroscopy. The C 1s spectrum (a), Cu 2p spectrum (b), and O 1s spectrum (c) at pentacene/Cu interface of samples, which fabricated at 2.5×10^{-5} Torr and 1.6×10^{-6} Torr.

of hole injection barrier, which is similar to that of gold/pentacene interface. This could cause the reduction of contact resistance in OFETs, and correspond to the high in the μ.

To clarify an effect on oxygen on the μ of the OFETs, other OFETs were fabricated, which were exposed to ambient air for 1 h before electrodes fabrication at

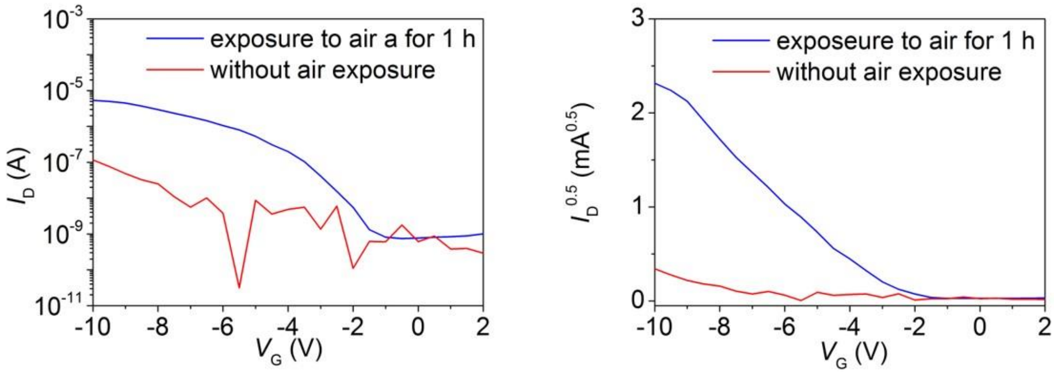

Fig.2.7. The transfer curves of the OFETs with Cu electrodes deposited at a pressure of 1.6×10^{-6} Torr (V_D = -10 V).

a low pressure of 1.6×10^{-6} Torr. As shown in Fig. 2.7, the OFET with air exposure before S/D Cu electrodes fabrication shows the better performance than that of the devices without air exposure. The electrical characteristics of these OFETs were calculated and summarized in the table 2.2. Based on this result, the effect of oxygen on the μ of OFETs was confirmed. Thus, we conclude that the reduction of contact resistance of OFETs could be due to the penetration of oxygen into the pentacene layer, which corresponds to the high μ in our OFETs

Table 2.2. Parameters of OFETs with copper electrodes deposited at a pressure of 1.6×10^{-6} Torr.

OFETs	μ (cm^2 V^{-1} s^{-1})	V_{th} (V)	On/off ratio
With air exposure for 1 h	0.13	-3.24	7.19×10^3
Without air exposure	0.04	-8.10	6.05×10^3

2.6. Conclusions

In summary, we reported the effect of deposition pressure on the performance of OFETs using copper as source/drain electrodes. These OFETs with copper electrodes fabricated at high pressure exhibit better performance compared with conventional gold- or copper-based devices. The reason for the μ enhancement of our OFETs could be due to the charge injection barrier reduction, which caused by the penetration of oxygen into pentacene layer during deposition under high pressure. A mechanism of background pressure effects on the performance of OFETs using copper electrodes has not been clearly understood yet. However, we believe this result would be helpful for improving OFETs performance using a simple method which could be applied in industrial applications.

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CHAPTER 3 || WRITE-ONCE-READ-MANY MLC MEMORY OFETS USING POLY (VINYL CINAMMATE) AS CHARGE TRAPPING LAYER*

A thin layer of poly (vinyl cinnamate) (PVCN) was used as a charge trapping layer in a pentacene OFET. The memory characteristics of the devices showed a non-volatile write-once-read-many memory behavior with the shifts of the threshold voltage of approximately 9, 17, 27 V after applying the programming voltages of -160, -180, and -200 V for 3 seconds, respectively. The memory OFETs with an on/off ratio of 10^5 exhibited stable logic states with retention time of 11,000 seconds. The memory effect in this OFET is ascribed to trapped holes at the interface between PVCN and silicon dioxide (SiO_2) layer. An ultraviolet photoelectron spectroscopy (UPS) and an ultraviolet-visible spectroscopy (UV-Vis) measurements were carried out to estimate the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) of PVCN. Based on this result, the operation mechanism was proposed.

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3.1. Introduction

In previous chapters, both the advantages and the disadvantages of organic MLC memories were discussed. Although resistor-[1,2] and capacitor-based[3,4] MLC memories exhibited a low operation voltage, the use of these memories required external circuit of a diode[5], or a transistor[6,7]. These structures may require a high-cost and complicated fabrication with 2 components in each cell. Thus, the transistor-based MLC memory OFETs have been attracted attention even if they operate at high voltage. From this point of this dissertation, I would like to focus on this structure of MLC devices.

In a charge trapping memory OFET, a thin film layer of polymer such as PαMS[8,9], PS[10], PVA[10,11], PMMA[12], Cytop[13] was inserted between dielectric layer and an active layer. Under an applied electric field, charges are injected from the S/D electrodes and trapped. The trapped charges would induce a change in the I_D or a shift of the V_{th} of memory OFETs, which still remain after electric field removal. This causes the memory effect in the OFETs.

A MLC memory effect in the OFETs is presented by several ON states of OFETs, which are obtained by applying different voltages. Guo et al. reported MLC memory OFETs based on a semiconductor of pentacene or copper phthalocyaine (CuPc)[14]. For the charge trapping layer, PS or PMMA could be used. The OFET using a trapping layer of PS showed a p-type behavior with the μ of 0.52 cm^2 V^{-1} s^{-1}, the V_{th} of -20 V and the on/off ratio of 10^6. In this memory, 7 level of ON states could be obtained. However, the programming/erasing operation required an assisted light source for the reduction of programming/erasing voltages. This requirement caused a limitation for its usage. In 2013, Chiu et al. reported write-once-read-many MLC memory OFET using a n-type semiconductor of N,N'-bis(2-phenylethyl)perylene-3,4,9,10-bis (dicarbonximide) and the charge trapping layer of a star-shaped poly((4-diphenylamino) benzyl methacrylate (star-PTPMA)[15]. However, the programming voltage up to 200 V was used to operate this memory. Recently, another MLC memory OFETs with the charge trapping structure was reported by Zang et al. in 2016[16]. This device used the new material of polyquinoline (PQ) to trap electrons in a pentacene transistor. These trapped electrons caused a hysteresis in the transfer curve, which corresponded to the MLC effect. The programming voltage in this memory was reduced to 100 V. However, the difference in I_D between some logic states was only an order of 2. In addition, the on and off current decay strongly after 300 cycles of reading. In general, the MLC memory OFET with the charge trapping structure has required high operation and programming voltages to inject charges from the electrodes. However, only few devices were reported. It motivates us to develop a new device using new material for charge trapping layer.

Poly (vinyl cinnamate) (PVCN) is a polymer which is used as the dielectric layer of the OFET[17]. This OFET is hysteresis-free because PVCN is hydroxyl group-free. After photo-crosslinking, the film of PVCN was robust even being immersed in developing solution. Thus, this material is promising for solution processing fabrication.

When PVCN was used as a charge trapping layer in a pentacene transistor, the OFET showed a p-type characteristic with the μ of 0.29 cm^2 V^{-1} s^{-1}, the V_{th} of -11.54 V and the on/off ratio of 2.53×10^5. The OFET was found to exhibit a memory effect, those shifts of the V_{th} was controllable. The memory window (ΔV_{th}) of approximately 9, 17, 27 V was observed after programming by a voltage of -160, -180, and -200 V for 3 seconds, respectively. The obtained logic states were stable with a trivial shift of the V_{th} even after erasing by a reversed voltage of 200 V for 100 seconds. Hence, this memory showed a write-once-read-many characteristic. The retention measurement was also carried out, which presented stable logic states with more than 11,000 seconds of reading. The origin of memory effect was proposed to be the trapped holes in the PVCN/SiO_2 interface. The details of this memory and its operation mechanism were discussed in this chapter.

3.2. Experimental

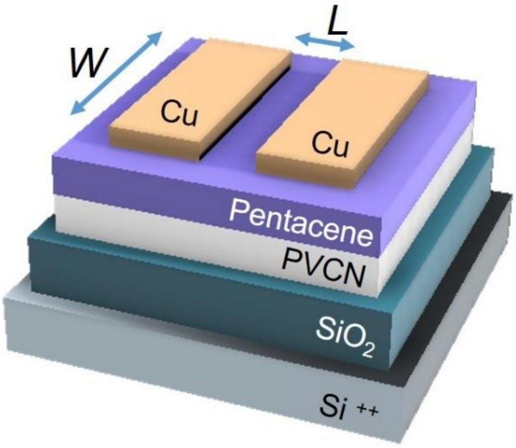

Fig.3.1. Schematic structure of memory OFET with a charge trapping layer of PVCN

Figure 3.1 shows the schematic structure of a memory in this study. The memory OFET was fabricated on a heavily doped silicon wafer (n^+Si, resistivity: 1-10 Ω·cm) coast with a 400-nm thick of silicon dioxide (SiO_2). The substrate was cleaned under the same procedure that described in the chapter 2 (clean ultrasonically in acetone, pure water, IPA sequentially followed by UV-O_3 treatment for 30 min). A layer of PVCN was fabricated by spin-coating onto the SiO_2 surface at a speed of 2,500 rpm for 60 seconds from a solution of PVCN in monochrolobenzene at a concentration of 2.5 mg/ml. Subsequently, the substrates were exposed to ultraviolet light (UV, λ = 254 nm, power = 6 W, AS ONE SLUV-6) for 10 min to produce photo-crosslinking, followed by dried at 140 ºC for 1 h. The thickness of the PVCN layer was measured to be 8 nm using an atomic force microscope (AFM, Keyence VN-8000 nanoscale hybrid microscope). The procedure of cleaning, spin-coating and drying were carried out in a clean booth environment. A 50-nm-thick pentacene layer (Aldrich) was thermally deposited onto the PVCN layer at a deposition rate of 0.3 Å/s under a base pressure of 1.5×10^{-6} Torr. Finally, the copper (Cu) source/drain electrodes were vacuum-evaporated on the top of the pentacene layer through a shadow mask at the pressure of 2.0×10^{-5} Torr and a rate of 0.3Å/s. The thickness of the Cu electrodes was 50 nm. The length (*L*) and width (*W*) of the channel were 50 μm and 2,000 μm, respectively.

To clarify the trapping site in the memory, memory OFETs with a structure of ITO (150 nm)/ PVCN (360 nm)/Pentacene (50 nm)/Cu (50 nm) were fabricated. The pentacene layer and Cu electrodes fabrication processes were similar to those of the Si^{++} /SiO_2 /PVCN /Pentacene /Cu devices.

The electrical characteristics of memory devices were measured using a semiconductor characterization (Keithley) system in the glove box.

3.3. Basic parameters of OFETs

Figure 3.2 (a) and (b) show the output and transfer characteristics of the memory OFETs. For the output characteristics, the I_D of the transistor was measured while the source-drain voltage (V_D) was varied at different gate voltage (V_G). As shown in the Fig. 3.2 (a), our memory OFET exhibited a p-type characteristic with a linear increase of the I_D at low drain voltages (V_D), and its saturation at high V_D, because the conducting channel in the pentacene layer was pinched off.

Figure 3.2 (b) shows the transfer characteristics of the memory OFET. The transfer curves were measured by sweeping V_G from 40 V to -80 V. The field-effect hole mobility (μ) of the devices can be calculated from the saturation regime, using the conventional metal-oxide semiconductor equation[18,19].

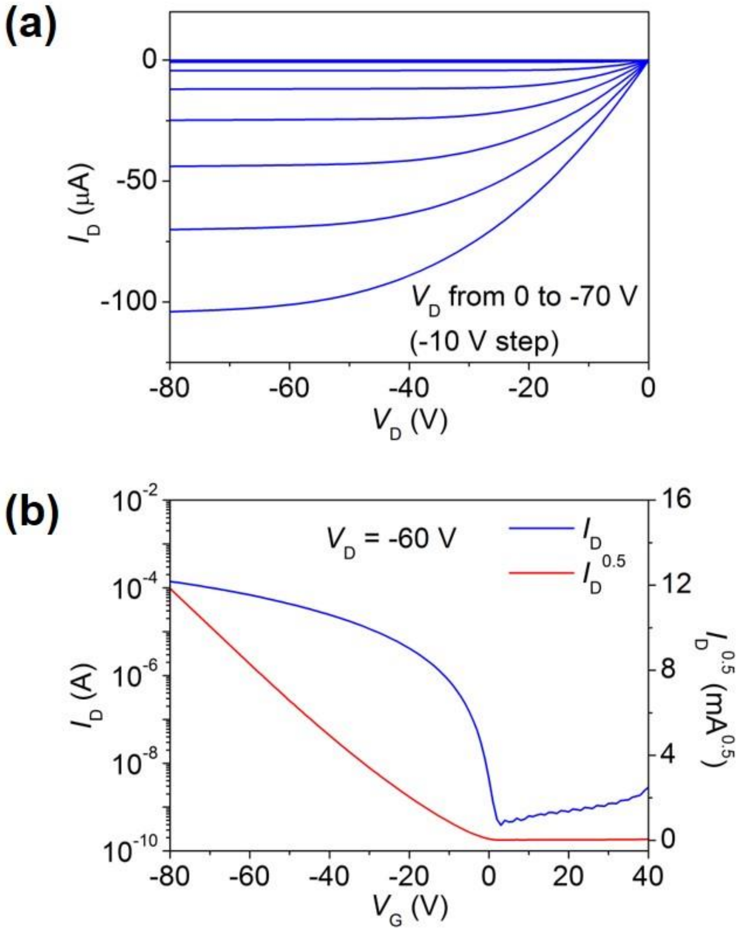

Fig.3.2. (a) Output and (b) transfer curves of the memory OFETs using a charge trapping layer of PVCN.

$$I_{\mathrm{D,sat}} = \frac{WC_{\mathrm{i}}}{2L}\mu(V_{\mathrm{G}} - V_{\mathrm{th}})^2,$$

where $I_{\mathrm{D,sat}}$ is the saturated drain current, W and L are the width and length of the channel, respectively, and C_{i} is the capacitance per unit area of the gate dielectric. The C_{i} of the OFET was estimated to be 8.44 nF·cm^{-2} from the dielectric constants of PVCN (3.37)[17], SiO_2 (3.9)[20] and their thickness. The V_{th} of the memory OFETs was calculated from the intercept of the linear plot of $(I_{\mathrm{D}})^{0.5}$ versus V_{G}. The V_{th}, μ and the on/off ratio were calculated to be -11.54 V, 0.29 cm^2 V^{-1} s^{-1} and 2.53×10^5, respectively. These results indicate that the memory OFETs would have good operational characteristics, when compared with other pentacene OFETs[12,13,21,22].

3.4. MLC memory properties of OFETs

3.4.1. MLC memory effect

The memory effect of the OFETs was observed when a voltage was applied to the gate while the S/D electrodes were connected to the ground. Charges are injected from the S and D electrodes through pentacene layer and trapped at the trapping layer of PVCN, which causes the change in the I_D or the shift of the V_{th} of the OFETs. Fig. 3.3 (a) and (b) show the principle (up) for programming the memory OFETs and the V_{th} shift in the case of electron and hole injection, respectively. For electron injection, a positive voltage (V_{pro}) was applied for 3 seconds. However, no shift of the V_{th} was observed. It indicated that electrons could not be trapped.

In contrast, when a negative voltage was applied, the large shift of the V_{th} was obtained, which was shown in Fig. 3 (b) The direction shift of the V_{th} to the negative V_G region was caused by the increase of trapped holes in the device. Because the

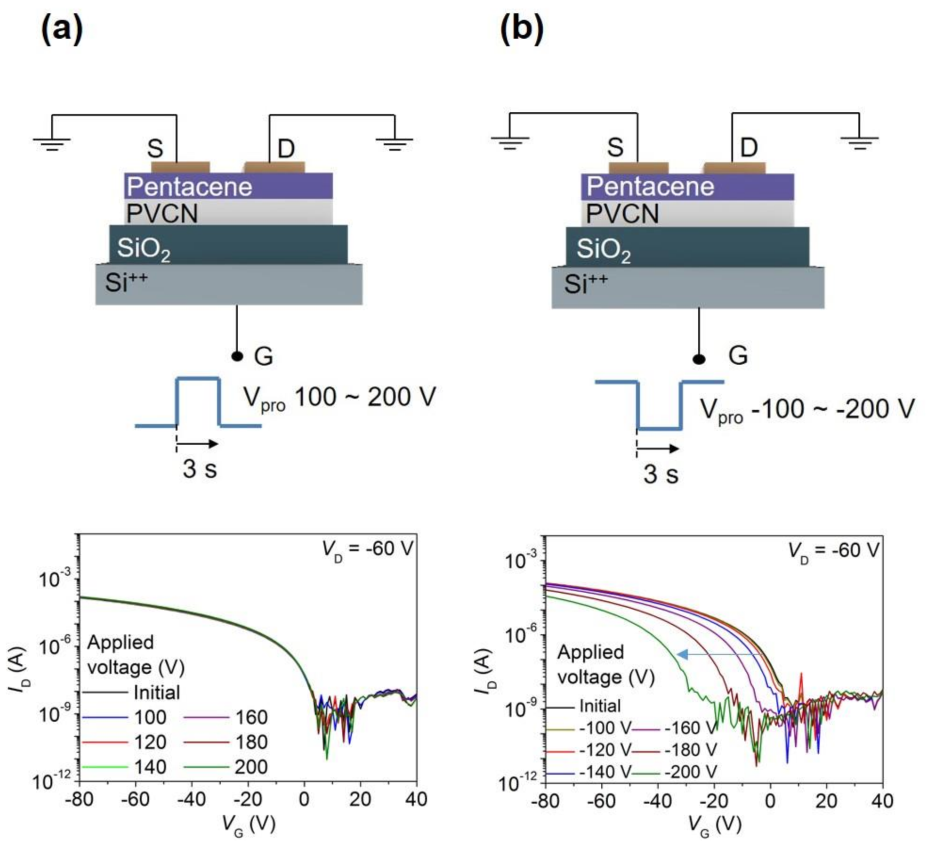

Fig.3.3. The configuration (up) and V_{th} shift (down) of (a) an electron and (b) a hole injection.

transfer curves shifted only by application of negative voltage, we defined a programming voltage is a negative voltage applied to the gate in this memory OFET. The table 3.1. shows the V_{th} after programming. Several ON states could be clearly observed by different programming voltages. It indicates the MLC memory effect in our devices.

Table 3.1. V_{th} after programming

V_{pro} (V)	-160	-170	-180	-190	-200
V_{th} (V)	-20.51	-24.34	-28.48	-33.28	-38.56

3.4.2. Stability of logic states

In a non-volatile memory, the data could be stored via programming (write) process. The stored data should be stable until it was over-written with the new data. To do this, the memory should be erasable. In our memory OFETs, the programmable ability was confirmed by the shift of the V_{th} when the programming voltage was applied (Fig. 3.4 (a)). For erasing the stored data in the memory, a positive voltage was applied to the gate to de-trap the trapped holes. However, a small shift of the V_{th} was observed (Fig. 3.4 (b)), which shown in the table 3.2. The reason why holes could not be de-trapped might be due to their high trap depth. Thus, an electric field caused by the voltage of 200 V was not enough for the de-trapping.

The memory OFETs using PVCN as the charge trapping layer exhibited several ON states. These ON states are stable which could not be erased. Based on

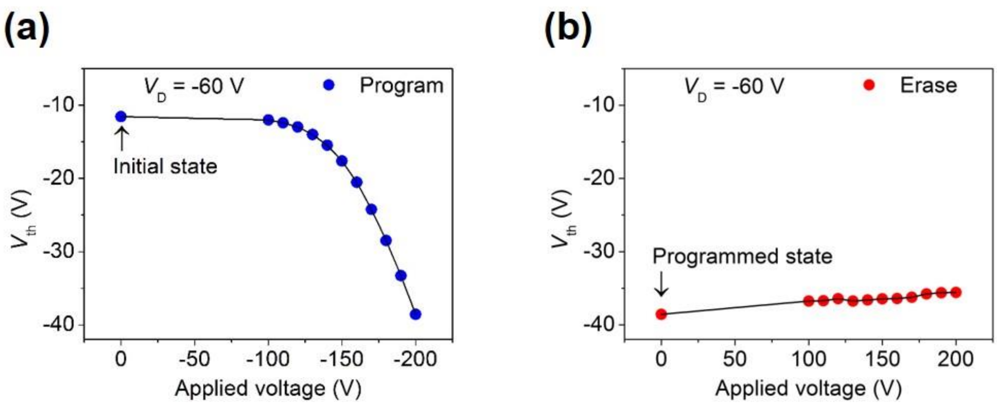

Fig.3.4. The change of V_{th} under different (a) programming and (b) erasing voltages

this result, we confirmed that these memory OFETs behaved as the write-once-read-many memory devices.

Table 3.2. V_{th} after erasing

Erasing voltage (V)	160	170	180	190	200
V_{th} (V)	-36.41	-36.24	-35.78	-35.61	-35.57

3.4.3. Retention characteristics

To investigate a long-term operation of the memory OFETs, the retention measurement was conducted. Four logic states of the memory were presented by the I_D at the V_G of -30 V and the V_D of -60 V from the initial transfer curve and transfer curves after programming at -160, -180 and -200 V for 3 seconds (Fig. 3.5 (a)). At each logic state, the I_D was measured continuously for over 10^4 seconds. As shown in Fig. 3.5 (b), all states were clearly distinguished. The ON/OFF ratio between the logic states of “00” and “11” was 3.52×10^6 and reduced during the reading process. However, the remained ON/OFF ratio was observed to be 4.24×10^5 after more than 10^4 seconds. Thus, our memory OFET are promising to show a long-term operation.

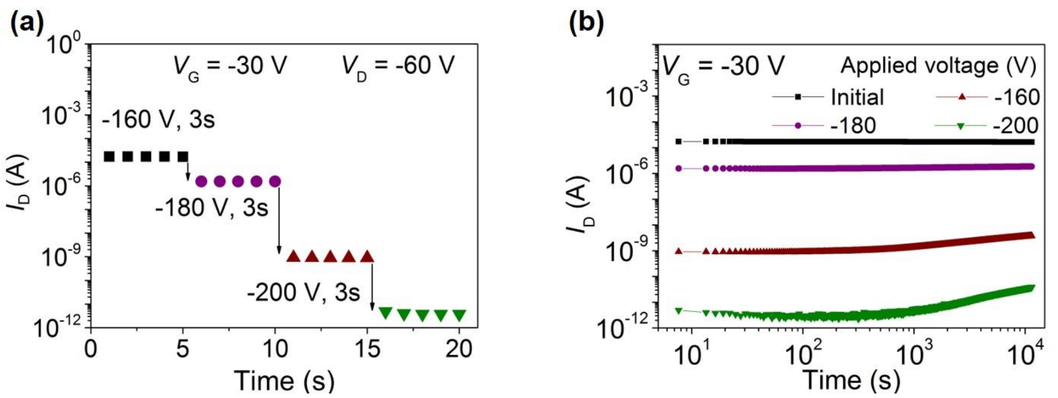

Fig.3.5. (a) Corresponding current after programming and (b) retention characteristics at a V_G of -30 V and V_D of -60 V.

3.5. Mechanism discussions

3.5.1. Trapping sites in the memory OFET

In our memory OFETs, the holes are injected from the electrodes under the programming electric field, then trapped there. The holes could not be injected from the gate electrode due to the insulator of SiO_2. There are 4 possibilities where holes could be trapped: (1) at the pentacene/PVCN interface, (2) inside the PVCN bulk, (3) at the PVCN/SiO_2 interface and (4) inside the SiO_2 thin film bulk.

Organic semiconductor material, which is used in our work, is pentacene. This material is known as a p-type semiconductor, which the dominant charge carriers are the holes. Thus, the first possibility of hole trapping site (at pentacene/PVCN interface) is seemed to be unsuitable. To clarify this point as well as to examine the possibility of hole trapping site at the PVCN bulk, a OFET with a structure of a glass substrate/indium tin oxide (ITO) (150 nm)/PVCN (360 nm)/Pentacene (50 nm)/Cu (50nm) (PVCN-OFET)) was fabricated under the same fabrication process. The 360 nm-thick of PVCN was fabricated by spin-coating a solution of PVCN 0.1 g/ml in monochlorobenzene at 2,500 rpm for 30 seconds, followed by UV exposure for 20 min and drying at 140°C for 1 h. The thickness of the PVCN layer was measured using an atomic force microscope (AFM, Keyence VN-8000 nanoscale hybrid microscope). When an electric field of -3.9 MV·cm^{-1}, which corresponds to an applied voltage of -180 V in our memory transistors, was applied to the PVCN-OFET, the measured

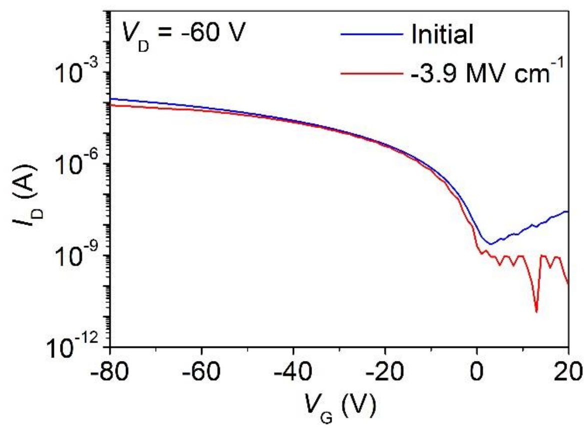

Fig.3.6. The transfer curves of PVCN-OFET at initial and after programming by an electric field of -3.9 MV·cm^{-1} at V_D of -60 V.

transfer curve was seemed not to shift (Fig. 3.6). It indicated that the holes could not be trapped both at the interface between the pentacene and the PVCN layer, and inside the PVCN bulk. This conclusion is in agreement in some other reports[13,23]. Thus, the trapping sites, which noticed in the possibilities (1) and (2) are denied.

In the case of trapped charges at SiO_2 layer, there are many researches on this topic since decades. Electrons[24-26] and holes[27-31] could be injected and trapped at a thin layer of SiO_2. However, these charge injections required to be taken in a condition using high energy source under vacuum atmosphere. Meanwhile, the hole injection in our memory was taken in room condition. Thus, we supposed that holes could not be trapped in our case. This assumption will eliminate the possibility (4) of hole trapping site, which listed above.

Based on these analysis, we concluded that holes are injected from S/D electrodes, travelled through pentacene layer and trapped at PVCN/SiO_2 interface, corresponded to the memory effect in our OFETs.

3.5.2. Operation mechanism

The operation mechanism of the memory OFETs could be explained based on the diagram of level energy. The lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO) of pentacene, PVCN and SiO_2 should be found in order to build this diagram.

The work function of Cu was found to be -4.6 eV[32] and LUMO, HOMO energy level of pentacene were -3.2 and -5.0 eV, respectively[33]. The SiO_2 is known as an insulator with a high bandgap. In a report by Zhang et al.[16], the LUMO energy level and the bandgap of the SiO_2 was -0.95 and 8~9 eV.

For the HOMO and LUMO energy level of PVCN detections, an ultraviolet photoelectron spectroscopy (UPS) and ultraviolet visible spectroscopy (UV-Vis) were carried out. Fig. 3.7 (a) shows the UPS spectra of a 7 nm-thick layer of PVCN prepared on a gold substrate. The UPS measurement used the lamp source He I with $h \cdot \nu$ of 21.2 eV. Based on the UPS spectra, the HOMO level was estimated to be -6.9 eV. On the other hand, the bandgap (E_g) of PVCN was calculated from the Tauc's plot (Fig. 3.7 (b)), which was obtained from the UV-Vis spectra[34]. The bandgap of PVCN is 4.0 eV. Hence, the LUMO energy level of PVCN is calculated to be -2.9 eV.

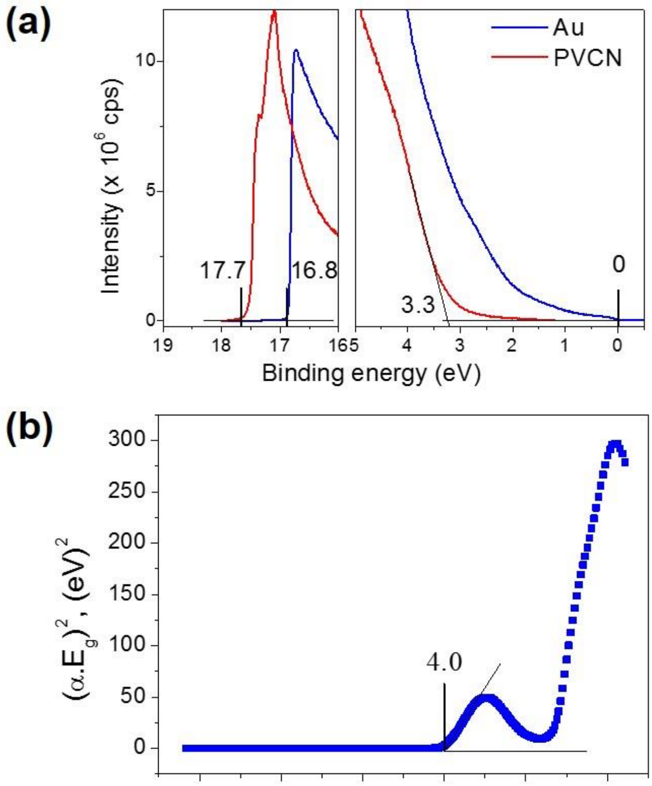

Fig.3.7. (a) UPS spectra of a thin layer of PVCN prepared on a layer of gold. (b) The Tauc's plot extract from the UV-Vis spectra of PVCN material.

Figure 3.8 shows the energy diagram of holes transfer and trapping between layers in our memory OFET. When a positive voltage was applied to the gate, electrons may not be injected due to the electron injection barrier between the Fermi level of the Cu electrode and the LUMO level of pentacene; or may be injected but could not be trapped because there is no trapped site. In the case of holes injection by negative voltagte (programming voltage), holes could be injected and trapped. The high hole injection barrier between the LUMO level of pentacene and that of PVCN may be the explaination for the high programming voltage which used in our devices. The number of trapped hole per area (ΔP) were estimated using the equation $\Delta P = C_i \cdot \Delta V_{th}/q$,[35] where C_i is the capacitance per area of gate dielectric, q is elementary charge, and ΔV_{th} is the V_{th} shift. The ΔP increased propotionally with the programming voltage increasement (Table 3.3), which related to the difference in the logic states. When erasing the devices, we supposed that the holes may are trapped at the PVCN/SiO_2 interface with a deep trapping site. Thus, it could not be de-trapped via a reversed electrical field application.

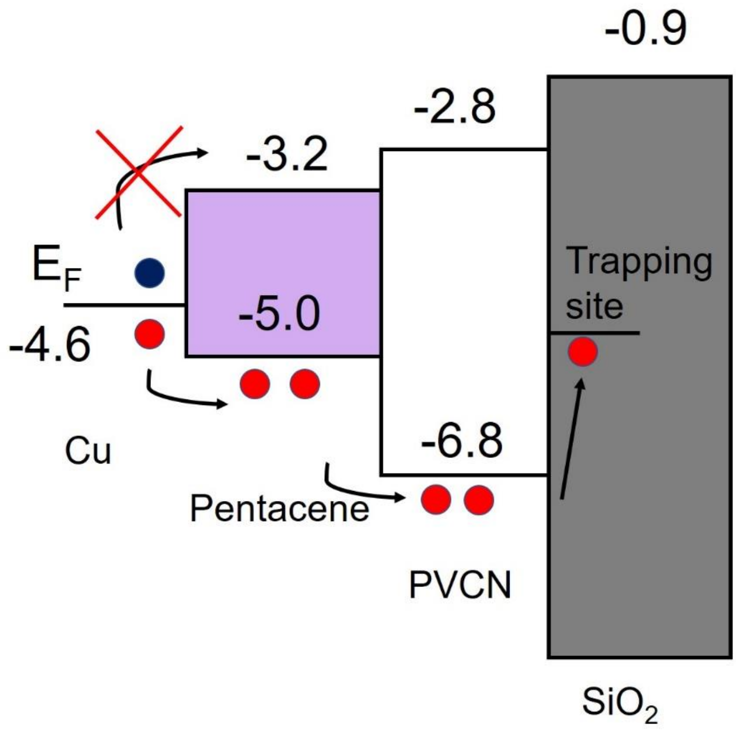

Fig.3.8. Schemes for hole transfer and trapping between PVCN and SiO_2 layer

Although the trapping mechanism of holes at the interface between the PVCN and the SiO_2 layer is still limited, the proposed mechanism above could be used to explain the memory behavior in our OFETs.

Table 3.3. Numbers of trapped holes under different programming conditions

V_{pro}, 3 s (V)	ΔV_{th} (V)	ΔP (cm^{-2})
-160	9	4.97×10^{11}
-180	17	9.38×10^{11}
-200	27	1.49×10^{12}

3.6. Conclusion

In this chapter, we reported a write-once-read-many MLC memory OFET. This memory OFET used a thin film of PVCN as the charge trapping layer. The OFET showed a p-type characteristic with the μ of 0.29 $cm^2 V^{-1} s^{-1}$, the V_{th} of -11.54 V and the on/off ratio of 2.53×10^5. Under the programming voltage of -160, -180 and -200 V for 3 seconds, the ΔV_{th} of 9, 17 and 27 V were observed. Each logic states, which was represented by the I_D, are stable for a long retention time up to 10^4 s. This memory effect is caused by the trapped holes at the PVCN/SiO_2 interface. The understanding of hole trap mechanism is still limited. However, the operation mechanism of the devices was discussed at the end of this part. We believe that this study could be helpful for a development of a write-once-read-many MLC non-volatile memory OFET with a reasonable cost.

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CHAPTER 4 || MLC ORGANIC MEMORY TRANSISTOR USING LITHIUM-ION-ENCAPSULATED FULLERENE AS CHARGE TRAPPING LAYER*

We report on multi-level non-volatile organic transistor-based memory using pentacene semiconductor and a lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as a charge trapping layer. Memory organic field-effect transistors (OFETs) with a $Si^{++}/SiO_2/Li^+@C_{60}$/Cytop/Pentacene/Cu structure exhibited a performance of p-type transistor with a threshold voltage (V_{th}) of -5.98 V and a mobility (μ) of 0.84 cm^2 V^{-1} s^{-1}. The multi-level memory OFETs exhibited memory windows (ΔV_{th}) of approximate 10 V, 16 V, and 32 V, with a programming gate voltage of 150 V for 0.5 s, 5 s, and 50 s, and an erasing gate voltage of -150 V for 0.17 s, 1.7 s, and 17 s, respectively. Four logic states were clearly distinguishable in our multi-level memory, and its data could be programmed or erased many times. The multi-level memory effect in our OFETs is ascribed to the electron-trapping ability of the $Li^+@C_{60}$ layer.

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4.1. Introduction

In previous chapters, we briefly introduced 1-bit and MLC memories including its structures, basic operation mechanism. We also reported a simple method to enhance the performance of OFETs for memory applications based on an effect of background pressure during copper deposition. As one of targets of this dissertation, we reported a write-once-read-many MLC memory OFET using a thin film of PVCN as charge trapping layer. In this memory, the memory window of 9, 17, and 27 V were observed when a programming voltage of -160, -180 and -200 V was applied to the gate for 3 seconds. Four stable states of this memory OFET could be distinguished after a long retention time of over 10^4 seconds. Although there are some disadvantages such as high operation or programming voltages and unerasable storage data, this study could be meaning somewhere due to not much researches on charge trapping MLC memory OFETs.

To solve the issue of high operation/programming voltages, a reduction of dielectric layer (SiO_2) could be used. However, our further target is a MLC OFET memory which stored data could be read/written many times. To do this, charges must be trapped and de-trapped at the trapping layer by using the programming and the reversed voltages. In addition, numbers of trapped charges should be controllable to obtain several ON states in the MLC devices.

As introduced in chapter 3, Guo et al. reported MLC memory OFETs based on the semiconductor of pentacene or copper phthalocyaine (CuPc)[1]. For the charge trapping layer, PS or PMMA could be used. Beside the use of PS or PMMA, only the use of polyquinoline (PQ) was reported[2]. It seems to be that the lack of material for charge trapping layer is a reason why just a few researches on MLC memory OFET based on charge trapping structure have been reported. Thus, an application of new material for charge trapping plays an important role for the MLC memory OFET development.

Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) contains a Li cation inside a fullerene cage. This material could be a potentially interesting material for the charge trapping layer of MLC memories, because of its multiple oxidation/reduction peaks observed in cyclic voltammogram[3]. In addition, its three-fold degenerated lowest unoccupied molecular orbital (LUMO) is expected to accept up to six electrons, and the number of electrons injected into the $Li^+@C_{60}$ can be controlled by an applied voltage[3,4]. Moreover, $Li^+@C_{60}$ has higher electron acceptability than pristine C_{60}[5,6] indicating a higher stability of the trapped electrons. Therefore, there is much potential in the use of $Li^+@C_{60}$ as an electron trapping material to fabricate MLC memories.

A multi-level memory OFET using $Li^+@C_{60}$ as charge trapping layer was investigated and reported in this chapter, which is the main goal of my dissertation. Clear differences in four logic states (one erased state and three programed states) can be obtained using $Li^+@C_{60}$ as the charge trapping layer. The shifts in the V_{th} (ΔV_{th}) from the erased state defining each of the programmed states were approximately 10 V, 16 V, and 32 V, obtained with a programing voltage of 150 V for 0.5 s, 5 s, and 50 s, respectively. These states accurately returned to the erased state by application of a voltage of -150 V for 0.17 s, 1.7 s, and 17 s, respectively. The term of multi-level is used instead of the term of MLC because the logic state change in MLC memory is caused by different voltages with a fix duration, which differs than that in our study. The repeatability of these shifts was confirmed by endurance cycle testing the device. The multi-level effect in our devices was attributed to the multiple oxidation/reduction peaks in cyclic voltammogram of the $Li^+@C_{60}$ layer. The mechanism operation of the memory will be analyzed in the next chapter of this dissertation.

4.2. Experimental

Figure 4.1 shows a schematic illustration of the memory OFETs used in our study. These multi-level memory OFETs were fabricated using heavily doped silicon wafers (n^+Si, resistivity: 1–10 Ω·cm) coated with a 400-nm SiO_2 film. These wafers were cleaned follows a procedure which described in previous chapters with acetone, pure water and IPA, and subsequently subjected to UV-O_3 treatment for 30 min. The salt of $Li^+@C_{60}$ bis(trifluoromethylsulfonyl)imide ($Li^+@C_{60}$ NTf_2^-) was purchased from Idea International Co. Ltd. This layer was fabricated by spin-coating onto the SiO_2 at 1,000 rpm for 30 s, using a solution of $Li^+@C_{60}$ NTf_2^- salt in chlorobenzene at a concentration of 2.4 mg/ml, and dried at 140 °C for 30 min. Then, a 10-nm-thick CYTOP layer (Asahi Glass) was spin-coated at 2500 rpm for 60 s, using a 0.5 wt % CYTOP solution, and dried at 100 °C for 2 h. The thickness of the CYTOP layer was measured by atomic force microscopy (AFM). A 50-nm-thick pentacene layer (Aldrich) was thermally deposited onto the CYTOP layer at a pressure of 1.6×10^{-6} Torr and a deposition rate of 0.3 Å/s. The copper (Cu) source/drain electrodes were deposited on the pentacene layer through a shadow mask, at a pressure of 2.5×10^{-5}

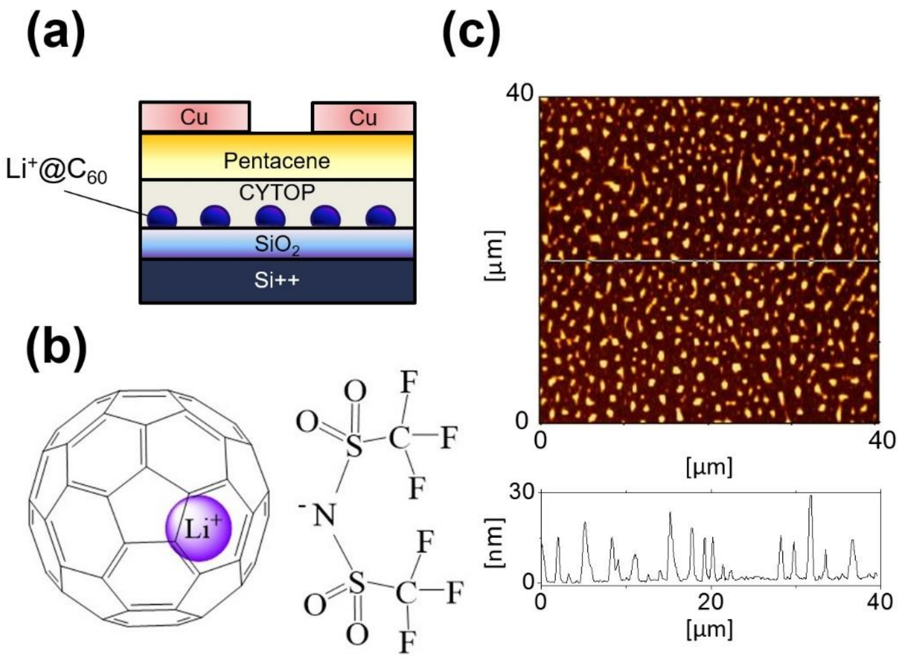

Fig.4.1. (a) Schematic illustration of the cross section of a memory OFET, (b) chemical structure of $Li^+@C_{60}$, and (c) AFM topographic image with a cross section profile of the $Li^+@C_{60}$ surface.

Torr and a rate of 0.3 Å/s. The length (L) and width (W) of the channel were 50 μm and 2000 μm, respectively. The thickness of the Cu electrodes was 50 nm.

The capacitance per unit area of the gate dielectric (C_i) was measured in a sample with a device structure of Si^{++}/SiO_2 (400 nm)/Li^+@C_{60}/Cytop (10 nm)/Cu (50 nm) (0.014 cm^2 area) using an Agilent 4284A LCR meter.

For comparison, memory OFETs without the Li^+@C_{60} were also fabricated.

The electrical characteristics of the memory devices were measured with a semiconductor characterization system (Keithley) in a dry nitrogen atmosphere, at room temperature.

4.3. Basic parameters of OFETs

The output characteristics of the memory OFET are shown in Fig. 4.2 (a). The drain current (I_D) of transistor was measured while the source-drain voltage (V_D) was varied from 0 to -60 V in -10 V steps, for different gate voltages (V_G). As shown in this figure, the I_D of transistor increased linearly at low drain voltages (V_D), and saturated at high V_D, because the conducting channel in the pentacene layer was pinched off. This curve therefore shows that the OFET behaved as a typical p-channel OFET.

Figure 4. 2 (b) shows the transfer characteristics of the memory OFET and the gate current (I_G) measured during evaluation. The transfer characteristics were

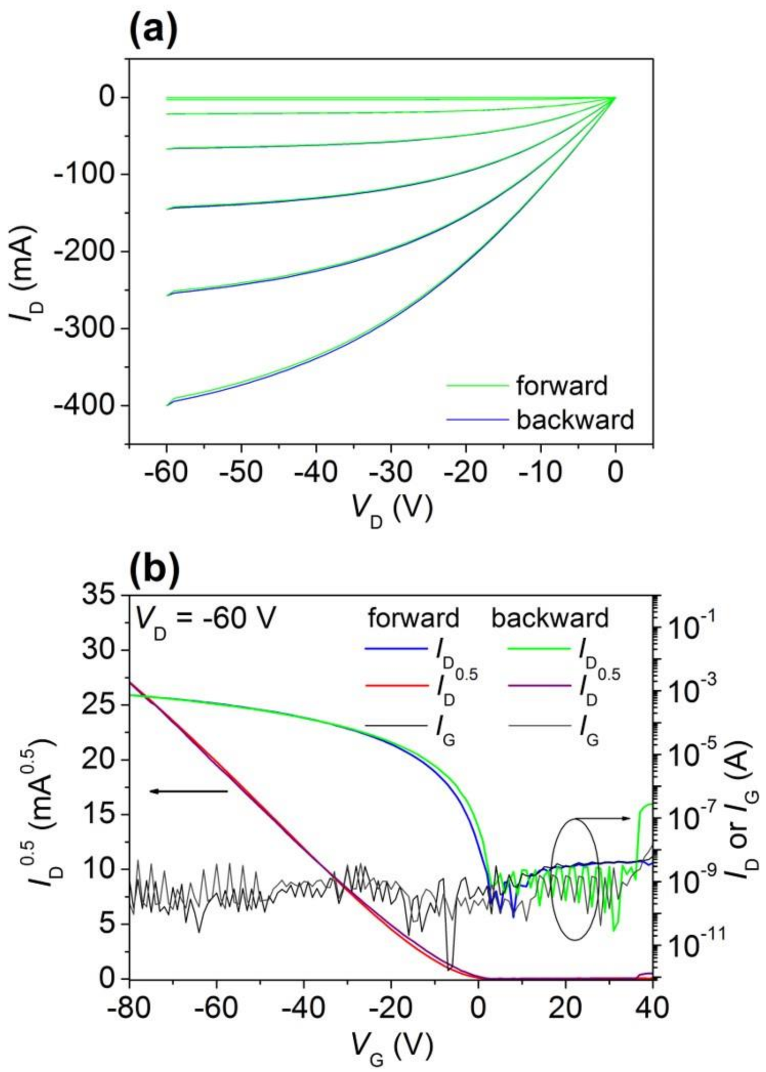

Fig.4.2. Characteristic curves of the memory OFETs at V_D = -60 V. (a) Output characteristics. (b) I_D–V_G, I_G–V_G, and $(I_D)^{0.5}$–V_G curves.

measured by sweeping V_G from 40 V to -80 V. The field-effect hole mobility (μ) of the devices can be calculated from the saturation regime, using the conventional metal-oxide semiconductor equation:[7,8]

$$I_{\mathrm{D,sat}} = \frac{WC_{\mathrm{i}}}{2L}\mu(V_{\mathrm{G}} - V_{\mathrm{th}})^2,$$

where $I_{D,sat}$ is the saturated drain current, W and L are the width and length of the channel, respectively, and C_i is the capacitance per unit area of the gate dielectric. The value of C_i for the CYTOP/Li^+@C_{60}/SiO_2 dielectric was 7.8 $nF \cdot cm^{-2}$ at 1 kHz. The V_{th} of the memory OFETs was calculated from the intercept of the linear plot of $(I_D)^{0.5}$ versus V_G. The V_{th}, μ, and the on/off ratio were -5.98 V, 0.84 $cm^2\ V^{-1}\ s^{-1}$, and 2.18×10^5, respectively. In addition, a trivial hysteresis was observed in the characteristics of the OFETs. Thus, the hysteresis in the transfer curve could not be the origin of memory effect that was discussed in the next section.

These results and the low value of I_G indicate that the memory OFETs exhibit good operational characteristics as typical OFETs, when compared with reported pentacene OFETs[9-12].

4.4. MLC memory properties of OFETs

4.4.1. Shift of the V_{th} under programmed/erased conditions

As analyzed in chapter 3, a multi-level memory requires several ON states, which are distinguished by the shift of the V_{th}. The shift of the V_{th} should be controlled by applying different gate programming/erasing voltages.

Figures 4.3 (a)(b) and (c) show the programming and erasing characteristics of our memory OFETs. During programming or erasing, the source and drain electrodes were grounded. Before programming, the OFET was set into erased state by applying a negative voltage of -150 V to the gate for 5 s, which results in V_{th} of -19.79 V (black line). When a voltage of 150 V was applied to the gate for 0.5 s, the transfer curve shifted to the positive V_G region with a V_{th} of -9.99 V (red line),

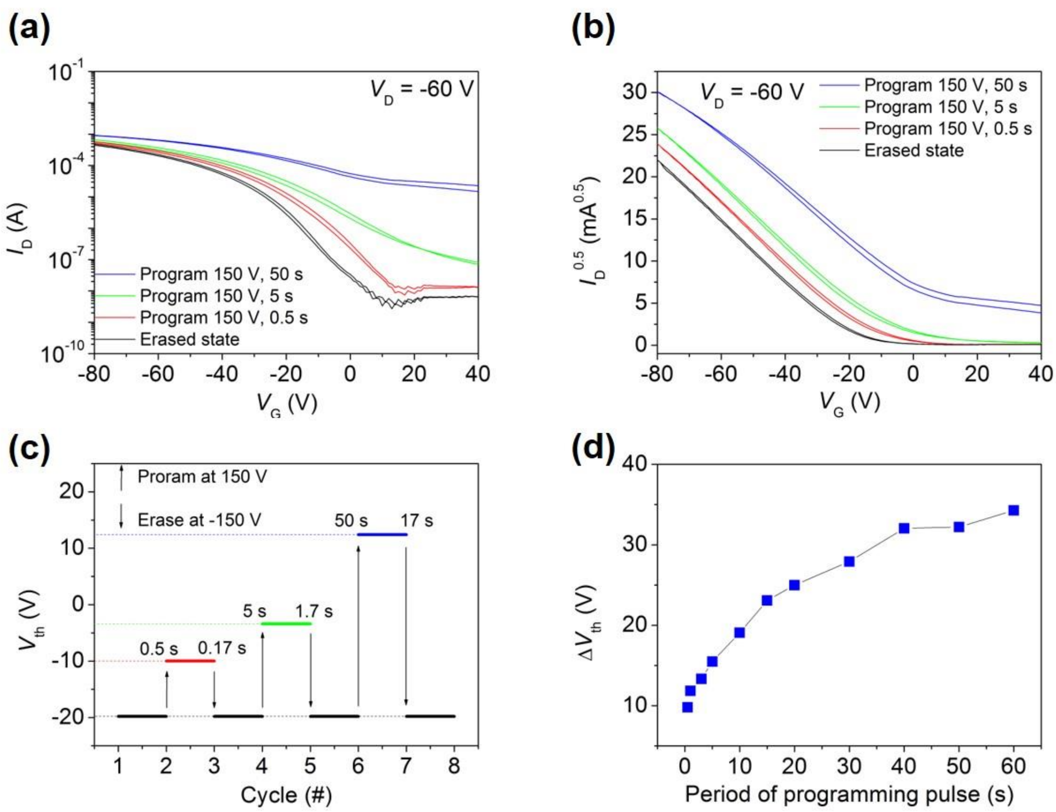

Fig.4.3. (a) I_D–V_G and (b) $(I_D)^{0.5}$–V_G curves of memory OFETs under different programming and erasing conditions. For programming/erasing, a gate pulse voltage of 150 V/-150 V is applied, with the source-drain electrodes connected to the ground. (c) Different V_{th} obtained by applying different gate voltage durations. (d) Shifts of the V_{th} under different programming voltages.

reflecting a memory window (ΔV_{th}) of approximately 10 V. Subsequently, a negative voltage of -150 V was applied to the gate for 0.17 s, to erase memory. The transfer curve shifted back to the erased state. The memory OFETs were then programmed with a voltage of 150 V for 5 s or 50 s, followed by erasing with a voltage of -150 V for 1.7 s or 17 s, respectively. The transfer curve shifted to positions with a V_{th} of -3.40 V (green line) and 12.40 V (blue line), and then returned to the erased state. The estimated values of ΔV_{th} were 16 V and 32 V. Fig. 4.3. (d) shows the change of V_{th} under a programming voltage of 150 V with different pulse durations.

4.4.2. Reproducibility of logic states

Another requirement is the repeatability of the voltage-current curve under the same applied voltage, both for programming and erasing. Repeatability ensures that the different logic states of multi-level memories can be replicated, even after several programming or erasing repetitions.

Figure 4.4 shows the write-read-erase-read cycles of our memory OFETs under repeated programmed and erased states at a read voltage (V_{read}) of -60 V. The repeatability of the magnitude of the I_D for each state indicates that each logic state could be reliably replicated after erasing. However, at each state, a deviation of the I_D

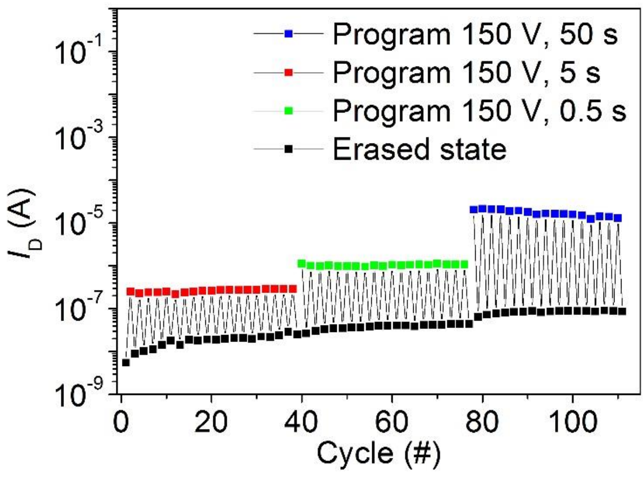

Fig.4.4. Endurance cycles of the memory OFETs

was observed, which would be caused by a hysteresis in transfer curve after programming.

4.4.3. Retention time characteristics

To evaluate the long-term operation of the memory OFETs, the retention times of both the programmed and erased states were measured (Fig. 4.5). After programming and erasing, the I_D of each state was measured for 50,000 seconds, at a V_D of -60 V and a V_G of 0 V. The different logic values were defined by the low I_D (erased state) and high I_D (programmed states) values. A clear difference in logic states was observed for more than 50,000 seconds, which is longer than reported results[13-18]. The I_D of the erased states increased some thousands of seconds later, which may be caused by a chemical interaction between a few $Li^+@C_{60}$ and the pentacene layer. Under the application of the V_D = -60 V to the gate electrode during the long-time operation, a few $Li^+@C_{60}$ cations could migrate to the pentacene layer, according to the electric field.

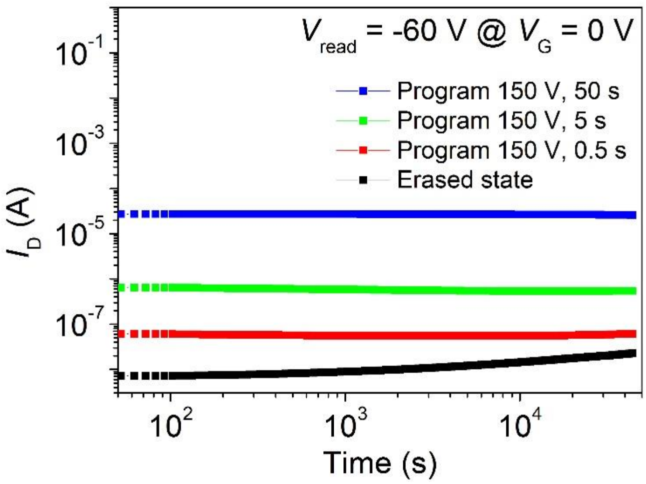

Fig.4.5. Retention characteristics of the memory OFETs

4.5. Proposed operation mechanism

In our memory OFETs, electrons are injected from the S/D electrodes and trapped, which induced the shift of the V_{th} after a programming voltage removal. In this section, electrons trapping site and a proposed operation are discussed.

4.5.1. The electron trapping sites in the memory OFETs

In our memories, when a positive voltage was applied for programming, electrons are injected from the electrodes, and then trapped. There are several possibilities where electrons could be trapped: (1) at the pentacene/Cytop interface, (2) inside Cytop bulk, (3) at the $Li^+@C_{60}$ layer, (4) at the interface between Cytop and SiO_2 and (5) at the SiO_2 bulk.

In 2007, Kalb et al. reported an OFET with a structure of ITO/Cytop /Pentacene/Au, where no shift of the V_{th} was observed under a programming condition of ±70 V for 2 h[19]. It clearly indicated that no electron could be trapped both at the pentacene/Cytop interface and inside Cytop bulk. This result is in line with some previous reported by Dao et al.[20,21] Thus, we eliminated the possibility (1) and (2). In the term of possibility (5), as discussed at chapter 3, there were some reports that electrons could be trapped at a very thin layer of SiO_2[22-24]. However, trapped electrons must be supplied by high energy resource. So that, the possibility (5) was also ruled out as well.

To clarify the origin of the multi-level memory effect of the memory OFETs with $Li^+@C_{60}$, we fabricated OFETs without the $Li^+@C_{60}$ layer, and its memory characteristics was used for comparison. The OFET without the $Li^+@C_{60}$ layer exhibited a performance with the μ of 0.32 $cm^2V^{-1}s^{-1}$, the V_{th} of -11.57 V and the on/off ratio of 7.41×10^5. Under the programming voltage of 150 V, the memory OFETs without the $Li^+@C_{60}$ layer did not show any shift of the transfer curve. It indicated that the memory effect in our multi-level memory OFET does not originate from the trapped electron at the Cytop/SiO_2 interface. The programming voltages were then increased up to 200 V. Figure 4.6 shows the obtained $(I_D)^{0.5}$–V_G curves of the memory OFETs without the $Li^+@C_{60}$ layer at the V_D of -60 V. With the programming voltage of 200 V applied for less than 250 s, the transfer curves were not considerably shifted,

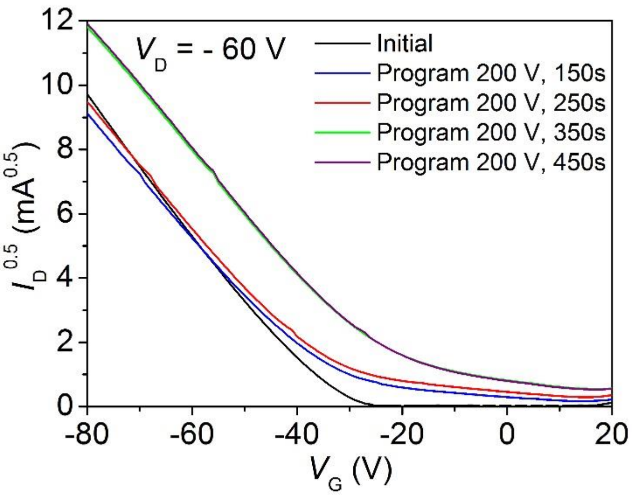

Fig.4.6. $(I_D)^{0.5}$–V_G curves of the memory OFETs without Li^+@C_{60}.

because not many electrons were being trapped by the charge trapping CYTOP layer. After programming for more than 350 s, the number of trapped electrons seemed to increase and then saturate, causing a large shift of the V_{th}. Memory OFETs without the Li^+@C_{60} layer do not therefore show a clear difference in logic states and do not exhibit several ON states required for multi-level memories. However, the memory OFETs without the Li^+@C_{60} layer exhibit a one-bit memory characteristic, which is in line with the results reported by Dao in 2012[20]. The possibility (4) so was denied logically. We therefore conclude that the electron-trapping ability of the Li^+@C_{60} layer is at the origin of the multi-level effect in our memory OFETs.

Based on these results, we concluded that the memory effect in our memory OFET originated from the trapped electrons at Li^+@C_{60} layer due to an applied voltage to the gate. The further investigation in the multi-level memory effect in our devices would be analyzed in the next chapter.

4.5.2. Proposed mechanism

Figure 4.7 shows a proposed mechanism of our memory OFETs. As shown in chapter 3, the work function of Cu was found to be -4.6 eV while the LUMO, HOMO energy level of the pentacene and the Cytop were -3.2, -5.0 eV[25], and -2.8, -9.1 eV[21],

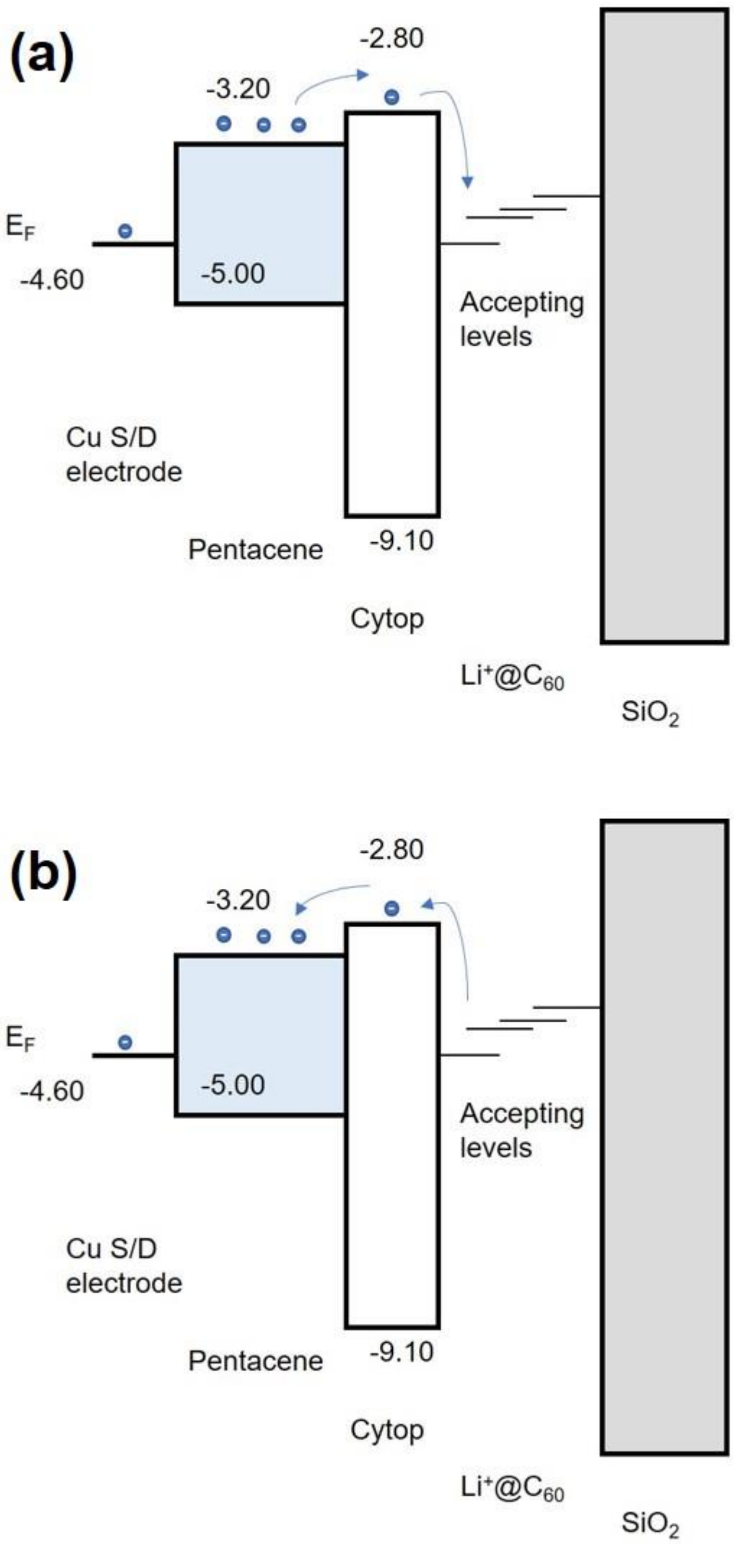

Fig.4.7. Schematic illustration of electron transport through pentacene and Cytop layers, then trapping at Li$^+$@C_{60}. (a) programming and (b) erasing procedures

respectively. The LUMO of the SiO_2 was also reported to be -0.95 eV with the bandgap of 8.0~9.0 eV[2].

When a voltage was applied to the gate, charges were injected from the S/D electrodes. Because of the deep HOMO level of Cytop, holes could not be injected, which was reported in liturature[13,14]. Under a positive electric field, only electrons could be injected, travelled through pentacene, and Cytop layer, then trapped at layer of $Li^+@C_{60}$ (Fig. 4.7. (a)). In our devices, electrons were not trapped at the interface between the Cytop and the SiO_2 layer, because the trapped electrons at the Cytop/SiO_2 interface required higher programming voltage up to 200 V, which described in the section 4.5.1.

The cyclic voltammetric (CV) curve of $Li^+@C_{60}$ [3] showed multi oxidation peaks corresponded to the multi LUMO levels of $Li^+@C_{60}$. We supposed that these multi LUMO levels of $Li^+@C_{60}$ could be the trapping levels of electrons in this layer.

For erasing the memory, a negative voltage was applied. The electrons could not be injected from the gate due to the thick insulator of SiO_2 and holes could not be injected from the S/D electrodes because of deep HOMO level of the Cytop. Thus, we supposed that electrons at $Li^+@C_{60}$ layer would de-trap, then go back to the electrodes (Fig. 4.7. (b)).

The number of trapped electrons in $Li^+@C_{60}$ layer caused the different shift of V_{th}, which corresponds to several ON states in our memories.

4.6. Conclusion

In this chapter, we demonstrated multi-level non-volatile memory transistors using $Li^+@C_{60}$ as a charge trapping layer. The produced OFETs exhibited good performance, with a low V_{th} of -5.98 V and a high μ of 0.84 $cm^2\ V^{-1}\ s^{-1}$. For three programmed states, a voltage of 150 V was applied to the gate for 0.5 s, 5 s, and 50 s, causing approximate shifts of the transfer curve of 10 V, 16 V, and 32 V, respectively. To return to the erased state, a negative voltage of -150 was used for 0.17 s, 1.7 s, and 17 s. A clear difference in the four logic states (one erased state and three programed states) was observed during more than 50,000 seconds. The multi-level effect was found to originate in the electron-trapping ability of the $Li^+@C_{60}$ layer, by comparison with OFETs without a $Li^+@C_{60}$ layer. The basic operation of the memory showed that the memory effect would be attributed to the injection of electrons into the $Li^+@C_{60}$ layer. Further analyzed discussion on the electron trapping mechanism will be shown in the next chapter. Additional research work is being conducted, focused on reduction of operation voltage, increasing the on/off ratio, improving the long-time operation of the devices, and applying for flexible memory devices. We believe that our frontier results will help the evolution of the $Li^+@C_{60}$ research field, and reveal its potential for electric applications.

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CHAPTER 5 || OPERATION MECHANISM OF MLC MEMORY OFETS USING LITHIUM-ION-ENCAPSULATED FULLERENE AS CHARGE TRAPPING LAYER

A memory OFET using Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as the charge trapping layer was fabricated. Under programming voltages of 150 V for 0.5, 5, 50 seconds, the observed memory windows (ΔV_{th}) of 10, 16, 32 V. The shifts of the V_{th} are ascribed to the number of trapped electrons in $Li^+@C_{60}$ molecules, where each molecule could trap up to 6 electrons. By programming for 0.5 and 5 seconds, the average number of trapped electrons per $Li^+@C_{60}$ molecule was 2.40×10^{-2}, 3.84×10^{-2}. Because of the low value of number of trapped electrons, only $Li^+@C_{60}$ molecules at the surface of $Li^+@C_{60}$ domains are supposed to trapped electrons. Beside the memory effect caused by the electron trapping, the $Li^+@C_{60}$ molecules were proposed to migrate into the pentacene layer. This migration causes the change in the I_D of the OFET, which is another origin of the memory effect in our memory device. To confirm the charge trapping in the $Li^+@C_{60}$ molecules by electric field, an ultraviolet-visible spectroscopy (UV-Vis) measurement was carried out to detect an evidence.

5.1. Introduction

In chapter 4, we reported a multi-level organic field effect transistor (OFET) memory using $Li^+@C_{60}$ as the charge trapping layer. The OFETs showed a p-type characteristic with the V_{th} of -5.98 V, the μ of 0.84 $cm^2 V^{-1} s^{-1}$, and the on/off ratio of 2.18×10^5. For programming, a voltage of 150 V was applied to the gate for 0.5 s, 5 s, and 50 s, causing approximate shifts of the transfer curve of 10 V, 16 V, and 32 V, respectively. To return to the erased state, a negative voltage of -150 was used for 0.17 s, 1.7 s, and 17 s. A clear difference in the four logic states (one erased state and three programed states) was observed during more than 50,000 seconds. The multi-level effect was found to originate in the electron-trapping ability of the $Li^+@C_{60}$ layer.

Also in chapter 4, an operation mechanism was discussed. Under programming conditions, electrons are injected from Cu source/drain electrodes, travelled through the pentacene and the Cytop layers and then supposed be trapped at $Li^+@C_{60}$. The trapped electrons would induce the charge carriers in the semiconductor channel, causing the change in the I_D or shift of the V_{th} of the memory OFETs.

This operation mechanism is valid only the electrons can be injected and reach the $Li^+@C_{60}$ layer, which must not be damaged after a fabrication of Cytop layer. Based on an average thickness of the $Li^+@C_{60}$ layer and its density, the density of $Li^+@C_{60}$ molecule per area in the charge trapping layer was estimated. Next, the density of trapped electrons in $Li^+@C_{60}$ layer was calculated based on the shift of the V_{th}. From these results, the average number of trapped electrons per $Li^+@C_{60}$ molecule under different programming conditions would be estimated. Subsequently, a model of electron trapping mechanism was proposed, where electrons would occupy the three-fold degeneration of LUMO states in a single $Li^+@C_{60}$ molecule. In the later part, an UV-Vis measurement was conducted for an evidence of trapped electrons in $Li^+@C_{60}$ molecules.

The memory effect in our memory OFETs might be a migration of $Li^+@C_{60}$ molecules into the pentacene layer, which could be another operation mechanism. In the case of the programming condition of 150 V for 50 seconds, the I_D of the memory OFET at the off-region is so high compared with that of the device under the programming condition of 150 V for 0.5 s. (Fig.5.1) We speculated that the $Li^+@C_{60}$ molecules migrated toward and somehow reach the pentacene layer. At the pentacene

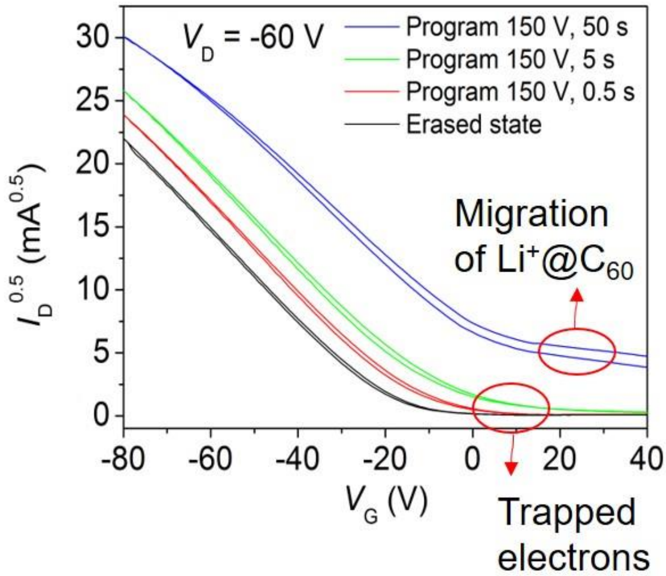

Fig.5.1. Two operation mechanisms which possibly occur in the memory OFETs

interface, the $Li^+@C_{60}$ molecules were ionized, which make the increase of the cation in the pentacene. As the result, the I_D of the memory OFET is high, which causes the memory effect in our devices.

All above discussion of the operation mechanism of the memory OFET would be the main topics, which is presented in the chapter 5 as follows.

5.2. Trapped electrons in a single $Li^+@C_{60}$ molecule

5.2.1. Stability of the $Li^+@C_{60}$ layer during fabrication process.

During the memory OFETs fabrication process, a layer of $Li^+@C_{60}$ was deposited by spin-coating at a speed of 1,000 rpm for 30 seconds using a solution of $Li^+@C_{60}$ bis(trifluoromethylsulfonyl)imide ($Li^+@C_{60}$ NTf_2^-) in monochlorobenzene with a concentration of 2.4 mg/ml, followed by dried at 140 ºC for 30 min. Then, a 10-nm-thick of Cytop was spin-coated at 2,500 rpm for 60 seconds, using a 0.5 wt % Cytop solution, and dried at 100 ºC for 2 h.

In fact, there are several type of $Li^+@C_{60}$ salts such as $[Li^+@C_{60}](SbCl_6^-)$[1,2], $[Li^+@C_{60}]$(TTF-C4P)[1,3,4], $[Li^+@C_{60}](PF_6^-)$[1,5-8], $[Li^+@C_{60}](OTf^-)$[9], and $Li^+@C_{60}$ NTf_2^- [9]. In our study, we used $Li^+@C_{60}$ NTf_2^- due to its higher solubility in monochlorobenzene, which compared with others[9].

Figure 5.2. shows the morphology with cross section profile of $Li^+@C_{60}$ layer on SiO_2 surface before and after spin-coating a layer of Cytop, which carried out by an atomic force microscopy (AFM, Hitachi SPA 400). Before the Cytop layer fabrication, $Li^+@C_{60}$ formed as islands on the surface of SiO_2. After the Cytop deposition, these islands of $Li^+@C_{60}$ have been observed to be stable, which were not damaged. Thus, the proposed operation mechanism, which was presented in chapter 4, is high possible.

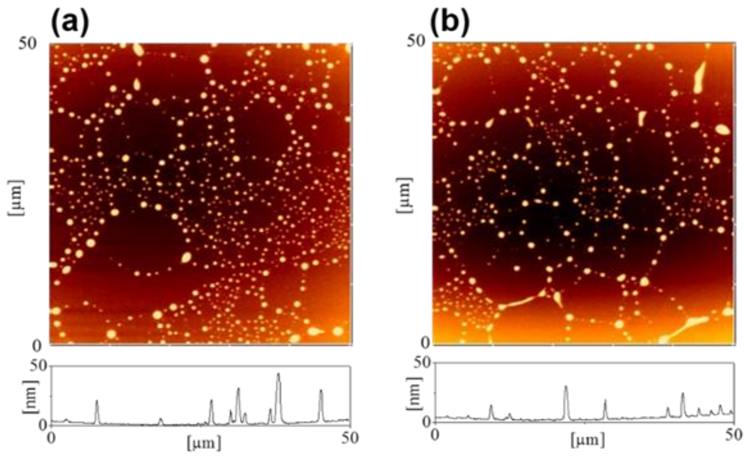

Fig.5.2. Morphology with a cross section profile of $Li^+@C_{60}$ layer on SiO_2 surface (a) before and (b) after spin-coating a layer of Cytop.

5.2.2. Number of trapped electrons per $Li^+@C_{60}$ molecule

Based on an assumption that all $Li^+@C_{60}$ molecules could trap the same number of electrons, the average number of trapped electron per $Li^+@C_{60}$ molecule was estimated by dividing the density of trapped electron (ΔN) by the density of $Li^+@C_{60}$ molecules per area (D_{area}) in the trapping layer. The calculations of ΔN and D_{area} are presented as follows.

Because the $Li^+@C_{60}$ acts as floating-gate in our memory, the ΔN was calculated using an equation[12]:

$$\Delta N = \frac{\varepsilon \cdot \Delta V_{th}}{d \cdot e}$$

where ε, d are the permittivity[11,12] (1.86×10^{-13} F·cm^{-1}) and thickness of the Cytop layer, e is the elementary charge, and the ΔV_{th} is the shift of the V_{th}, caused by a programming voltage.

The result of calculation was presented in the table 5.1. As shown, the density of trapped electrons in the $Li^+@C_{60}$ layer increased with the programming pulse durations.

Table 5.1. Density of trapped electrons at $Li^+@C_{60}$ layer under different programming conditions

Programming conditions	ΔV_{th} (V)	ΔN (cm^{-2})
150 V, 0.5 s	10	2.16×10^{13}
150 V, 5 s	16	3.46×10^{13}

The D_{area} was estimated from the average height of $Li^+@C_{60}$ layer on the SiO_2 surface and the estimated density (D) of $Li^+@C_{60}$ salt. The average height of the $Li^+@C_{60}$ layer was roughly estimated from the morphology of the $Li^+@C_{60}$ surface on the SiO_2. As shown in the Fig. 5.2(a), the $Li^+@C_{60}$ layer does not cover the SiO_2 surface completely. If we consider the lowest signal of the cross-section profile refers to the surface of the SiO_2 layer, the average roughness obtained from the AFM measurement could be used as the average height of the $Li^+@C_{60}$ layer. Based on this assumption, the $Li^+@C_{60}$ layer was estimated to be 8.00 nm. In other hand, the D of $Li^+@C_{60}$ has not reported yet. We estimated this value based on a method provided by Professor Shinobu Aoyagi in Nagoya City University[2], where the calculation method was used for a salt of $Li^+@C_{60}$ $SbCl_6^-$. We assumed the distance between a molecule to others in the crystal structure of $Li^+@C_{60}$ NTf_2^- salt is equal than that of $Li^+@C_{60}$ $SbCl_6^-$ salt. So that, a cubic of $Li^+@C_{60}$ NTf_2^- included 4 molecules has a volume of 3,554.60 Å^3. The molecule weight of $Li^+@C_{60}$ NTf_2^- is 1,007.68 g·mol^{-1}. As the result, the D of $Li^+@C_{60}$ salt which used in our experiment, was estimated to be 1.88 g·cm^{-3}. Subsequently, the D_{area} of $Li^+@C_{60}$ layer could be calculated to be 9.00×10^{14} cm^{-2}.

As mentioned above, we assumed that all $Li^+@C_{60}$ molecules could trap electrons. Thus, the average numbers of trapped electron were estimated to be 2.40×10^{-2} and 3.84×10^{-2} under a programming conditions of 150 V for 0.5 and 5, respectively. These low values of trapped electrons would be due to the assumption based on that all $Li^+@C_{60}$ molecules in trapping layer equally contribute to trap electrons. It seems to be that electron trapping occurs only at $Li^+@C_{60}$ molecules at the surface of $Li^+@C_{60}$ domains, where each $Li^+@C_{60}$ molecule could trap one, two, three or more electrons.

5.2.3. Model of trapped electrons in a single $Li^+@C_{60}$ molecule.

The $Li^+@C_{60}$ molecules at the surface of $Li^+@C_{60}$ domains were supposed to trap electrons. Beside of this, it was reported that each $Li^+@C_{60}$ molecule could trap

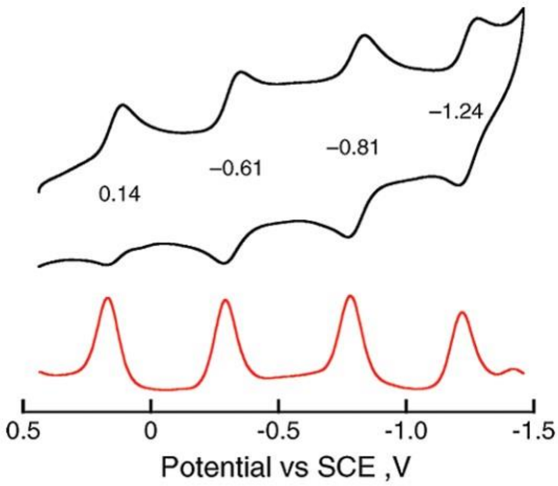

Fig.5.3. Cyclic voltammogram of $Li^+@C_{60}$ PF_6 (10^{-4} M) recorded in PhCN containing 0.1 M $TBAPF_6$.[3]

up to 6 electrons[2,3]. In this part, the trapping level energy of electron in $Li^+@C_{60}$ molecule was analyzed.

In order to analysis the trapping levels of the electrons in the $Li^+@C_{60}$ molecules, we discussed based on the cyclic voltammetry of the $Li^+@C_{60}$ PF_6, another $Li^+@C_{60}$ salt. Figure 5.3 shows the CV curve of $Li^+@C_{60}$ salt using the solution of the $Li^+@C_{60}$ PF_6 (10^{-4} M) in benzonitrile (PhCN) containing an electrolyte of tetrabutylammonium hexafluorophosphate ($TBAF_6$) (0.1 M), referred from Professor Fukuzumi[3]. From the CV curve, the trapping levels of $Li^+@C_{60}$ PF_6 was calculated to be -4.54, -3.79, -3.59 and -3.16 eV, respectively using the equation[14]

$$\mathrm{LUMO} = -\mathrm{e}[E_{red} + 4.4]$$

where E_{red} is the reduction potential referring to SCE electrode.

Based on these results, the possible trapping mechanism of electrons into the $Li^+@C_{60}$ molecule was shown in the Fig. 5.4. When the programming voltage was applied, the electrons were injected from the S/D electrodes, travelling through the pentacene and Cytop layer and trapped at the $Li^+@C_{60}$ molecules at the surface of the

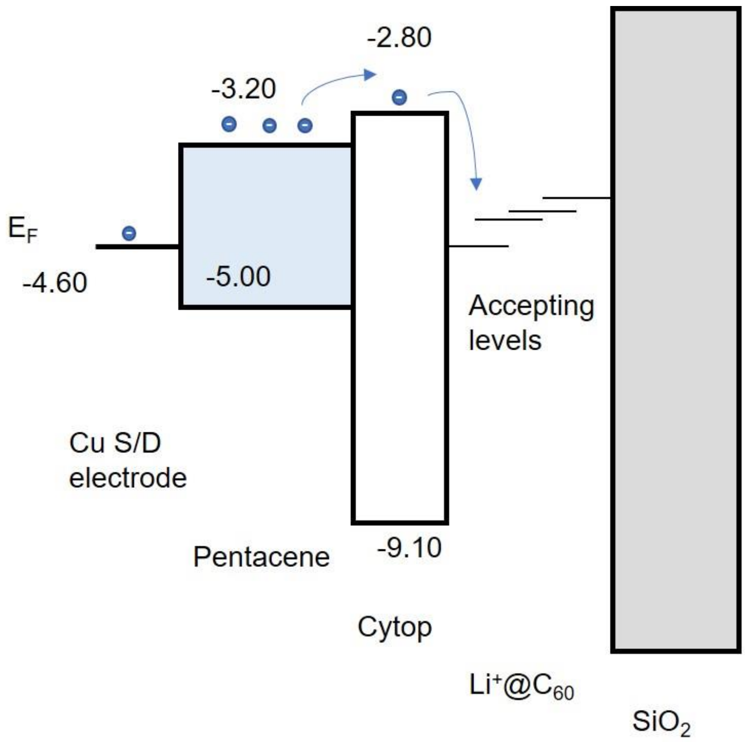

Fig.5.4. Trapping mechanism of electrons in the floating gate of $Li^+@C_{60}$

floating gate. Each $Li^+@C_{60}$ molecule could trap electrons at the trapping levels (or accepting levels) of -4.54, -3.79, -3.59 and -3.16 eV. When the programming duration increased, the number of active $Li^+@C_{60}$ molecules would increase, resulting in the increase of the trapped electron in the floating gate, causing the multi-level effect in the device. When a reversed voltage was applied, the trapped electrons would de-trap since the high insulator of the SiO_2.

The different numbers of trapped electrons in the $Li^+@C_{60}$ molecule and generally in $Li^+@C_{60}$ layer were controlled by the programming voltage durations. It would induce the I_D in the channel of the memory OFET, which corresponded to the multi-level memory effect in our devices.

5.3. Evidence of electron trapping in the $Li^+@C_{60}$ layer

In the previous section, we supposed that the multi-level memory effect originated from the trapped electrons in $Li^+@C_{60}$ layer. The trapped electrons in $Li^+@C_{60}$ molecules could be excited into the higher energy level when they receive high enough photon energy. Therefore, the trapping operation of electron into $Li^+@C_{60}$ molecule is valid only if new peaks could be observed in the absorption spectra of $Li^+@C_{60}$ under different bias voltage.

Due to this, we fabricated a capacitor with a layer of $Li^+@C_{60}$ for an ultra-violet visible spectroscopy (UV-Vis) measurement.

Experimental

A capacitor with a structure of glass/ITO (150 nm)/active layer (320 nm)/Al (100nm) was prepared. A sample without a layer of active layer was also fabricated for the reference sample.

The active layer was fabricated by spin-coating a solution of poly (vinyl cinnamate) (PVCN) and $Li^+@C_{60}$ NTf_2^- with a ratio of 8:1 in monochlorobenzene (concentration of 45 mg of mixture per 1 ml). After spin-coating, the sample was put under UV exposure for 20 min, followed by dried at 140 ºC for 1h. The material of PVCN plays a role of an insulator in the capacitor.

The UV-Vis measurement was carried out in room temperature before and after an application of a bias voltage between two electrodes of the capacitor.

For comparison, a capacitor with an active layer using PVCN was fabricated.

Results and discussion

Figure 5.5 shows the UV-Vis spectrum of the $Li^+@C_{60}$ NTf_2^- salt in PVCN before and after a voltage application between two electrodes for 10 seconds. In the spectrum, the unstable of signals at the wavelength between 760 nm to 900 nm could be the noise during measurement, which caused by the measurement system.

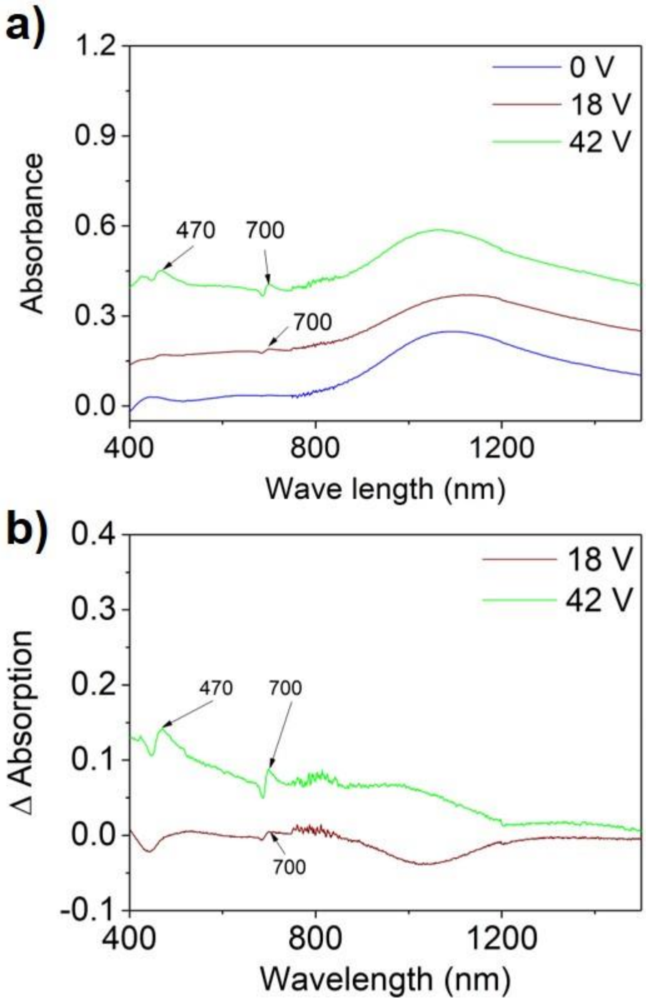

Fig.5.5 (a) UV-Vis spectrum and (b) spectrum subtraction of PVCN:Li^+@C_{60} salt after and before applying a voltage for 10 seconds.

As shown in Fig. 5.5 (a), a shift of a tumor at a wavelength of between 1,000 and 1,200 nm could be due to an interference effect. When a voltage was applied between electrodes of the capacitor, a small current travelled through an active layer of PVCN:Li^+@C_{60}. The heat was caused by this current, would have an effect on the thickness of the active layer, which corresponds to the interference[16-18].

In Fig. 5.5 (b), the peaks at wavelength of 425, 470 and 700 nm appear after a bias voltage was applied. The amplitude of these peaks increased proportionally with the amplitude of applied voltages. On the other hand, we found a similarity between the spectra of the Li^+@C_{60} in thin film and those in the solution under the application of the voltage, especially in the $3e^-$ curve. (Fig. 5.6). It could be an evidence for the electron trapping at the Li^+@C_{60} molecules by applied voltage.

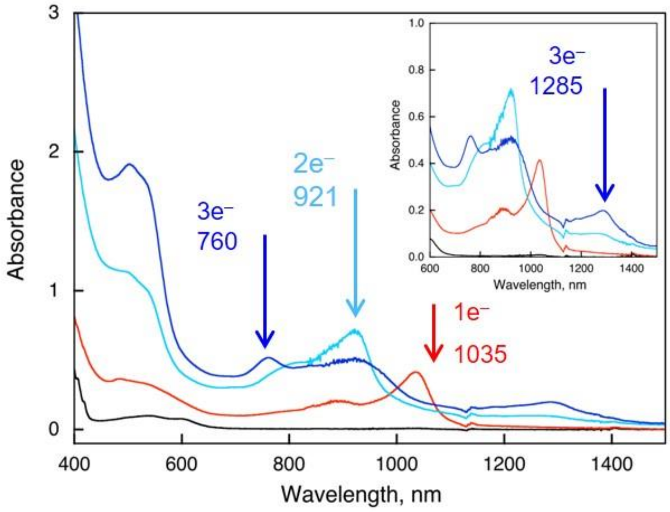

Fig.5.6 UV-Vis spectrum of $Li^{+}@C_{60}$ PF_6 in solution, provided by Prof. OhKubo, Osaka University

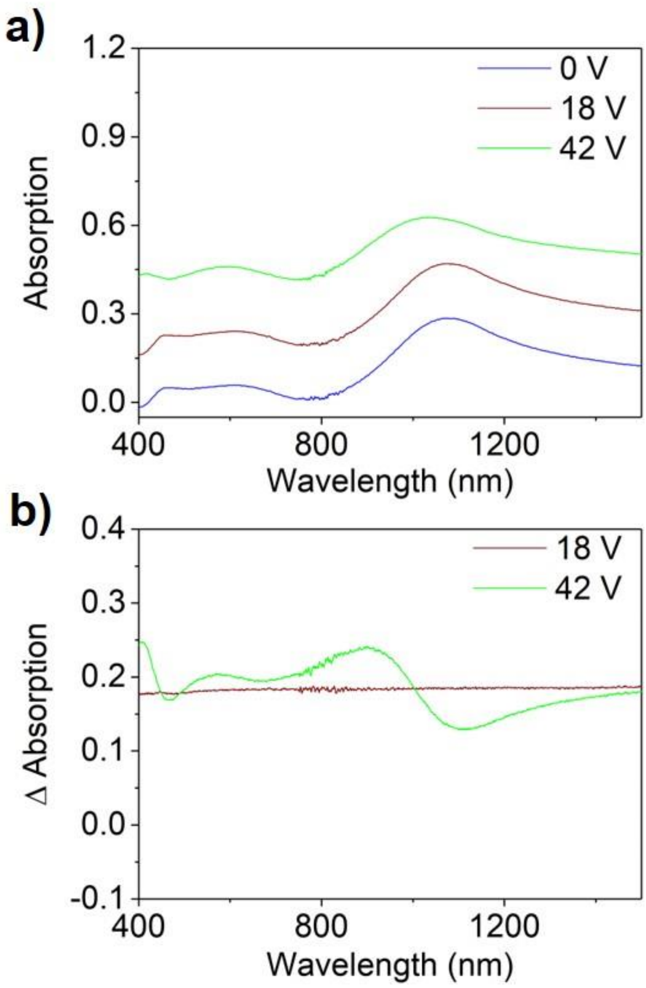

Fig.5.7. (a) UV-Vis spectrum and (b) spectrum subtraction of PVCN after and before applying a voltage for 10 seconds.

To clarify the trapping site at the $Li^+@C_{60}$ molecules which caused under applied voltage, another capacitor using PVCN as an active layer was fabricated and the UV-Vis measurement was carried out for comparison. Fig. 5.7 shows the UV-Vis spectrum of PVCN after and before applying the bias voltages between electrodes. As shown in the spectrum (Fig. 5.7 (a)) and spectrum subtraction (Fig.5.7 (b)), there is no change in UV-Vis spectra before and after applying a voltage of 18 V. Under higher applied voltages, the spectra changed. However, no clear peaks were observed and no new peaks were appeared. It is clear that at least, the peaks with a wavelength of 470 and 700 nm in the spectra of $Li^+@C_{60}$ and PVCN capacitor are originated from an interaction between $Li^+@C_{60}$ molecules and the trapped electrons.

Although the electron trapping mechanism has not been clear, this UV-Vis result above could be an evidence for the electrons which are trapped at $Li^+@C_{60}$ molecules under an application of a voltage.

5.4. Migration of $Li^+@C_{60}$ molecule into the pentacene layer

As discussed in the section 5.1, the memory effect in our OFETs could be occurred by the migration of the $Li^+@C_{60}$ molecules in to the pentacene layer. Under programming condition, the $Li^+@C_{60}$ molecules not only trap electrons, which induced the I_D of the OFETs, but also migrate into the pentacene layer somehow. Some $Li^+@C_{60}$ molecules might reach the pentacene layer and then ionize the pentacene molecules by catching the electrons of the pentacene structure. As the result,

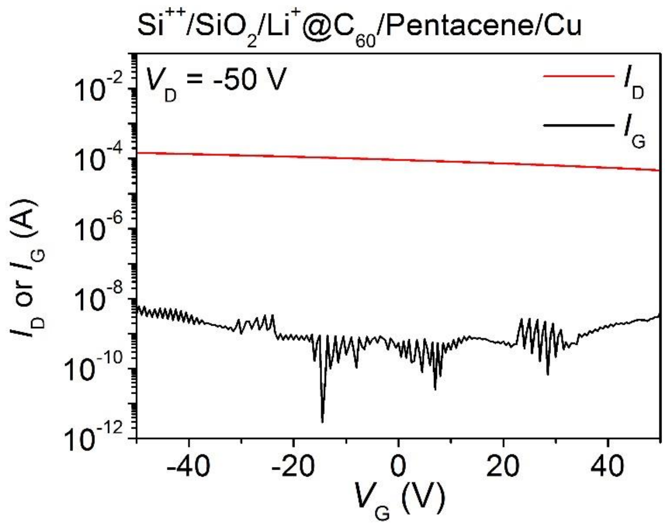

Fig.5.8. Transfer characteristics of the OFETs without CYTOP layer

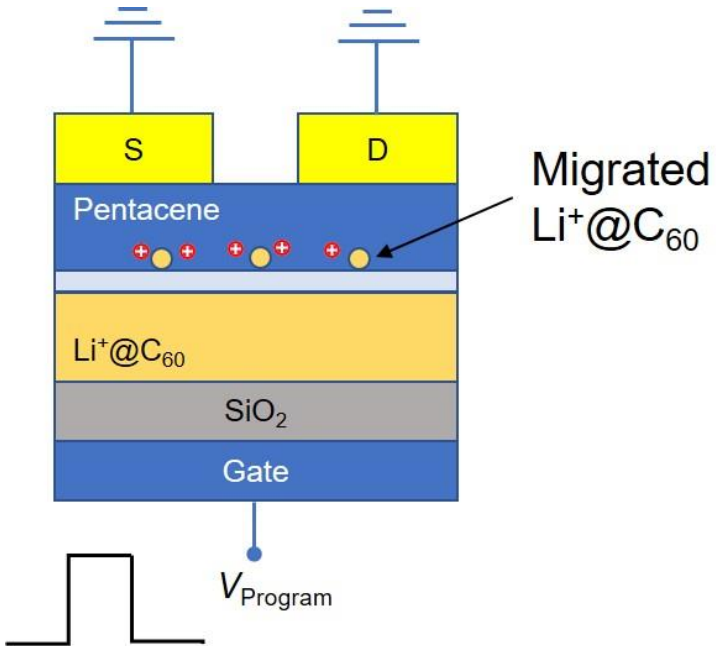

Fig.5.9. Migration of the $Li^+@C_{60}$ molecules into the pentacene layer

the cations in the pentacene layer increase, which caused the increase of the I_D if the memory OFETs. To confirm this assumption, we fabricated the OFET without the thin insulator of Cytop. As shown in the Fig. 5.8, the I_D of the OFET always is high, not depends on the applied voltage to the gate. It clearly indicated that the $Li^+@C_{60}$ molecules may ionized the pentacene molecules, which corresponds to the increase of the charge carrier in the channel of the OFET. Based on this result, we proposed that the migration of the $Li^+@C_{60}$ molecules into the pentacene layer could be one of the origins of the memory effect in our devices. (Fig. 5.9)

5.5. Conclusion

In this chapter, a deep discussion on the electron trapping mechanism was conducted. In the memory OFET using Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$) as charge trapping layer, the ΔV_{th} of 10, 16, 32 V was observed under a programming condition of 150 V for 0.5, 5 and 50 seconds. The shifts of V_{th} are ascribed to the number of trapped electrons in $Li^+@C_{60}$ molecules, where each molecule could trap up to 6 electrons. By programming for 0.5 and 5 seconds, the average number of trapped electrons per $Li^+@C_{60}$ molecule was 2.40×10^{-2}, 3.84×10^{-2}. Because of the low value of number of trapped electrons, only $Li^+@C_{60}$ molecules at the surface of $Li^+@C_{60}$ domains are supposed to trapped electrons. To confirm the charge trapping in the $Li^+@C_{60}$ molecules by electric field, an UV-Vis measurement was carried out to detect an evidence. Beside the memory effect caused by the electron trapping, the $Li^+@C_{60}$ molecules were proposed to migrate into the pentacene layer. This migration causes the change in the I_D of the OFET, which is another origin of the memory effect in our memory device.

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CHAPTER 6 || CONCLUSION AND FUTURE WORK

6.1. Conclusions

Based on the understanding of an organic field effect transistor (OFET) including the material, design structure, the operation mechanism, fabrication process and characterization, studies on OFET's performance and its applications for MLC memories have been carried out. This result of research indicated that a background pressure plays the role on the increase of the OFET mobility. This simple technique was applied to fabricated the MLC memory OFET in this dissertation. Then, a charge trapping write-once-read-many MLC memory OFET using poly (vinyl cinnamate) was fabricated, followed by a multi-level memory OFET using Lithium-ion-encapsulated fullerene ($Li^+@C_{60}$). These memories exhibited several ON states which could store much more data in a simple structure of a transistor.

The dissertation was summarized at each chapter as follows:

Chapter 1

The general introduction of organic memories was reviewed, which started from a single bit memory, and then a MLC memory. Based on this, some current issues were discussed and lead us to focus on the MLC memory based on a structure of an OFET, which operated on charge trapping mechanism

Chapter 2

Before a fabrication of a memory OFET, the performance of the OFET should be enhanced. A simple technique was found and applied that high background pressure during copper source/drain electrodes could improve the mobility (μ) as well as reduce the threshold voltage (V_{th}) of the OFETs. By deposited under the background pressure of 2.5×10^{-5} Torr, the μ of the OFETs is c.a. 2 times and 3 times c.a. greater than that of the OFETs with gold and copper electrodes fabricated under low pressure of 1.6×10^{-6} Torr, respectively. The increase of the μ was due to the reduction of contact resistance, which caused by a penetration of oxygen into the active layer of pentacene during the fabrication process. We believe this result would be helpful for improving OFETs performance using a simple method which could be applied in industrial applications.

Chapter 3

In the chapter 3, we reported a write-once-read-many memory OFET using poly (vinyl cinnamate) as the charge trapping layer. The OFET showed a p-type characteristic with the μ of 0.29 $cm^2\,V^{-1}\,s^{-1}$, the V_{th} of -11.54 V and the on/off ratio of 2.53×10^5. Under a programming voltage of -160, -180 and -200 V for 3 seconds, the ΔV_{th} of 9, 17 and 27 V were observed. Each logic states, which was represented by the I_D, are stable for a long retention time up to 10^4 s. This memory effect is caused by the trapped holes at the PVCN/SiO_2 interface. For the understanding of the operation mechanism, the HOMO and LUMO level of PVCN was estimated from the UV-Vis and UPS spectrum. Subsequently, the operation of the memory was proposed. However, the understanding of hole trap mechanism is still limited. Beyond that, we believe that this study could be helpful for a development of a write-once-read-many MLC non-volatile memory OFET with a reasonable cost.

Chapter 4

The write-once-read-many memory has a limited range of applications due to the erasable storage of data. Thus, a MLC memory OFET has been the main target of our research. To solve this issue, a layer of $Li^+@C_{60}$ was used as charge trapping layer. The memory OFETs exhibited p-type characteristics, with the V_{th} of -5.98 V and the μ of 0.84 $cm^2\,V^{-1}\,s^{-1}$. For three programmed states, a voltage of 150 V was applied to the gate for 0.5 s, 5 s, and 50 s, causing approximate shifts of the transfer curve of 10 V, 16 V, and 32 V, respectively. To return to the erased state, a negative voltage of -150 was used for 0.17 s, 1.7 s, and 17 s. A clear difference in the four logic states (one erased state and three programed states) was observed during more than 50,000 seconds.

The multi-level effect was found to originate in the electron-trapping ability of the $Li^+@C_{60}$ layer, by comparison with OFETs without a $Li^+@C_{60}$ layer. The basic operation of the memory showed that the memory effect would be attributed to the injection of electrons into the $Li^+@C_{60}$ layer.

Chapter 5

In the last chapter, further discussion on the electron trapping mechanism of the multi-lever memory OFETs using $Li^+@C_{60}$ as the charge trapping layer was discussed. Under a programming condition, electrons were injected from the source/drain electrodes of the OFET, travelled through pentacene layer and trapped. Average numbers of trapped electron in each $Li^+@C_{60}$ were estimated to be 2.40×10^{-2} and 3.84×10^{-2} under programming conditions of 150 V for 0.5 and 5 seconds. Low values of numbers of trapped electrons per $Li^+@C_{60}$ molecule indicated that only $Li^+@C_{60}$ molecules at the surface of $Li^+@C_{60}$ domains are supposed to trapped electrons, which occupied at level energies of -4.54, -3.79, -3.59 and -3.16 eV. In addition, an UV-Vis measurement was conducted for an evidence of trapped electrons in $Li^+@C_{60}$ molecules. Another mechanism of the memory operation in our OFETs could be the migration of the $Li^+@C_{60}$ molecules into the pentacene layer where the pentacene molecules could be ionized and correspond to the increase of the I_D in the OFETs.

6.2. Future work

In this dissertation, a write-once-read-many MLC memory OFET using PVCN and a multi-level memory OFET using $Li^+@C_{60}$ for the charge trapping layer were fabricated. However, there are still some questions that have not been answered yet, which could be our future work.

At first, an operation voltage was high in our devices, which compared to other works. It was caused by a thick dielectric layer of SiO_2 that we used. Because of this reason, we fabricated a memory OFET with a charge trapping of $Li^+@C_{60}$ material using a 100 nm-thick of SiO_2 as dielectric layer. However, this OFET showed a low performance with a μ of 0.02 $cm^2\ V^{-1}\ s^{-1}$, a V_{th} of -0.6 V and an on/off ratio of 2.5×10^3(Fig.6.1. (a) and (b)). When this OFET was applied in the memory application, a

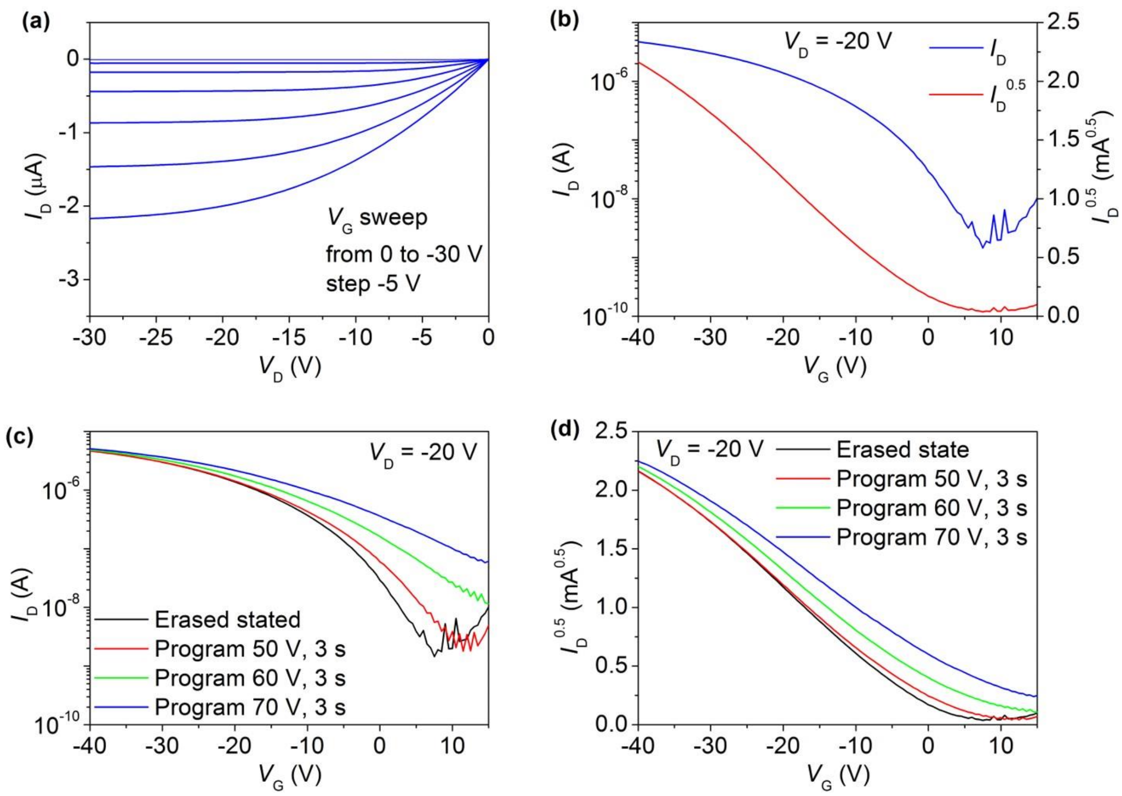

Fig.6.1. (a) output, (b) transfer curves of the memory OFET with 100 nm-thick of SiO_2. (c)(d) the shift of transfer curves under programming by a voltage of 50, 60 and 70 V for 3 seconds.

ΔV_{th} of 1.3, 5.0 and 14.6 V was observed under applied voltages of 50, 60 and 70 V for 3 seconds to the gate. The memory could be erased by a reversed voltage of -45, -

50 and -55 V for 3 seconds, respectively (Fig.6.1. (c) and (d)). However, this memory OFET operated for only few cycles of program-read-erase-read. A reduction of operation voltage of this device as well as the memory OFET using PVCN would be one of short-term works for us.

Secondly, in the case of memory OFET using PVCN as charge trapping layer, holes are injected and trapped. The trapping phenomena seems to be suitable for n-type OFET. Thus, fabrication and characterization of a n-type memory OFET using PVCN could be other reseacrch topic.

Thirdly, in the case of memory OFET using $Li^+@C_{60}$ as charge trapping layer, the electrons were not trapped at the interface between SiO_2 and a layer of polymer. Thus, it is high possible that we could fabricate a flexible memory using flexible substrate such as a plastic substrate.

Lastly, the operation of the memory OFET could be explain using a diagram of level energy. In this diagram, charge could be injected in to the charge trapping layer. But a question is that how the charge trap at there or what the connection between charges and molecules in this layer is. Up to this moment, no clear answer has been found yet. It would be a long-term plan of my work.

LIST OF PUBLICATIONS

Journal

1. **Cuong Manh Tran**, Heisuke Sakai, Yuki Kawashima, Kei Ohkubo, Shunichi Fukuzumi, Hideyuki Murata, "Multi-level non-volatile organic transistor-based memory using Lithium-ion-encapsulated fullerene as a charge trapping layer", Org. Electron. **45**, 234-239 (2017)
2. **Cuong Manh Tran**, Heisuke Sakai, Tatsuya Murakami, Hideyuki Murata, "Effect of background pressure on the performance of organic field effect transistors with copper electrodes", IEICE Trans. Electron. **E100-C**, 122-125 (2017)

International conferences

1. <u>Cuong Manh Tran</u>, Heisuke Sakai, Yuki Kawashima, Kei Ohkubo, Shunichi Fukuzumi, Hideyuki Murata, "Operation mechanism of a multi-level organic field effect transistor memory using $Li^+@C_{60}$ as a charge trapping layer", 9th International Conference on Molecular Electronics and Bioelectronics, Kanazawa, Japan, June 26-28th, 2017.
2. <u>Cuong Manh Tran</u>, Heisuke Sakai, Tatsuya Murakami, Hideyuki Murata, "Write-once-read-many multi-bit memory organic field effect transistor using poly (vinyl cinnamate) as charge trapping layer", 12th International Conference on Nano-Molecular Electronics, Kobe, Japan, Dec 14-16th, 2016.
3. <u>Cuong Manh Tran</u>, Heisuke Sakai, Yuki Kawashima, Kei Ohkubo, Shunichi Fukuzumi, Hideyuki Murata, "Multi-bit non-volatile organic transistor-based memory using Lithium-ion-encapsulated fullerene as a charge trapping layer", 230th Pacific RIM Meeting on Electrochemical and Solid-state Science, Honolulu, Hawaii, Oct 2-7th 2016.
4. <u>Cuong Manh Tran</u>, Heisuke Sakai, Tatsuya Murakami, Hideyuki Murata, "Effect of background pressure on the performance of organic field effect transistors with copper electrodes", 9th International Symposium on Organic Molecular Electronics, Niigata, Japan, May 18-20th 2016.
5. <u>Cuong Manh Tran</u>, Heisuke Sakai, Tatsuya Murakami, Hideyuki Murata, "High performance organic field effect transistor with copper as source/drain

electrodes", IISc-JAIST Workshop on Functional Inorganic and Organic Materials, JAIST, Ishikawa, March 07th 2016.

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6. Cuong Manh Tran, Heisuke Sakai, Tatsuya Murakami, Hideyuki Murata, "Multi-bit memory effect in an organic transistor using a charge trapping polymer", The 64th Spring Meeting of Japan Society of Applied Physics 2017, Yokohama, Japan, Mar 14-17th 2017.
7. Cuong Manh Tran, Heisuke Sakai, Yuki Kawashima, Kei Ohkubo, Shunichi Fukuzumi, Hideyuki Murata, "A new type of multilevel organic field effect transistors using lithium-ion-encapsulated fullerene", The 63rd Spring Meeting of Japan Society of Applied Physics 2016, Tokyo, Japan, Mar 19-22nd 2016.
8. Cuong Manh Tran, Heisuke Sakai, Tatsuya Murakami, Hideyuki Murata,"The increase of organic field effect transistor mobility by copper electrodes deposition at high background pressure", The 76th Autumn Meeting of Japan Society of Applied Physics 2015, Nagoya, Japan, Sep 13-16th 2015.