Doctoral Dissertation

Study of the Physical Properties of Graphene Nano-Ribbon Band-to-Band Tunnel Transistor

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DECLARATION

I, Ahmed Mohammed Mohammed Hammam, declare that this thesis is the result of my own work and includes nothing, which is the outcome of work done in collaboration except - where specifically indicated in the text. It has not been previously submitted, in part or whole, to any University of the institution for any degree, diploma, or other qualification.

Signed:_____

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Ahmed Mohammed Mohammed Hammam

ABSTRACT

Study of the Physical Properties

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Tunnel field effect transistors (TFET) have attracted much interest due to their low OFF state current (I_{OFF}) and the possibility of reaching a subthreshold swing (SS) below the limit (60 mV/decade) of standard CMOS technology. However, all experimentally realized TFETs based on conventional semiconductors exhibit low ON-state current (I_{ON}), which limits their usefulness in integrated circuits (ICs). Due to the atomically thin nature, width tuneable bandgap, and low effective mass, graphene nanoribbons (GNR) are seen as one of the most promising materials to overcome this limitation. Theoretical reports on graphene-based TFETs underline this potential. However, to the best of our knowledge, GNR-TFET operation has not been realized experimentally, yet. The strict requirements for the width (which is used to control the energy gap) and the electrostatic doping with high spatial resolution make such devices very challenging in reality. By developing a thin-film based fabrication process using direct electron-beam lithography (EBL), GNR-TFET operation is demonstrated successfully in this work for the first time. SS slopes as low as ~42 mV/decade are obtained from devices operating at 5 K. The I_{ON} current density is ~6.1 μA/μm.

Chemical vapor deposited (CVD) graphene is patterned into narrow ribbons by using hydrogen silsesquioxane (HSQ) resist. As the GNR width of has a direct effect on the energy gap, accurate control in the sub-20-nm regime is required. Several optimizations are described in detail, and 15 nm wide ribbons with an energy gap of ~70 meV are achieved. In addition, three top gates with gap separation of down to 30 nm are deposited above the GNR with high alignment accuracy, enabling the sharp *p-i-n* doping profile along the channel. Devices with two and three top gates are discussed, and how the individual channel gating affects the device operation. Extracted SS slopes are independent of temperature below 40 K.

Keywords: CVD Graphene, Graphene Nano-Ribbon (GNR), Tunnel field effect transistor (TFET), Electrostatic doping, GNR *pn* junction, Subthreshold Slop (SS).

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1 Introduction

1.1 Moore`s law and CMOS Limitations

Complementary metal oxide semiconductor (CMOS) devices have continuously been downscaled for decades following Moore's law[1]. According to Moore's law, the number of transistor per processor chip double every 18-24 month, while gate length halves every 3-4 years (see Figure 1.1). The performance of Very Large Scale Integration (VLSI) circuits has been gradually improved by scaling down device dimensions. However, the standby power governed by the leakage current at their OFF state is now exceeding the dynamic power at the ON state[2]. One possible way to decrease the leakage current is decreasing the drain voltage (V_d). However, to reduce the V_d the threshold voltage (V_{th}) needs to be reduced as well to keep the same circuit performance and gate overdrive. Unfortunately, the this not possible for the following reason: the V_{th} cannot be scaled down without scaling the subthreshold swing (SS) as well,

$$I_{off} = I_{th} \exp\left(-\frac{2.3V_{th}}{SS}\right) \quad (1)$$

Where I_{th} is the threshold current, I_{off} is the leakage current. from Eq(1), it is obvious that to maintain the same leakage current V_{th} cannot be reduced while keeping SS fixed. Since the SS limit for MOSFET is 60 mV/dec, the V_{th} and V_d cannot be scaled down. Therefore, scaling the device dimension down without scaling the V_d will increase the leakage current (standby power), see Figure 1.2. Therefore, there is an urgent need for alternatives that can overcome or complement with the traditional CMOS technology.

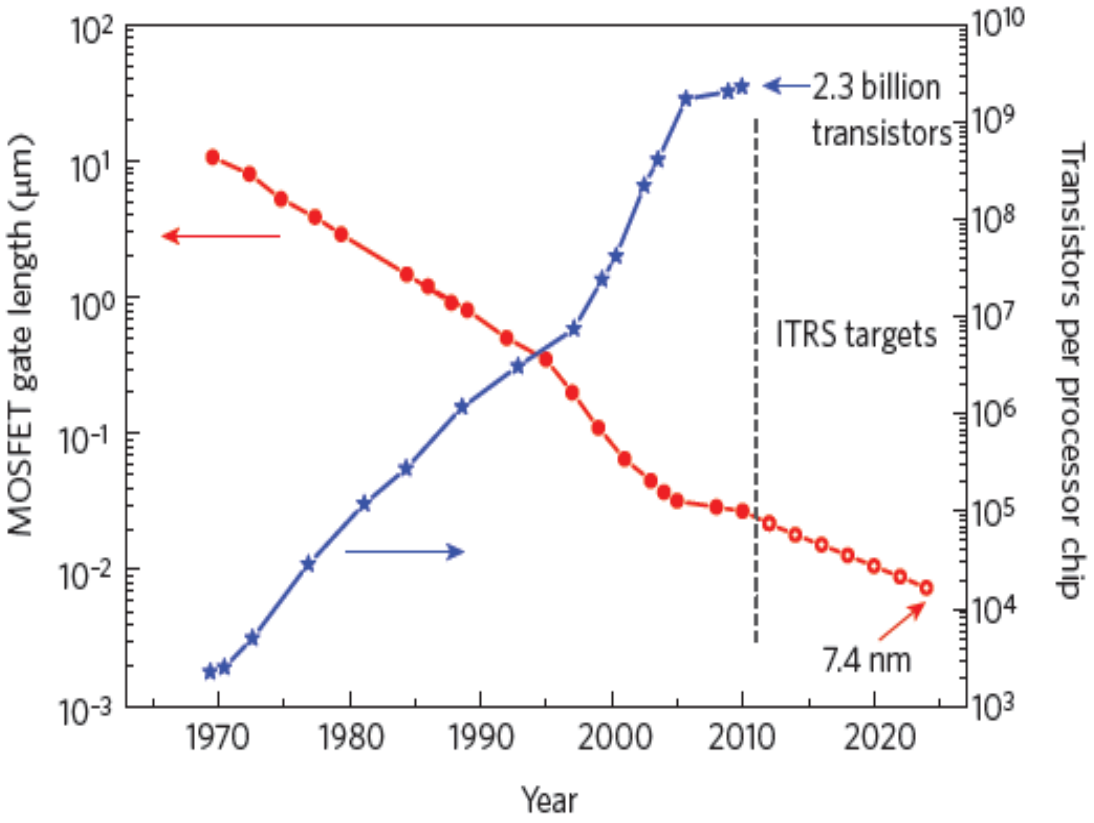


Figure 1.1- Scaling of transistor gate length and number of transistor per processor chip vs. year

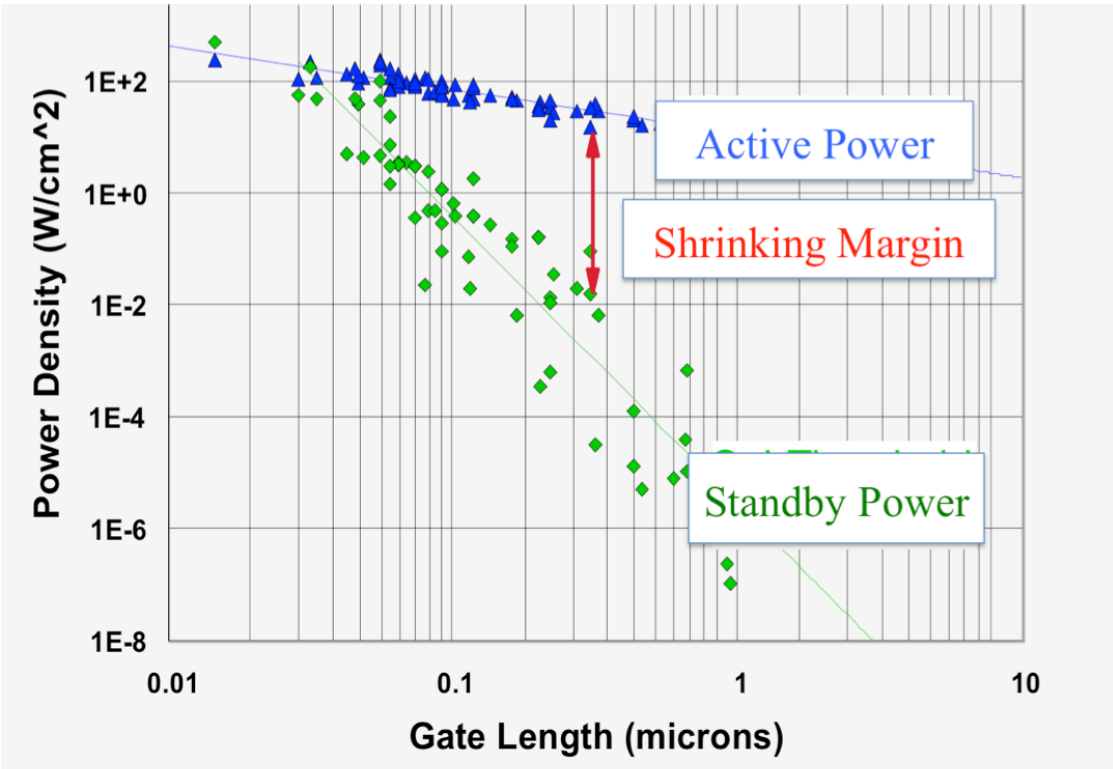


Figure 1.2.The trend of Power consumption with CMOS scaling. Reproduced from (without permission)[3]

There are many devices proposed to tackle this problem, for instance, the FinFET ([4], the semiconductor nanowire FET [5], and carbon nanotubes based FETs [6] and Graphene[7]. However, these devices are based on the same physics of conventional FET, where the limiting factor is (kT/q). In order to overcome this issue, various types of abrupt switches are currently examined, which are anticipated to realize a subthreshold slope (SS) smaller than the theoretical limit of 60 mV/decade at room temperature for Metal-oxide-semiconductor field effect transistors (MOSFET) and a lower threshold voltage, leading to a remarkable reduction of the leakage floor [8]. In the next section, the status and the main challenge facing the TFET will be discussed.

1.2 Tunnel Field Effect Transistor(TFET): State of the Art

1.2.1 Operation Mechanism

The TFET structure is similar to the MOSFET structure. In the TFET, drain and source are of opposite doping types. The device structure and band profile in the OFF state are drawn in Figure 1.3a and b, respectively. In the OFF state, the built-in potentials of the p-i and n-i junctions result in a staircase-like band-profile. When a small V_{DS} is applied to the equilibrium state, electron and holes currents are blocked by the built-in potential barriers. Now in the n-TFET, if a positive gate bias is applied, the bands in the channel move down. For positive V_{DS}, charge carriers can tunnel through the bandgap at the source/channel junction as soon as the minimum of the conduction band in the channel became lower than the valence band in the source. This operating mode is the N-channel ON state of the TFET. In a similar manner, in the p-TFET operation mode can be attained by applying a negative V_{GS} and negative V_{DS}. In this case, the energy band in the channel move up, and tunneling takes place at the source-channel junction as illustrated in Figure 1.3b.

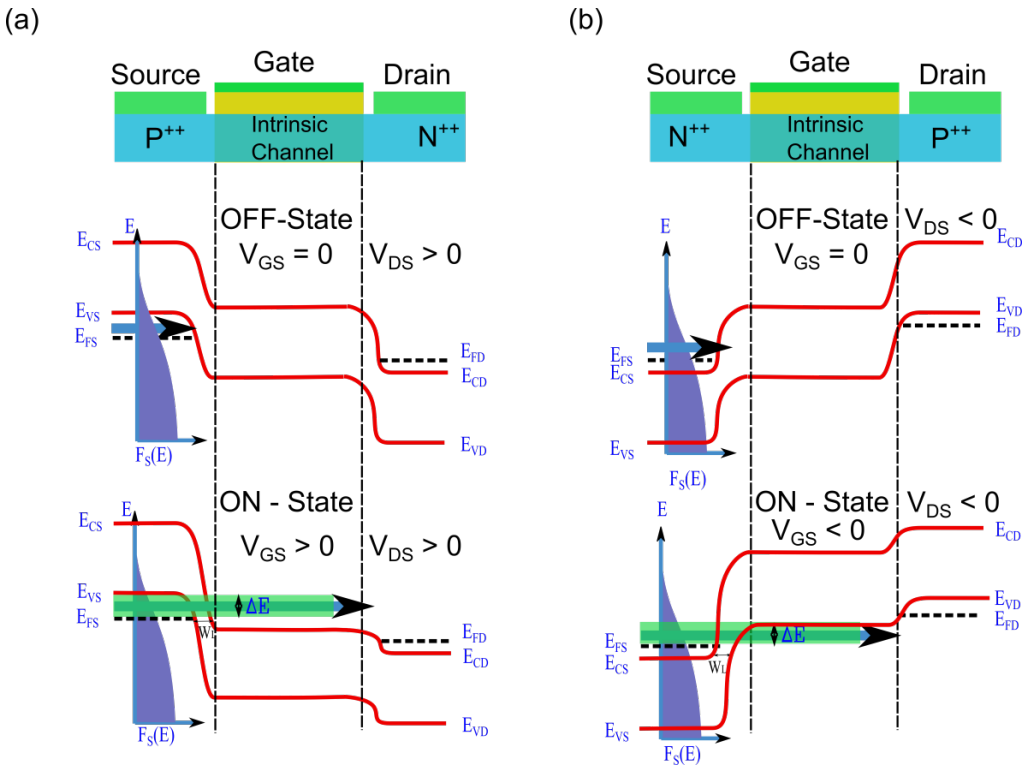


Figure 1.3. (a) The device structure of n-TFET and the corresponding energy band diagram in the OFF and ON state. (b) The device structure of p-TFET and the corresponding energy band diagram in the OFF and ON state. FS(E) is the Fermi-Dirac distribution of electrons in the source region. WL is the minimum tunnel width, EFS/D is the source-drain Fermi level, and ΔE is the allowed tunnel window.

It is worth to mention here that, in contrast to the MOSFET, the Fermi-Dirac tail is completely truncated (filtered) by the energy band. Only energy allowed window (ΔE) can tunnel through the barrier. This is the reason why the TFET does not depend on the temperature (Fermi-Dirac distribution) and works as a high band and low band filters.Therefore, it possible to achieve an SS of below 60 mV per decade[9].

1.2.2 State of the Art

Recently, TFET attracted great attention due to its capability of achieving sub-thermal limit SS and lower off state current. The first experimental TFET achieved by Appenzeller et al. in 2004[10]. Figure 1.4 summarizes the achievements of different TFET types according to the SS and I_{on}/I_{off} ratio. Summary of the best achievements is shown in the table in the figure. As shown in Figure 1.4, Ge/sSi[11] and SiNW[12] achieved sub-60 mV/dec SS and got high Ion/Ioff ratio ranging from 10^5 to more than 10^7, respectively. However, the general trends of Group IV materials [13],[14]and Ge[14]–[16] demonstrate small ON-state currents rising from the indirect energy gaps and lower tunneling probability. In contrast to Group IV, Group III-V materials like InGaAs [17], InAs [18],[19], and InSb [20] have higher ON-state currents attributable to

their narrower and direct energy gaps. In 2012, Tomioka et al. fabricated III-V nanowire (NW)/Si heterojunctions TFET and achieved SS of 21mV/dec. With I_{ON}/I_{OFF} ratio ~ 10^6 and I_{ON} current ~ 1μA/μm [21]. The broken-gap and staggered hetero-junctions, for instance, InAs/GaSb [22] and AlGaSb/InAs [23], enhances I_{ON} by shrinking the tunneling distances. In addition, utilizing of resonant tunneling into TFETs sharpen the tunneling window and consequently reduces the SS down to ~ 25 mV/dec [22],[24]. In 2014 Kim et al.[11] achieved SS of 28 meV/dec with I_{on}/I_{off} ratio over 10^7. However, the ON current is still below 0.1 μA/μm.

	MOSFET	InGaAs TFET	InAs TFET	Ge/Si TFET	SiNW TFET
On-state current (μA/μm)	~1,000	10	~1	< 0.1	1.2

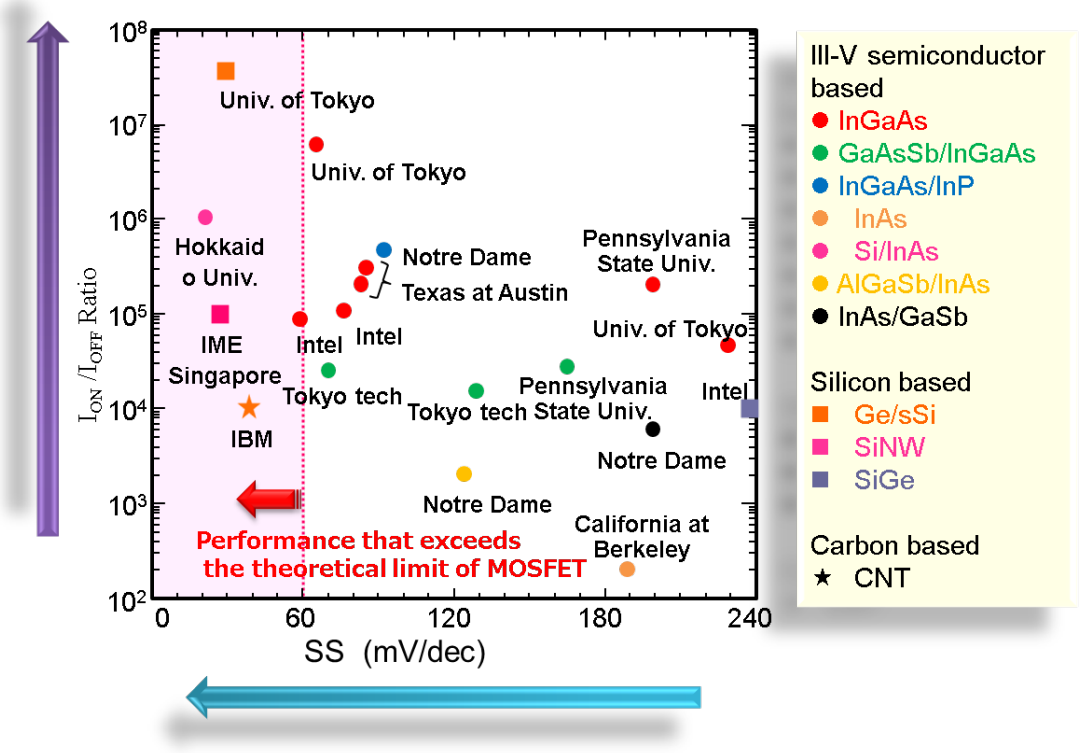


Figure 1.4 – Subthreshold Slop (SS) and Ion/Ioff ratio of different types of TFET. On top of the figure, a summary of the best achievement of high ON current TFETs compared with MOSFET.GNR-TFET expected to exceed the MOSFET ON current.

To enhance the I_{ON} tunneling current materials with narrow band gap and small effective masses are favorable [25],[26]. The simulation work by Knoch et al. [27],[28] showed that 1-D semiconductor-based TFETs are recommended due to its exceptional gate control and higher tunneling probability [28].

1.2.3 Recent attempts of two dimensional-based TFET

As mentioned in the previous section two-dimensional (2D) semiconductor material is favorable for TFET applications. Due to its atomically thin body, 2D-based TFETs expected to show a superior gate control, which increases the electric field strength at the tunneling junction. Therefore, the transmission probability significantly increases and consequently the I_{ON} current expected to be improved as well. Many simulations works confirmed the advantages of 2D semiconductors materials than bulk semiconductors as a platform material for TFET applications [29]–[38].

Recently, in 2015 Sarkar et al. successfully fabricated the first planner TFET from two-dimensional semiconductor with SS of 31 meV/dec and 10^6 I_{ON}/I_{OFF} ratio [39]. Sarkar et al. used monolayer MoS_2 as a channel material and highly p-doped Ge as a source. However, the ON current is still very low (~ 1μA at 1V drain voltage) which is three orders of magnitude lower than the high scaled MOSFET. Also, due to its planner structure, the ON current is highly dependent on the interface area between the channel and the source. So that, the only way to increase the ON current is by increasing the interface area which gives rise to difficulty on the future scale down of such kind of TFET. Even by using low thickness and high κ dielectric materials the ON current will not increase, but only the SS may improve. In reality, the function of the gate in that device is turning the device off. Because the device will be in the ON state when the gate voltage is zero and negative voltage should apply to suppress the electron tunneling.

Müller et al. [40] fabricated graphene *p-i-n* junction, with three independent gates, from 30 nm wide GNR. They claimed that interband tunneling is observed, however, due to the low band gap Eg they were not able to extract a clear inverse subthreshold slope since leakage currents deteriorate the off-state behavior of the device [41]. It worth to mention that, Nakahari et al., [42] studied the same structure like our device in chapter four, but with different dimensions and entirely different purpose. In his work, he tried to use the built-in potential of the *p-i-n* junction to decrease the OFF current in the graphene-based FET. For the same purpose, he proposed a new method [43] to introduce energy gap in the graphene.

All the previous work has the same issue that is the low I_{ON} current. Based on the WKB approximation, low dimensional and low effective mass material exhibit higher tunneling probability. Therefore, GNR has been considered one of the most promising candidates for TFET applications, due to its atomically thin body and 1D nature. Moreover, GNRs have a width-tuneable narrow bandgap [44]–[49], and more flexible to

large-scale integration and planar processing compared to carbon nanotubes (CNTs). Further, GNR can be electrostatically doped, by varying the gate polarity one can convert TFET from n-type to p-type. This great feature of GNR will make the fabrication of complementary switches very flexible. However, realizing a reliable GNR-TFET is quite challenging. To introduce a reasonable energy gap to the GNR, the width should be around 10 nm, which is a very tough task to achieve. Therefore, fabrication methods and techniques should be developed to realize very narrow GNR with a sizable energy gap. Also, GNR edge states and quantum condiments come to the pictures at such narrow ribbons. These challenging and difficulties should be taken into consideration during the fabrication of the GNR-TFET.

1.3 The Purpose of this study

There has not been any experimental report of GNR-TFET operation until now. Therefore, this dissertation investigates and studies the feasibility of realizing GNR-TFETs and aim to:

- Demonstration of BTBT based GNR-TFET
- Demonstrate I_{ON} >> conventional TFET

This includes understanding the physics of the GNR *p-i-n* junction because a TFET is, in principle, a *p-i-n* junction. According to [50]–[52], the carriers cannot be confined in graphene *p-i-n* junction. Therefore, the first step was fabricating and studying the carrier transport in the GNR-PIN junction. This, however, requires the graphene to have a sizeable bandgap opening. By patterning 2D graphene sheet to a very narrow ribbon with a width of less than 20 nm a sizable band gap can be opened. For a *p-i-n* junction, additionally accurately defined doping regions are necessary. Since graphene can be electrostatically doped [53],[54] and this method is easier and more versatile than other doping methods[55], [56], I planned to fabricate top gates to introduce doping to the GNRs. Fabricating top gates with very narrow separation gap (~ 25 nm) is quite challenging by using positive tone EBL-resist. So that, optimizing the fabrication process or propose fabrication methods are needed to tackle this kind of fabrication tool limitations. First, I designed and fabricated GNR *p-n* junction to study the electronic transport through consecutive *p*-doped and *n*-doped regions. The objective of this step is to get evidence of the existence of Band-To-Band-Tunnelling (BTBT) tunneling and suppression of unwanted Klein tunneling. Then GNR-TFET (triple gated configuration)

fabricated and characterized, which confirmed for the first time the existence of BTBT current in a planner GNR transistor. Subthreshold swing (SS) as small as ~22 mV/dec is reported. In the following section, the structure of the thesis will be shown.

1.4 Thesis Structure

This dissertation organized into six chapters. Below the content each chapter is shown:

- Chapter 2: **Graphene Band-to-Band Tunnel Model.** In this chapter, graphene is introduced, and some of its extraordinary properties which related to this work are reviewed and discussed. The atomic structure and electronic properties of graphene are included. Then I summarized the Band-To-Band Tunnel (BTBT) model of the two-dimensional (2D) semiconductors, followed by the physics of subthreshold swing (SS) slope in GNR-TFET.
- Chapter 3: **Fabrication and Experimental Setup**. In this chapter, I first provide some detail about electron beam lithography. Then the fabrication process of our two top gate PIN junctions and three top gates GNR devices is explained in detail. Also, I mentioned the experimental difficulties and its diagnosis. I explained in details the GNR patterning using HSQ by EBL-RIE technique.
- Chapter 4: **Sharp switching behavior in GNR *p-n* junction**. In this chapter, the GNR *p-n* junction structure is explained. The measurement set up and procedures are explained in detail. The results and the analysis of the GNR *p-n* junctions are explained and discussed in details.
- Chapter 5: **GNR Tunnel Field Effect Transistor**. In this chapter, I presented the results of the simulation study of the triple gate GNR devices with different dimensions. GNR-TFET introduced experimentally for the first time. The SS slope for two devices showed temperature independence at low temperature with SS of 47 mV/sec.
- Chapter 6: **Summary:** In this chapter, I conclude this thesis. Also, outlook on future work regarding graphene TFETs is provided.

2 Graphene Nano-Ribbon Band-to-Band Tunnel Model

2.1 Introduction

Graphene is a single layer of 2 dimensional (2D) carbon atoms arranged in a honeycomb lattice. Graphene can be considered as the root of all other graphitic materials such as carbon nanotubes (CNT) and other fullerenes of all other dimensionalities (Figure 2.1) [57]. Graphene has exceptional mechanical, electrical and thermal properties [58], [59]. The most attractive feature in graphene is superb electronic properties, for example very high mobility, long mean free path at room temperature and exceptional ballistic transport. These superior features expected to enhance the device speed [60]. The graphene mobility is much greater than that of the conventional semiconductor, of approximately 1400 $cm^2 V^{-1} s^{-1}$. Subsequently, graphene has been counted as a promising candidate material for electronic applications. However, its applications in digital electronic are impossible by the lack of energy gap in 2D pristine graphene. Therefore, opening an energy gap in graphene is essential for graphene-based electronics.

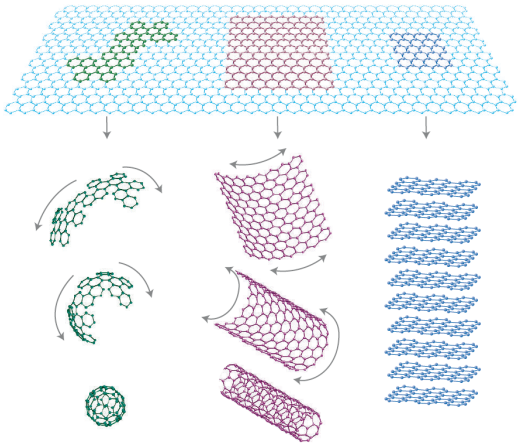


Figure 2.1. Graphene is the root of all other graphitic materials of all other dimensionalities. Carbon-nanotubes, 0D buckyballs, or stacked into 3D graphite. Reproduced from [57].

Opening an energy gap (E_g) in graphene can be achieved by shrinking the 2D graphene sheet to narrow ribbon, called GNR, with widths smaller than 50 nm[47]. Many techniques and methods have been developed to make GNRs, such as chemical[61]–[64], sonochemical [65],[66] and lithographic [47],[67],[68] methods. Recently a novel of e-beam lithography combination with HIM milling has been demonstrated and achieved a minimum feature size of 3 nm [69]. In section 2.3 below, the different types of GNRs and its characteristics in will be discussed in details.

Ambipolar field effect behavior of carriers is one of the great features of graphene, which afforded the possibility to control the carrier type, concentration, and the Fermi level position in graphene [70],[71],[72], top and back gates are usually used for that purpose[70],[73]. In this method, Fermi level of the intrinsic graphene can be precisely tuned to the conduction or valence band, corresponding to the gate voltage polarities. n and p typed graphene can be realized by applying positive and negative voltages respectively (see Figure 2.2).

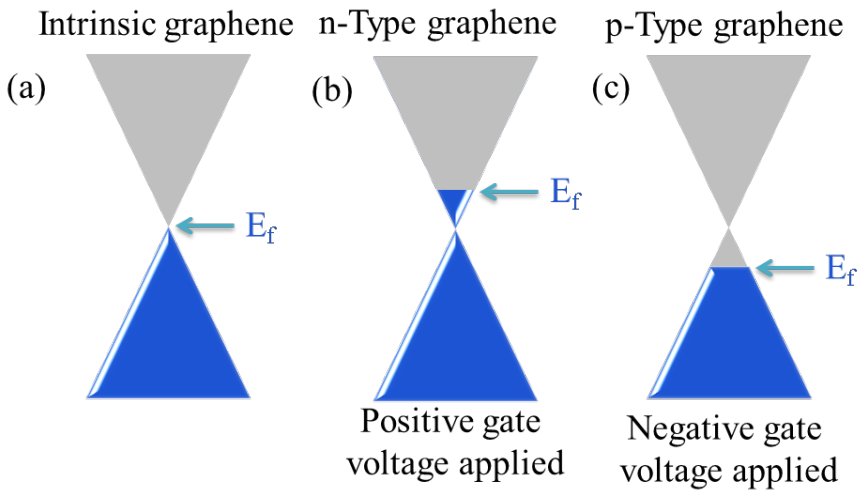


Figure 2.2. (a) Band structure of intrinsic graphene. Band structures of (b) n-Type (positive gate voltage applied) and (c) p-Type (negative gate voltage applied) graphene with the bandgap. EF lies in conduction and valence band, respectively.

2.2 Band Structure of Graphene

Figure 2.3 shows the hexagonal graphene lattice, where each unit cell contains two carbon atoms, A and B. The lattice vectors $a_1 = \frac{a}{2}(\sqrt{3}, 1)$ and $a_2 = \frac{a}{2}(\sqrt{3}, -1)$, where $a = \sqrt{3}a_{c-c} = 2.46$ Å is the lattice constant. In the reciprocal lattice space, the first Brillouin zone spanned by the wave vector $K = (K_x, K_y)$ is also hexagonal. Of particular importance are the two inequivalent points K *and* K' at the six corners of the Brillouin

zone. Their positions are given by $\pm\frac{2\pi}{\sqrt{3}a}(1,\frac{1}{\sqrt{3}})$,$\pm\frac{2\pi}{\sqrt{3}a}(0,\frac{2}{\sqrt{3}})$, and $\pm\frac{2\pi}{\sqrt{3}a}(-1,\frac{1}{\sqrt{3}})$. The low-energy band structure of graphene can be well defined by a simple tight-binding Hamiltonian considering only nearest-neighbor hopping and one π orbital per carbon atom. This simple model allows for an analytical solution of the energy bands [74]:

$$E^{\pm}(K_x, K_y) = \pm\gamma_0\sqrt{1 + 4\cos(\sqrt{3}\,K_x a)\,\cos(K_y a) + 4cos^2(K_y a/2)} \quad 2.1$$

Where $\gamma_0 \sim 2.7\ eV$ is the nearest-neighbor hopping integral shown in Figure 2.3a. In pristine undoped graphene, the conduction and valence bands touch at the $K\ and\ K'$ points. Expanding Eq. (2.1) near $K(K')$ yields a linear dispersion:

$$E^{\pm}(\kappa) = \pm\hbar v_F|K| \qquad (2.2)$$

Where $\kappa = K - K(K')$ is is the wave vector measured from $K(K)'$ and v_F is the electronic group velocity given by:

$$v_F = \frac{\sqrt{3}\gamma_0 a}{2\hbar} \qquad (2.3)$$

Equation (2.2) produces touching conic bands at the $K\ and\ K'$ points of the Brillouin zone as shown in Figure 2.3c. Electrons in graphene are referred to as Dirac fermions because of this linear, photon-like dispersion and the touching points in momentum space are called Dirac points. The Fermi level E_F resides precisely at the Dirac point in undoped graphene. E_F increases (decreases) upon electron (hole) doping. Equation (2.2) is a good approximation as long as the energy does not deviate too far from E_F, or conversely that the momentum does not deviate too far from the $K(K')$ point. This condition is satisfied in most current graphene devices [75].

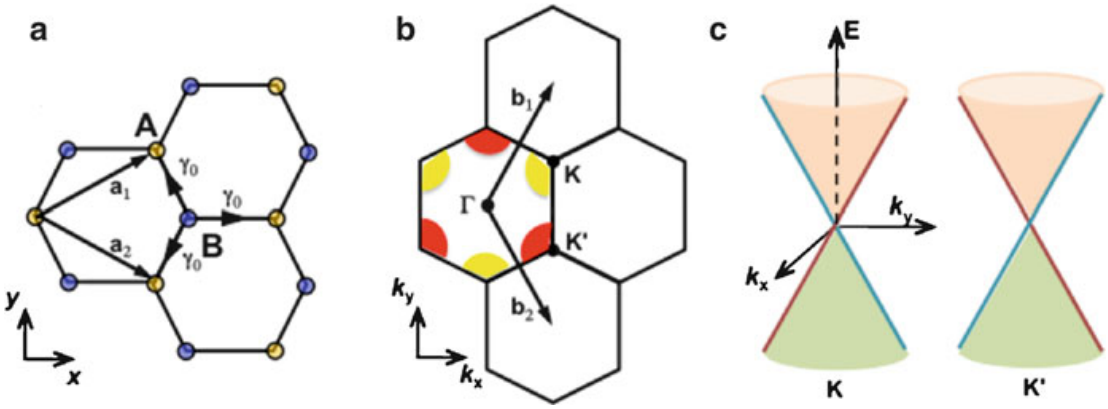


Figure 2.3. The band structure of graphene. (a) The hexagonal lattice of graphene. (b) The reciprocal lattice in momentum space. (c) The Dirac cones near the $K\ and\ K'$points of the Brillouin zone Carriers in different cones with opposite momenta have the same pseudo spin. Reproduced from [75]

2.3 Graphene Nanoribbon

The electronic properties of a graphene sheet change dramatically as the size shrinks [76], [77]. Graphene nanoribbons (GNRs) are a potential solution for using graphene in digital electronics since they can have a band gap. Two important considerations emerge in graphene nanoribbons (GNRs), namely, quantum confinement and the effect of edge states as will be discussed later in this chapter. Figure 2.4(a and b) show schematics of two different kinds of GNRs with the same width (W): armchair in (a) and zigzag in (b). In both cases, electronic states are constricted in the x direction, similar to a particle confined in a one-dimensional quantum well. This quantum confinement leads to quantized momentum $k_x = n\pi/W$ (n = 0, 1,2, . . .). It divides the Brillouin zone into discrete energy bands as shown in Figure 2.4c [75].

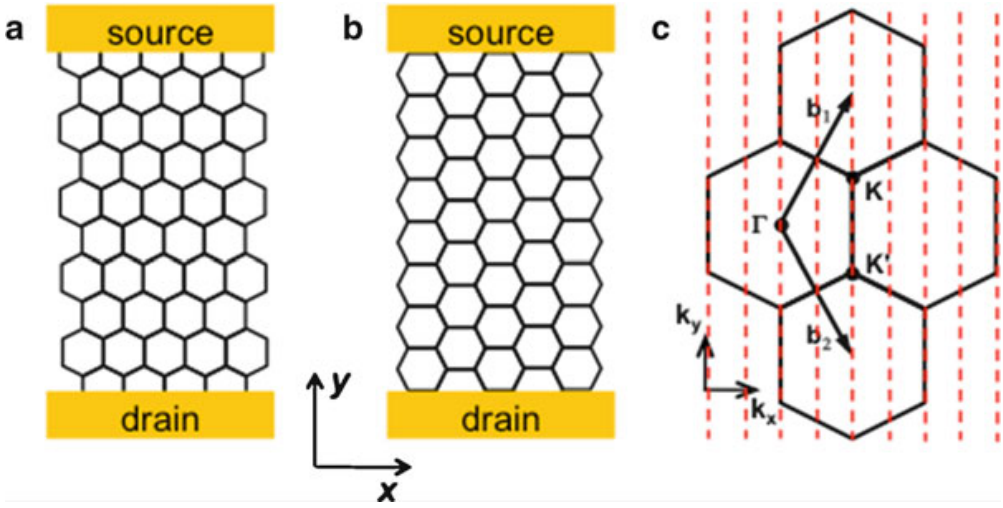


Figure 2.4 - The edge configurations of nanoribbons. (a) An armchair ribbon. (b) A zigzag ribbon. (c) Confinement in the x direction quantizes kx, as illustrated by the dashed lines. This quantization slices the band structure of 2D graphene into 1D discrete bands. Reproduced from (without permission) [75].

The spacing between adjacent bands is on the order of $\Delta E \approx \hbar v_F \pi / W$ or 2eV/W(nm). The finite gap in its band structure makes the GNR potentially useful in digital nano-electronics, an arena of applications closed to 2D single-layer graphene because of the lack of a band gap. In practice, this is a technically challenging route since a sizable bandgap of ~ 1 eV requires a small W, on the order of a few nm. GNRs may be metallic or semiconducting depending on their edge termination. This sensitivity shouldn't be surprising since GNRs are really just unrolled carbon nanotubes. In Figure 2.5, the electronic dispersion of a zigzag (a) and two armchair GNRs (b, c) are shown [78], [79]. These results are obtained by solving the Dirac equation with appropriate boundary conditions. In realistic devices, the edge often contains a mixture

of zigzag and armchair regions. Han et al. [67] studied extensively the carrier transport of GNR structures patterned by EBL technique. They showed that GNRs with width W <100 nm shows a decrease in minimum conductance (g_{min}) at low temperature. The narrowest GNRs show the greatest inhibition of g_{min}. The suppression of G close to the Dirac neutrality point (DNP) implies an energy gap opening [67]. The energy gap dependence on the GNR width is shown in Figure 2.6 [67]. Furthermore, Han et al. studied the crystallographic orientation effect on the size of the energy gap but they could not to confirm any relation between crystallographic direction and the energy gap[67].

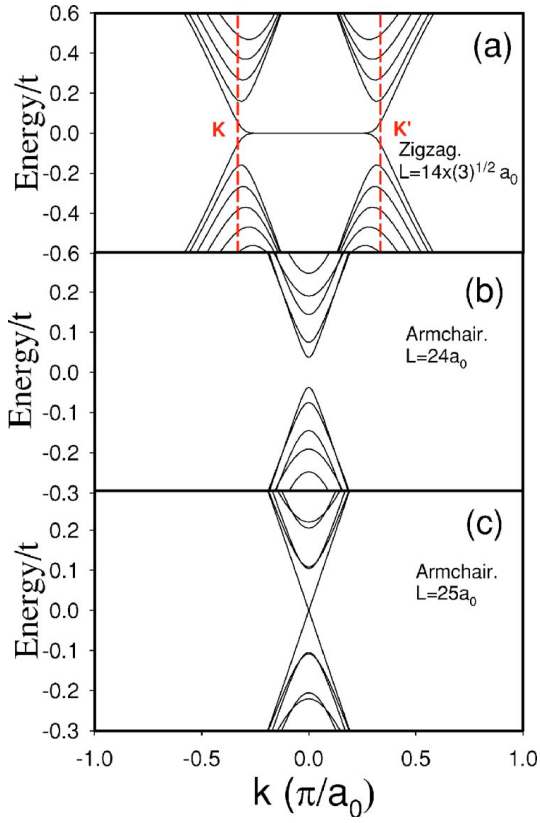


Figure 2.5 - The band structure of nanoribbons showing the dispersionless, localized edge states in a zigzag GNR in (a). The bands of gapped and gapless armchair GNRs are shown in (b) and (c) respectively. Reproduced from (without permission) [79]

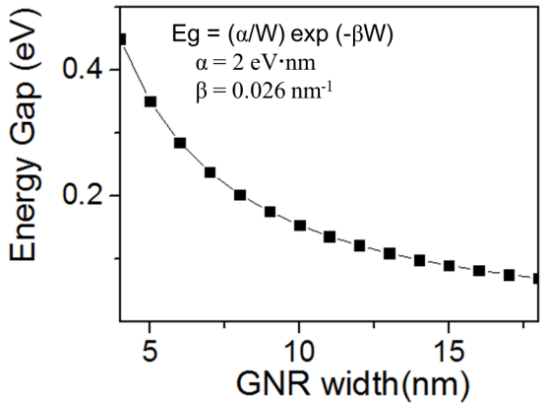


Figure 2.6 – Energy gap (Eg) as a function of GNR width. Reproduced from (without permission) [67].

2.4 The physics of Band-to-Band Tunnel Transistor

Tunneling field-effect transistors (TFET) became one of the most promising successors for MOSFET. These type of transistors can possibly achieve electronic switching with energy much lower than traditional MOSFET. The recent rise of 2-D semiconductors offers a new material platform for achieving these devices. TFETs take benefit of the ability of interband tunneling of charge carriers to overcome the MOSFET thermal limit of 60 mV/dec. In a TFET, switching ON and OFF can be achieved abruptly by controlling the relative position of the band in the channel via the gate bias. This function can be accomplished in a reverse-biased *p-i-n* structure.

2.4.1 Device structures and working mechanism

In Figure 2.7(a) a schematic diagram of an n-type GNR-TFET, which consisted of the heavily doped p-type source and heavily doped n-type drain separated by a central channel. The p-type source and n-type drain are achieved by electrostatic doping the GNR underneath the source and drain contacts respectively. Here, a quasi-one-dimension GNR is considered. TFET operation mechanism can be explained as follow: in the TFET OFF state (Figure 2.7b), the conduction band edge of the channel is located above the edge of the source valence band, so that BTBT is inhibited due to the wide tunneling length (W_L) as shown in Figure 2.7b, in this case, the TFET become in the off-state. Applying a negative gate voltage (Figure 2.7c) pushes the energy bands down. As the channel conduction band edge has been pushed below the source valence band edge, a conductive channel opens up, and the carriers can tunnel through the narrow barrier to the empty states of the channel. The carriers outside the energy window $\Delta\Phi$ are filtered out and only carriers inside the allowed energy window can tunnel into the channel.

Jena et al. [2008] developed a theory for interband tunneling in semiconducting GNRs and carbon nanotube p-n junction [80]. However, at 2012 Majumdar published a correction [81] to some equations in Jena's paper followed by confirmation of Jena [82]. Therefore, both of [80] and [81] should be considered during the treatment of BTBT in GNRs. Based on Jena's theory, Zhang et al. [83] proposed an analytical model of GNR-TFET. Due to the similarity of Zhang model to our fabricated GNR-TFET, I used the model here to drive the tunneling current (I_{ON}) as shown below. The electrostatics of 1-D GNR is resolved by a potential surface method, where the GNR surface potential, $\Phi_{F(x)}$, is given by the 1-D Poisson equation [83].

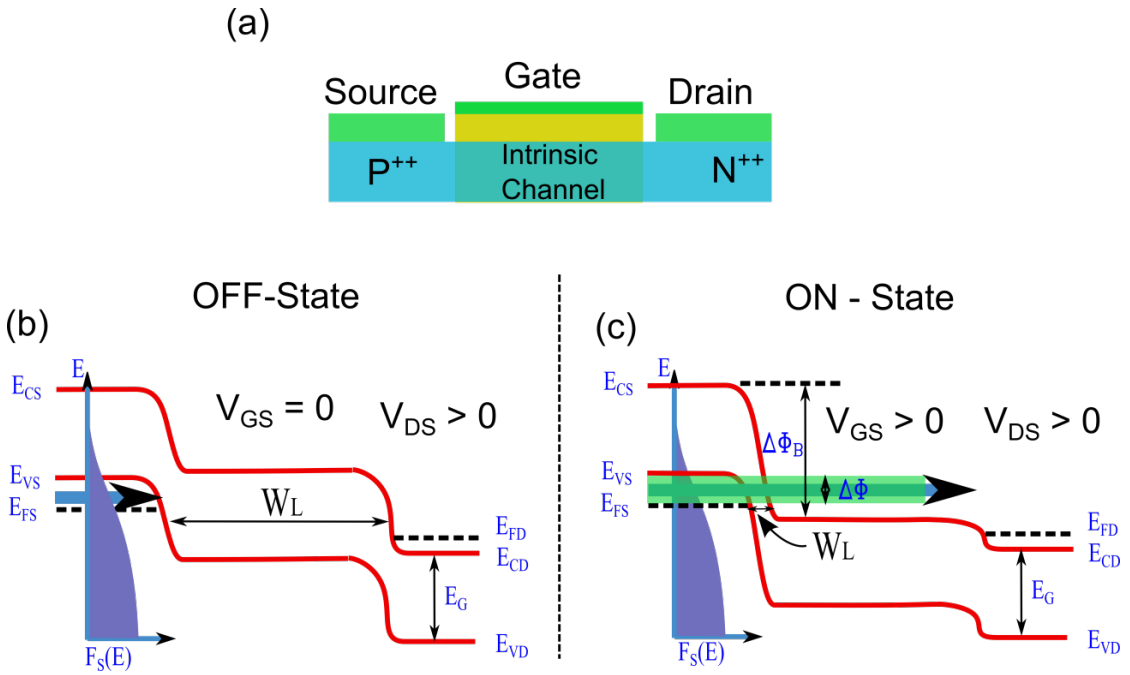


Figure 2.7. The operation mechanism of TFET. (a) Schematic diagram of n-type TFET. (b) Schematic energy band profiles for the OFF state. (C) Schematic energy band profiles for the ON state.

$$\frac{d^2\Phi_F(x)}{dx^2} - \frac{\Phi_F(x) - \Phi_G - \Phi_B}{\lambda^2} = -\frac{q(\pm N)}{\varepsilon_{GNR}} \quad (2.4)$$

Where Φ_G is the gate potential

$q\Phi_B = ((E_G/2) - qV_T\, ln(N/n_i))$ is the built-in potential

$E_G = (2\pi\hbar v_F/3W_{GNR}) \sim 1.3/W_{GNR}$ [79],[84] the bandgap of GNR

$v_F = 10^8$ cm/s is the Fermi velocity of carriers in graphene [85]

W_{GNR} is the ribbon width

V_T is the thermal voltage which h given by ($qV_T = K_BT$)

n_i is the intrinsic carrier concentration,

N is the doping concentration

$\lambda_L = \sqrt{(\varepsilon_{GNR}/\varepsilon_{OX})t_{GNR}t_{OX}}$ is the relevant length scale for potential variations;

ε_{OX} and ε_{GNR} and are oxide dielectric and GNR constants, respectively, and t_{OX} is the gate oxide thickness. t_{GNR} = 0.35 nm [86] is the GNR thickness.

The tunneling ON-state current (I_{ON}) is given by the integration of the product of charge flux and the transmission probability inside the energy window $\Delta q\Phi$

$$I_{ON} = \int q\, v_g \rho_{GNR}(K) \times [f(E - E_{FD}) - f(E - E_{FS})] T_{WKB} dK$$

$$= \int_0^{\Delta\Phi} \frac{q}{\pi\hbar} v_g \rho_{GNR}(K) \times [f(E - E_{FD}) - f(E - E_{FS})] T_{WKB} dK$$

$$I_{ON} = \frac{q^2}{\pi\hbar} T_{WKB}\, V_T \times \begin{bmatrix} ln\left(exp\left(\frac{(\Delta\Phi - E_{FS})}{qV_T}\right) + 1\right) \\ -\ln\left(exp\left(-\frac{E_{FS}}{qV_T}\right) + 1\right) \\ +\ln\left(exp\left(\frac{-V_{DS}}{V_T}\right) + 1\right) \\ -\ln\left(exp\left(\frac{(\Delta\Phi - qV_{DS})}{qV_T}\right) + 1\right) \end{bmatrix} \quad (2.5)$$

Where $v_g = \frac{1}{\hbar}\frac{dE}{dK}$, $\rho_{GNR}(K) = \frac{1}{\pi}$ is the one dimensional density of states, and T_{WKB} is the tunnelling probability of a triangular potential with a barrier height of E_G [87] and given by the WKB approximation :

$$T_{WKB} \approx exp\left(-\frac{4W_L\sqrt{2m^*}\sqrt{E_G^3}}{3q\hbar\,(E_G + \Delta\Phi)}\right) \quad (2.6)$$

$$T_{WKB} \approx exp\left(-\frac{4}{3}\sqrt{\frac{E_G}{13.6}}\left(\frac{1}{1+\frac{\Delta\Phi}{E_G}}\right) \times \sqrt{m^*} \times \frac{W_L}{a_0}\right) \quad (2.7)$$

T_{WKB} is dependent on the bandgap E_G. Here, W_L is the tunneling length and describes the spatial extent of the transition region at the source–channel interface (see Figure 2.7); it depends on the device geometry. Using Eq. 2.5 and 2.6 the current density is analyzed as a function of the gate-source potential difference at room temperature [88]. The off state current for the one-dimensional case is given below [88]:

$$I_{OFF} = \left(\frac{q^2 V_T}{\hbar\pi}\right) e^{\left(\frac{-\Delta\Phi_B}{qV_T}\right)} \quad (2.7)$$

2.4.2 High I_{ON} current

Achieving high ON current is the main challenge facing TFETs. Thus because the ON current significantly relies on the tunneling probability, T_{WKB}, of the tunneling barrier. In this section, the targeted parameters and how to optimize the I_{ON} current in TFET will be discussed. The following parameters should be satisfied in TFETs [89] To surpass CMOS transistors,

- I_{ON} > 1000 µA/µm
- SS_{avg} below 60 mV over more than five orders of magnitude of current

- $I_{ON}/I_{OFF} > 10^5$
- and $V_{DD} < 0.5$ V

To achieve a high tunnel currents and a sharp SS, the transmission probability of the source-channel barrier would be close as possible to unity for a minor variation in V_{GS}. The WKB approximation, shown in equation (2.6), proposes that the following parameters should be reduced for higher tunneling probability:

i. Energy gap (E_g),

ii. Tunnelling length (W_L)

iii. Carrier effective mass (m*)

Whereas m* and E_G depend only on the material (material parameter), but W_L is greatly affected by some factors, for example, the geometry of the device, doping profile, dimensions, and gate capacitance [90], [91]. A narrow W_L implies a strong gate control of the channel bands. Moreover, strong modulation needs a high dielectric permittivity (high-κ) materials with thin thickness [92],[93]. Also, the channel body thickness would be reduced [28],[91],[94], [95] that means the 2D and 1D material is the best choice for TFET. The sharpness of the doping level at the source-channel junction is also crucial[89]. That necessitates a drop in the doping level of around 4–5 orders of magnitude within a few nanometers [93]. However, the source Fermi energy should not be too large to avoid the energy filtering effect described above [28]. The doping level at the source is an essential parameter [96] as it will be discussed later.

2.4.3 Low Subthreshold Swing (SS)

Cao et al. [96] showed that the subthreshold swing (SS) is mainly consisted of two components, as shown in Eq.(2.7)

$$SS = \frac{SS_T SS_{FD}}{SS_T + SS_{FD}} \quad (2.7)$$

SS is the total subthreshold swing, SS_T is subthreshold swing (Tunnelling probability contribution), and SS_{FD} is subthreshold swing (truncated Fermi-Dirac distribution contribution). Where SS_T is given by:

$$SS_T = \frac{2\sqrt{2}\ \ln(10)h}{-q\pi\sqrt{m^* E_G}\ \frac{dW_T}{d\Phi}} \quad (2.8)$$

Also, SS_{FD} is giving by:

$$SS_{FD} = \frac{\ln(10)KT}{q}\left(1+\exp\left(\frac{E_{CS}-E_{FS}-\Delta\Phi}{KT}\right)\right)\ln\left(\frac{1+\exp\left(\frac{E_{FS}-E_{CS}+\Delta\Phi}{KT}\right)}{1+\exp\left(\frac{E_{FS}-E_{CS}}{KT}\right)}\right) \quad (2.9)$$

Where ħ is the reduced Planck`s constant.

Now the behavior of the SS at different doping levels will be explained:

- Low Doping Level Regime

In Eq. (2.9), when the doping concentration (Na) is low, E_{FC} will be inferior E_{FS} and SS_{FD} reduced to

$$SS_{FD} = \frac{\ln(10)\Delta\Phi}{q} \quad (2.10)$$

If the tunneling probability is assumed to be close to unity[28], in this case, the total SS is a function of SS_{FD} this implies that SS will be very close to zero by approaching ΔΦ to zero. Moreover, the SS exhibit a linear dependence on ΔΦ for larger ranges of SS < 60 mV/dec. [28]. However, low doping (Na) means low I_{ON} current.

- High Doping Level Regime

In Eq. (2.9) if the Na became strong the Fermi level E_{FS} will be pushed above the E_{CS} , in this case, Eq.(2.9) reduces to

$$SS_{FD} = \frac{\ln(10)KT}{q}\left(1-\exp\left(\frac{-\Delta\Phi}{KT}\right)\right) \quad at\ (0 < \Delta\Phi < 2KT)\ (2.11)$$

From Eq. (2.11), it is obvious that SS_{FD} is exponentially approaching zero by decreasing ΔΦ. On the other hand, the SS_{FD} will increase rapidly by increasing ΔΦ (in contrast to the linear dependence in the low doping regime). From the above discussion and Eqs. (2.8, 2.10 and 2.11) one can realize that the source doping level (Na), tunneling length (W_T), band gap (E_G) and the effective mass (m*) are the four critical parameters for TFET performance [90]. The former two parameters can be classified as electrostatic parameters and the other two parameters as material parameters [96]. This means low energy gap material with low effective mass will boost the I_{ON} and decrease the SS (see Eq.2.6). The other two parameters (W_T and Na) at some extent they are related to each other. Increasing Na will decrease W_T, moreover, by change the doping profile (abrupt doping profile of the source) decrease the tunneling length as well. Therefore, GNR-TFET is one of the

promising devices due to the small E_G, small effective mass m* and excellent electrostatic control due to the thin body (quasi-1D).

2.5 Summary

In this chapter, the main advantages of using GNR in the TFET applications were discussed. An analytical model for both ON state and OFF state currents has been discussed. According to this model, I would like to emphasize on the main parameters that can enhance the GNR-TFET performance as follow:

- ON Current boost parameters:
    - Low energy gap (E_G) ---------- satisfied in GNR
    - Low effective mass ---------- satisfied in GNR
    - Channel thin body ---------- satisfied in GNR
    - High source doping level
    - High dielectric permittivity (High k)
    - Low dielectric thickness
    - Double gate channel control
    - Appropriate source/drain metal contacts (e.g.using Pd at p-doped source)
- OFF current suppression parameters
    - Drain voltage < Eg/q
    - Low drain doping level
    - Heterostructure (low energy gap at source and higher energy gap at channel and drain)
    - Heterostructure dielectric engineer (high-k dielectric in source-channel junction and low-k at the channel-drain junction)
    - Underlap the top gate at the channel-drain junction (shift the top gate away from the channel-drain junction.

3 Fabrication and Experimental Setup

3.1 Introduction

The unique feature of all semiconducting materials is the existence of average energy gap (up to ~1.2 eV), which makes it possible to control the carrier transport through them. In graphene, the energy gap is zero, meaning that the carrier transport through a graphene-based device would be impossible. Moreover, even with the existence of local potential barrier (e.g. *p-n* junction), the carrier cannot be confined due to the Klein tunneling phenomena[50]–[52], [97]–[100]. However, patterning 2-D graphene into a narrow ribbon and confining the carriers to a 1-D system, an energy gap can be opened. The value of the energy gap can be calculated from the empirical equation $W = (\hbar\, v_f)/E_g$ ($\hbar$ is the reduced Plank constant, W is the GNR width and $v_f = 10^6$ m/s is the Fermi velocity)[101]. According to this equation, GNR widths of less than 10 nm are needed to open an energy gap higher than 100 meV. Therefore, patterning of GNRs with sub-10 nm widths is the main challenge. Furthermore, TFETs in general consists of a *p-i-n* junction: the source is heavily p-doped, and the drain is n-doped with an intrinsic (I) region in between as depicted in Figure 3.1.

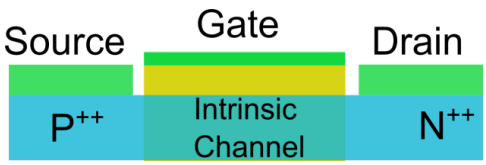


Figure 3.1. Schematic diagram of the TFET

Therefore, our GNR-TFET will have the same structure. However, in contrast to the conventional semiconductor, the strong C–C bonds in graphene makes the chemical doping is tricky and tough. The only viable method successfully demonstrated is electrostatic doping that has been already used for realizing tunnel junctions in CNT FETs[10], and the same can be attained for GNRs. As explained in chapter 2, GNRs can be doped electrostatically, Figure 3.2, shows illustrate how the electrostatic doping can be introduced by a vertical electrical field created by a top gate.

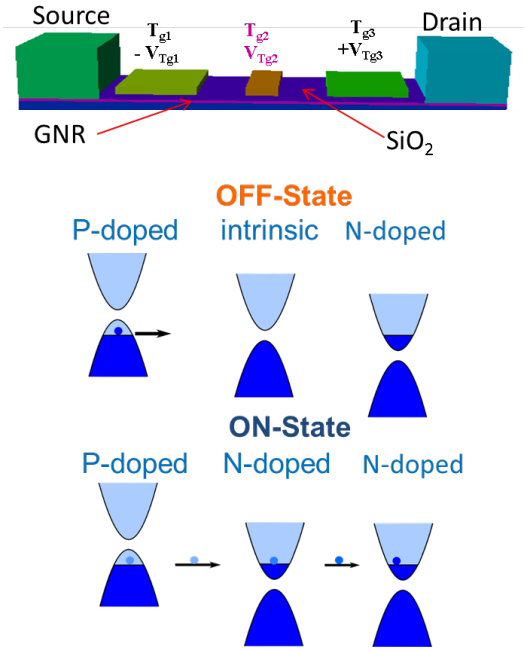


Figure 3.2. Schematic diagram of our electrostatic doped GNR-TFET (top) Tg1 and Tg3 are used to define the p-doped and n-doped regions by applying negative and positive voltage respectively. Switching between OFF state and ON state by the middle gate (bottom).

Currently, the most reliable technique for fabricating graphene nano devices is Electron beam lithography (EBL). Usually, EBL followed by one of the following processes, 1) Reactive-Ion-Etch (RIE) or 2) metal deposition and lift-off. In this technique, the EBL used to define the structure with the desired dimensions by writing on positive or negative e-beam resist. Then, in case of negative e-beam resist the EBL step will be followed by RIE. however, in case of positive e-beam resist the EBL step will be followed by depositing the desired metal then lift-off. The main drawback of using EBL-RIE method is introducing edge roughness to the GNR that affects the electronic transport significantly [67]. The finest structures and resolution that can be realized by EBL depends on many parameters, accordingly the yield can vary from one fabrication to another. Here, I will discuss extensively each fabrication step including optimization, challenges, and diagnosis that introduced in each fabrication step.

3.2 Optimization of Electron Beam Lithography Writing Technique

For all lithographic steps, direct electron beam lithography (EBL) was used (Elionix ELS-7500). Understanding the EBL writing process is very crucial to achieve very fine

structures as required for GTFETS. To achieve high-resolution writing, tight control of the following three main parameters are essential:

iv. Beam Size (BS)

v. Beam Step Size (BSS)

vi. Writing Strategy.

3.2.1 Beam Size

When the electron beam strikes a point on the resist covered sample, the spatial distribution g(r) of the electrical charge provided by the beam irradiation over the resist is approximated by the sum of the two Gaussian distribution functions as follows:

$$g(r) \propto g_f(r) + \eta g_b(r), \quad (3.1)$$

$$g_f(r) = \frac{1}{\pi\sigma_f^2} e^{\left(-\frac{r^2}{\sigma_f^2}\right)}, (3.2)$$

$Forward\ scatter\ distribution\ caused\ by\ the\ resist$

$$g_b(r) \frac{1}{\pi\sigma_b^2} e^{\left(-\frac{r^2}{\sigma_b^2}\right)}, (3.3)$$

$Back\ scatter\ distribution\ \ mainly\ due\ to\ the\ substrate\ interaction$

$$\eta = \eta(Z, Va), (3.4)$$

$the\ resist\ sensitivity\ ratio\ between\ back\ and\ forward\ scatte$ring

Where σ_f,σ_b and η are the forward scattering distribution, backscattering distribution and sensitivity ratio between forward and back scatter respectively. When the specimen is a Si substrate covered with a resist, the further approximation is shown below can be used:

$$\sigma_f^2 = \sigma_{f0}^2 + R_{rms}^2 \ (3.5)$$

$Forward\ scatter\ distribution\ (beam\ diameter\ is\ considered)$

$$\sigma_{f0} = 9X10^8 \left(\frac{t}{V_a}\right)^{1.5}, (3.6) \quad forward\ scateer\ distribution$$

$where\ t\ is\ the\ resist\ thickness\ and\ Va\ is\ the\ acceleration\ voltage$

$$\sigma_b^2 = \sigma_{b0}^2 + R_{rms}^2, (3.7)$$

$Back\ scatter\ distribution\ \ (beam\ diameter\ is\ considered)$

$\sigma_{b0} = 1.03X10^{-13}V_a{}^{1.7}$, (3.8) Back scatter distribution

$R_{rms} = 0.5\ x\ (\ beam\ diameter)$ is the mean square radius of the beam diameter

From Eq (3.5), when the beam diameter is small enough against the forward scatter (σ_{f0}^2), the beam diameter can be ignored. According to the specifications provided by Elionix about the ELS-7500 (see Figure 3.3a), for a beam current of 20 pA , beam diameter of only ≈ 2-3 nm is expected. Therefore, during our GNR patterning, 20 pA current is used throughout. Moreover, equations (3.6 and 3.7) indicate that by decreasing the resist thickness and increasing the acceleration voltage, higher resolution can be achieved. Figure 3.3b exhibits the interaction cross-section of the e-beam with the resist and substrate at different acceleration voltages. The highest available beam energy for the ELS-7500 is 50 kV, which is used here.

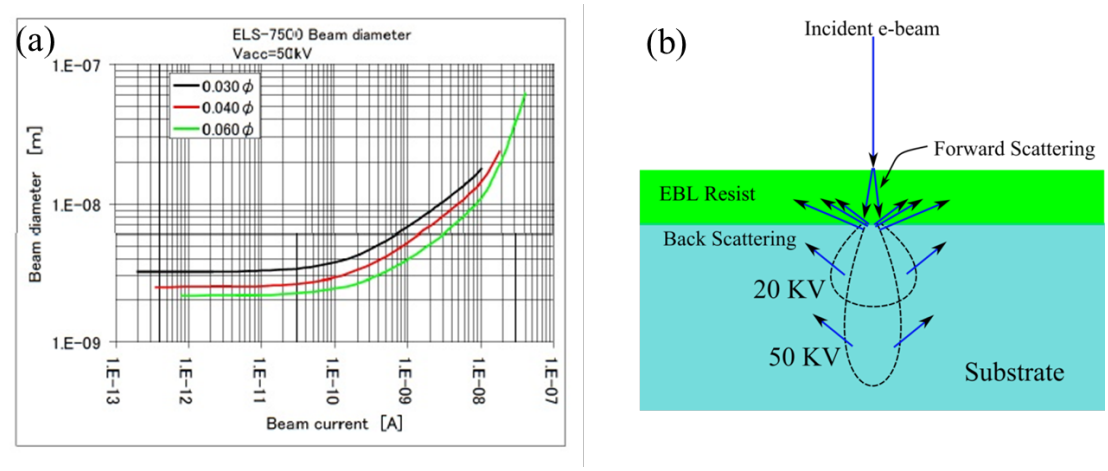


Figure 3.3. (a)Beam diameter as a function of beam current at acceleration voltage 50 KV forELS-7500. Reproduced from (without permission). (b) Electron beam – matter interaction cross section https://www.seas.upenn.edu/~nanosop/Elionix_Recipes.htm]

From the above discussion, the requirements for a high-resolution writing recipe can be summarized as follows:

- Minimize the beam diameter
- Decrease the resist thickness
- Increase the acceleration voltage

3.2.2 Beam Step Size

EBL is, compared to ultraviolet lithography, a spot exposure technique. However, line or filled pattern is more commonly required in the application. Due to the principle of EBL, there are therefore some points that must be considered when approaching small pattern. Beam step size (BSS) is defined as the distance between two neighboring exposure lines and can be set to any value that is within the positioning accuracy of the EBL system. Depending on the designed linewidth, the exposure of a line is conducted by exposing one line (single excel or 1-excel) or *n* adjacent lines (*n*-excel lines). These different writing strategies are illustrated in Figure 3.4. In general, the smaller the beam diameter used, the narrower the resulting line can become (see Figure 3.4a). However, if the BSS is, for example, equal to twice the beam size (BS), the line obtained after developing will most likely not be continuous (see Figure 3.4b. In Figure 3.4c, an example of a line with two excel is shown for which the BSS is equal to half the BS; the proximity exposure causes broadening of the linewidth (the red circles). Nevertheless, to get the thinnest possible lines, single pixel lines can be written, where the line width is equal to the beam size (see Figure 3.4a and d). Of course, the exposure dose significantly affects the linewidth, too high dose will unnecessarily broaden the pattern while insufficient exposure will create a discontinuous pattern. a dose test is needed to determine the optimum dose for a particular line width. It should be noted that, when approaching single-digit nm patterning by EBL, there are numerous effects outside of the control of the operator that makes it impossible to obtain universally valid values. Individual tests with the actual resist and similar samples on the same EBL system are without an alternative. In a summary, the beam step size should be carefully chosen according to the beam diameter (beam current) and the size of the structure.

3.2.3 Writing Direction

In the previous sections, I discussed the effect of the beam size, beam step size and writing strategy (choosing BBS according to BS and structure) on the EBL writing process. In this section, I would like to point out to the importance of the writing direction on the resolution of the final pattern. As depicted in Figure 3.5, the scanning direction differs from one shape to another according to the design. According to the ELS-7500 operation manual, the scanning direction for irregular shapes (not rectangle shaped) is always performed in the x-direction. However, for example, if the structure is a vertical rectangle the scanning will be carried out in Y-direction, and if it is a horizontal rectangle,

the scanning will be performed in the X-direction. Grigorescu et al.[102] Reported about the overexposure at the side of patterns that is attributed to the longer dwell time of the beam when moving from exposure line to exposure line. Therefore, if the highest resolution in Y-direction is needed, the structure should be design to be scanned in the X-direction and vice versa (see Figure 3.6).

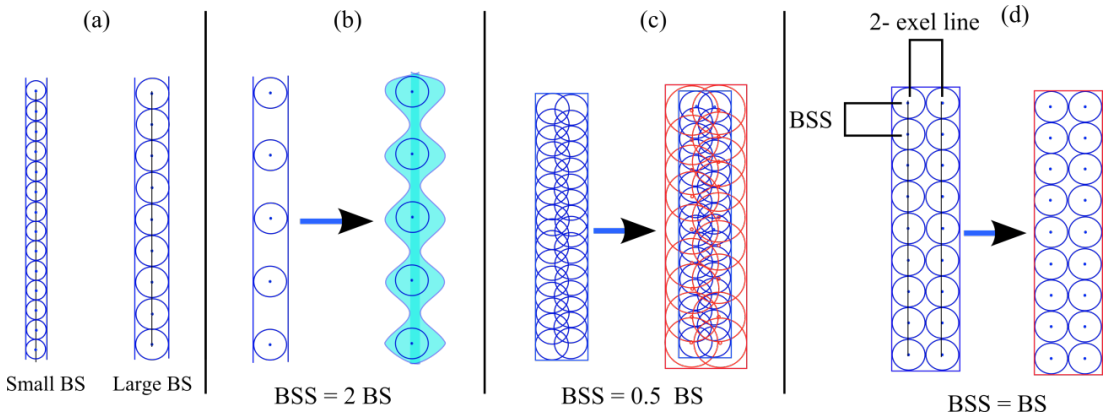


Figure 3.4. Schematic representation of the possible writing strategies: (a) single excel, single pass: designed linewidth = BSS, and (b) BSS = 2 X BS (c) BSS = 0.5 X BS and (d) n excel, single pass: designed linewidth = nxBSS, n=2 and BSS = BS

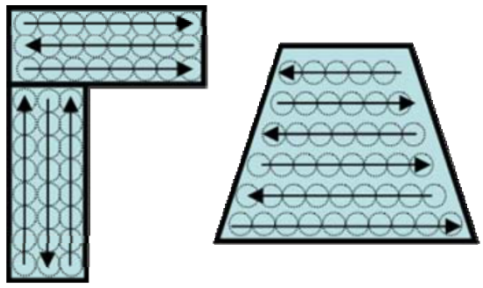


Figure 3.5. Scanning direction at different shapes

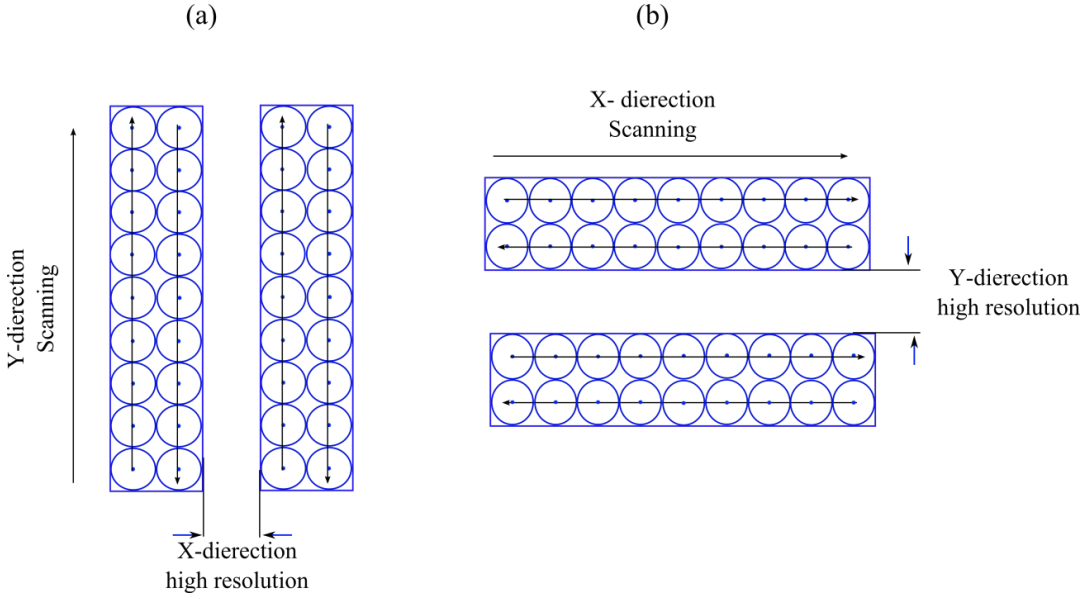
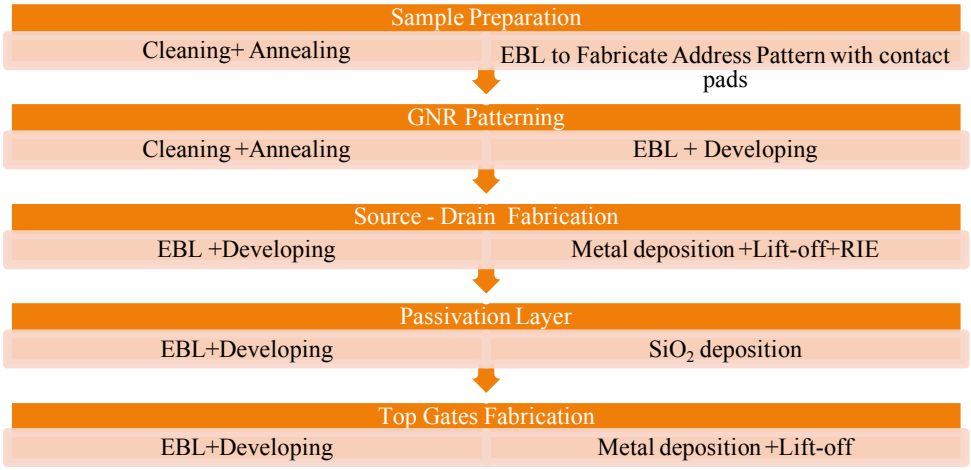


Figure 3.6. Writing direction for higher resolution (a) Y-direction scanning for X-direction higher resolution. (b) X-direction scanning for Y-direction higher resolution

3.3 Devices Fabrication

In the previous section, I showed the importance of EBL writing strategy (choosing lowest beam diameter, matching beam step size with beam diameter, decreasing the resist thickness, using higher acceleration voltage and choose the writing direction) to increase the resolution. These parameters must be taken into consideration during designing and fabricating the device. As shown below, in each fabrication step EBL is involved. In one, a complete run of the device fabrication EBL used five times and e-beam evaporation three times. The challenge here is to keep very accurate alignment for each EBL-lift-off step. Otherwise, the fabrication will fail. Here in this section, I will explain the details of each fabrication step. The following hierarchy explains the major steps of our device fabrication



3.3.1 Sample Preparation

In this work, chemical vapor deposition (CVD) - grown Graphene on copper (Cu) is used. The samples were received from Graphene Platform Co., Ltd. Single layer of CVD graphene transferred on SiO_2/Si substrate where the SiO_2 is thermally grown with thickness 100 nm on top of highly N- doped silicon with resistivity < 50 Ω.cm.

Graphene is very sensitive to impurities and contaminants; therefore, the cleanliness of graphene is vital when studying its intrinsic properties. Due to the polymer residue after the transfer process, cleaning the sample is necessary and critical. Therefore, the sample kept in hot Acetone (60°C) for 30 min before rinsing in IPA for additional 2 min. Then the sample annealed in the infrared furnace (ULVAC VHC-P610CP) for 3 hrs at 250°C in (Ar+H_2) atmosphere. Figure 3.7 shows Raman spectrum of one of the received samples (before cleaning). Address pattern (5.91X6.5) mm^2 with registration marks and contact pads fabricated by one EBL step on top of (10X10-mm^2) CVD sample.

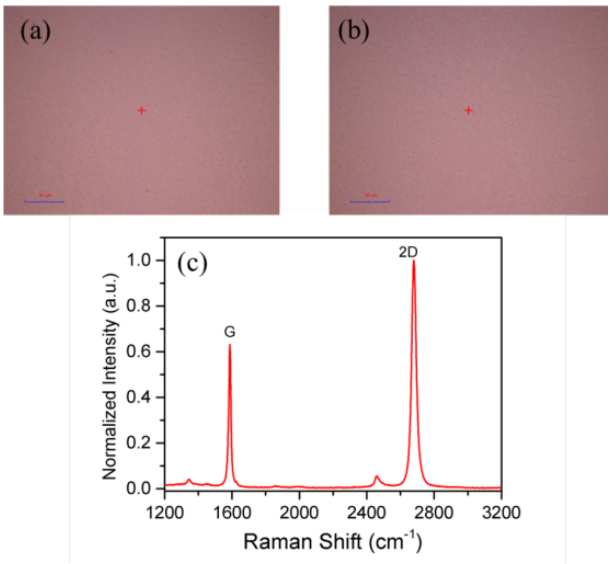


Figure 3.7. (a) and (b) images of CVD graphene sample from Graphene Platform. (c) A Raman spectrum of our CVD samples.

Usually, a positive bilayer resists used to coat the sample. This bilayer resists consists of Methyl Methacrylate (MMA)/Poly Methyl Methacrylate (PMMA 495K). MMA resists (spin-coated at 2000 rpm), and PMMA resists (spin-coated at 4000 rpm) were baked for 300 seconds at 180°C directly after spin coating. It is important to mention that MMA is more sensitive to the e-beam than PMMA. Sensitivity measured by the minimum e-beam dose required to achieve clear cut after developing step (see Figure 3.8 step 2). Higher sensitivity means lower dose required for clear cut and vice versa. Usually, for MMA/PMMA bilayer a base e-beam dose of 210 $\mu C/cm^2$ used.The benefit of using bilayer resist (high sensitivity layer + lower sensitivity layer) is the realization of an undercut after developing step in the profile of the resist layer (Figure 3.8 step 2 and 3). Realization of the undercut significantly enriches the lift-off process (see Figure 3.9). The e-beam exposure was performed using Elionix ELS-7500 EBL system operating at an acceleration voltage of 50 keV. The exposed sample was rinsed (developed) in 1:1 MIBK: IPA mixture (Methyl isobutyl ketone (MIBK):2-Iso-Proponal (IPA)) for 51 secs, then immediately rinsed in IPA for 30 seconds. Before metallization, the sample was placed in a Reactive Ion Etch (RIE) chamber to etch the CVD graphene. This step makes it possible to have the metal in direct contact with the SiO2. Otherwise, if graphene is between the SiO2 and metal, peeling occurs during consecutive fabrication steps. The uncovered Graphene layer was etched in O_2 (10 sccm) using an RF power of 30 W for 10 sec and at a pressure of 4 Pa. Then, e-beam evaporation system (ULVAC MUE-ECO-EB) was used to deposit Cr/Au (10 nm/70 nm) at a base pressure of 1×10^{-3} Pa. the rate

of deposition is 1 Å/second and 2.5 Å/second for Chromium and gold, respectively. Then lift-off was carried out in Acetone at 60°C (sample kept in hot Acetone for at least 40 min) followed by a rinse in IPA. I have found that the commonly used N-Methyl-2-Pyrrolidone (NMP) cannot be used for lift-off with CVD samples used, as it caused large-area peeling and folding as seen in Figure 3.10 a and b. This step was very important to guarantee mark detection with high accuracy for next EBL steps.

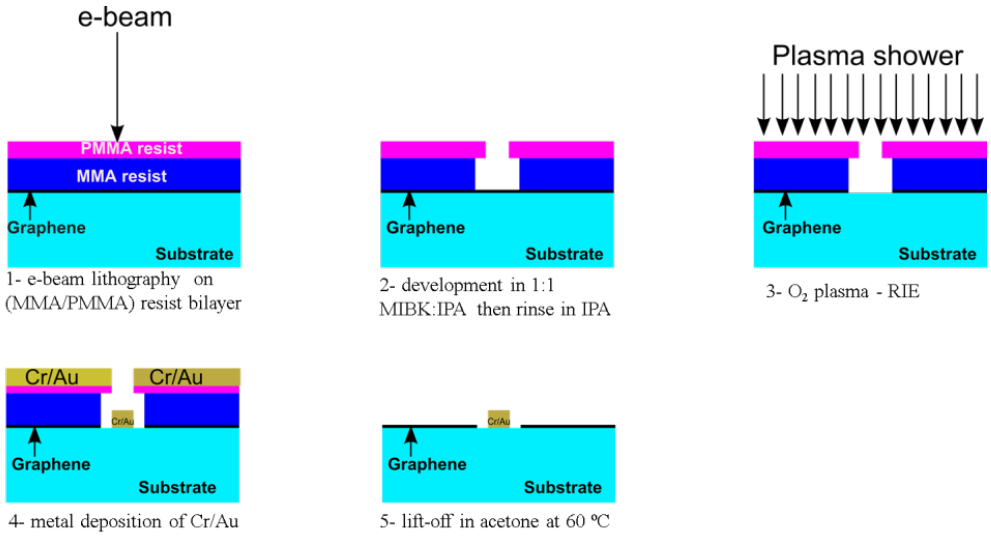


Figure 3.8. Schematic illustration of the EBL-lift-off technique for metal deposition

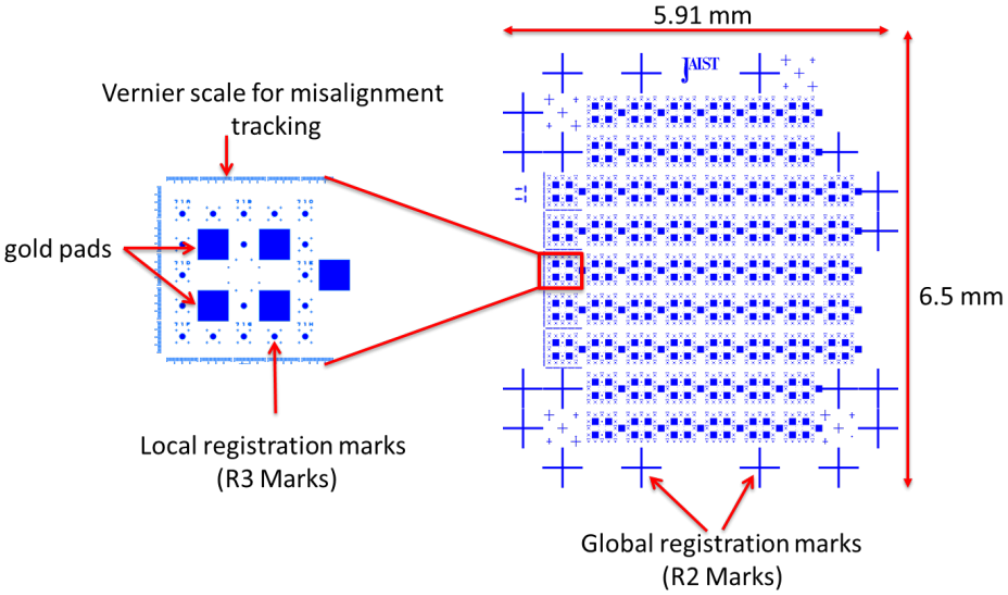


Figure 3.9. (Right) Address pattern design and layout. (left) the chip layout with Vernier scale for misalignment tracking and gold pads.

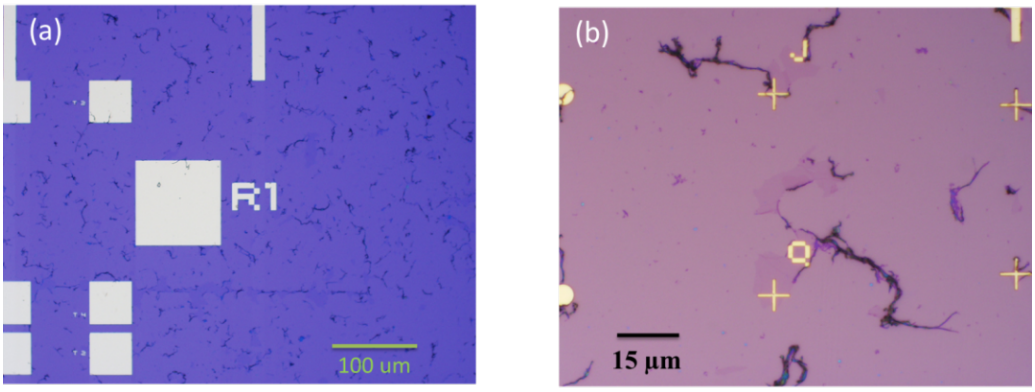


Figure 3.10. (a,b) Optical microscope images illustrate the effect of NMP on our CVD graphene. Graphene peeled and folded during lift-off in NMP.

3.3.2 GNR Patterning by e-beam lithography

After the address pattern fabrication, the GNRs are formed. In this section, I will clarify the CVD graphene was patterned with the required dimensions using EBL and RIE etch. High-resolution Hydrogen silsesquioxane HSQ, negative tone resist (remains on the substrate after exposure and developing), used to pattern our GNR. HSQ is produced by DOW CORNING(R)- XR-1541-002 in MIBK. Figure 3.11 Shows the chemical structure of HSQ. Since the thickness of the resist is critical for EBL in general, as mentioned before and even more so for this high resolution, patterning generated a thickness as a function of RPM curve. Cleaned Si substrates were coated by HSQ at different RPM values (from 2000 to 5000 RPM). Consecutively, the samples were baked for 2 minutes at 150ºC. Ellipsometry determines the thickness of the HSQ layer; I repeated the test two times, and then I take the average thickness (see Figure 3.12).

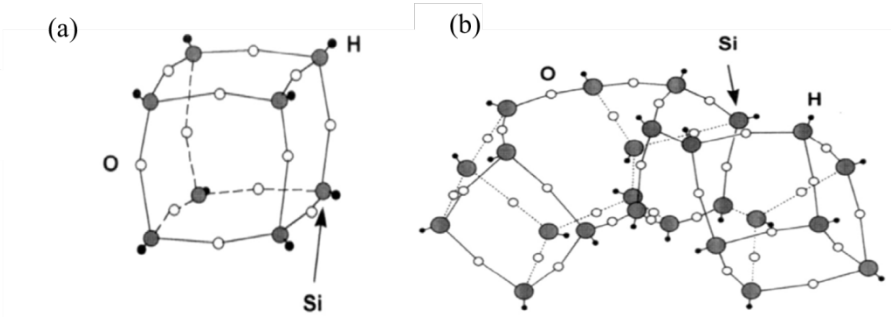


Figure 3.11. Schematic illustration of the molecular structure of HSQ: (a) cage structure for an eight-corner oligomer; (b) random structure of the resist solution. Reproduced from [102]

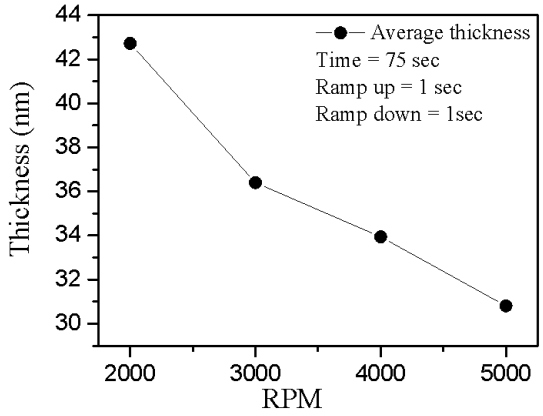


Figure 3.12. HSQ layer thickness determined at different RPM by Ellipsometry.

Before fabrication Dose test is performed to determine the optimal dose for each GNR dimensions. Following are the GNR fabrications steps:

- Hydrogen-Argon ($Ar+H_2$) Annealing: before GNR patterning the sample annealed in the infrared furnace for 3 hrs at 250°C with a gas ($Ar+H_2$) flow rate of 1L/min.

- HSQ coating: directly after annealing the sample is coated with HSQ to avoid any moisture adsorption on the graphene. HSQ is spun at 5000 rpm (closed lid), resulting in a thickness of around 32 nm (compare Figure 3.12). According to Grigorescu et al.[102] closing the lid of the spin coater decreases the thickness of the HSQ due to the slow evaporation of the solvent. After that, the sample pre-baked at 90ºC for 40 min to increase the contrast [102].

- EBL exposure and development: To achieve the highest resolution the minimum beam current is used to decrease the e-beam diameter (see Figure 3.4d). Usually, the local registration marks (R3) are used which give < 100 nm position accuracy. However, this process is time-consuming, and HSQ is very sensitive to the time between coating and exposure. Therefore, I decided not to use R3 registration to decrease the change in sensitivity between the first exposed chip and the last one. Since I did not use R3 registration, I get up to ≈ 0.5 μm misalignment to the initially fabricated alignment structure. To compensate for this misalignment, I used a Vernier scale to determine the X and Y misalignment for later compensation. After e-beam exposure, the sample immersed in MF319 (TMAH

2.2%) for 70 secs to develop the HSQ resist, followed by gentle rinsing in flowing water for additional 30 sec.

By accident, I discovered that the HSQ mask is not hard enough and can be bent or even broken during spin coat the resist for the next step. Figure 3.14 shows SEM images of the HSQ mask, after RIE, without baking after coating the sample with SML resist (spun at 5000 rpm for 20 sec) then stripped by Acetone. As shown in Figure 3.14 (a-d) some of the HSQ lines are bent, and others are unfolded or even broken. The resolve this issue it was found that a sample bake (5 min at 250ºC) is sufficient to harden the HSQ mask so it can withstand the next fabrication steps.

3.3.3 Source – Drain Fabrication

After patterning the HSQ hard mask, to contact the GNR, the source–drain electrodes were fabricated by using conventional EBL-lift off technique. A bilayer resist layer of (MMA/PMMA) was used (I used the same recipe mentioned in3.3.1 for EBL exposure and development process). Deposition of metal was done by evaporating Cr/Au with 5/35 nm respectively (for more details see section 3.3.1). Then, lift-off was carried out in hot Acetone (sample kept in hot Acetone for at least 40 min at 60°C) followed by a rinse in IPA (see Figure 3.15). Then the graphene uncovered layer was dry etched in O_2 (10 sccm) using an RF power of 30 W for 10 secs and at a pressure of 4 Pa.

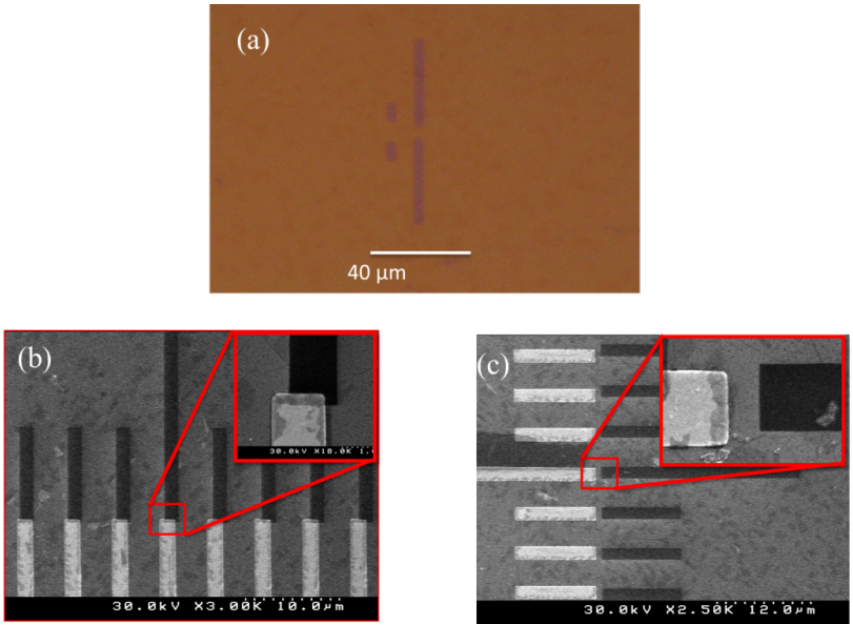


Figure 3.13. (a) HSQ hard mask on top of the CVD single layer graphene. (b,c) SEM images of Vernier scale used to determine the shift in X-direction (b) and Y-direction (c).

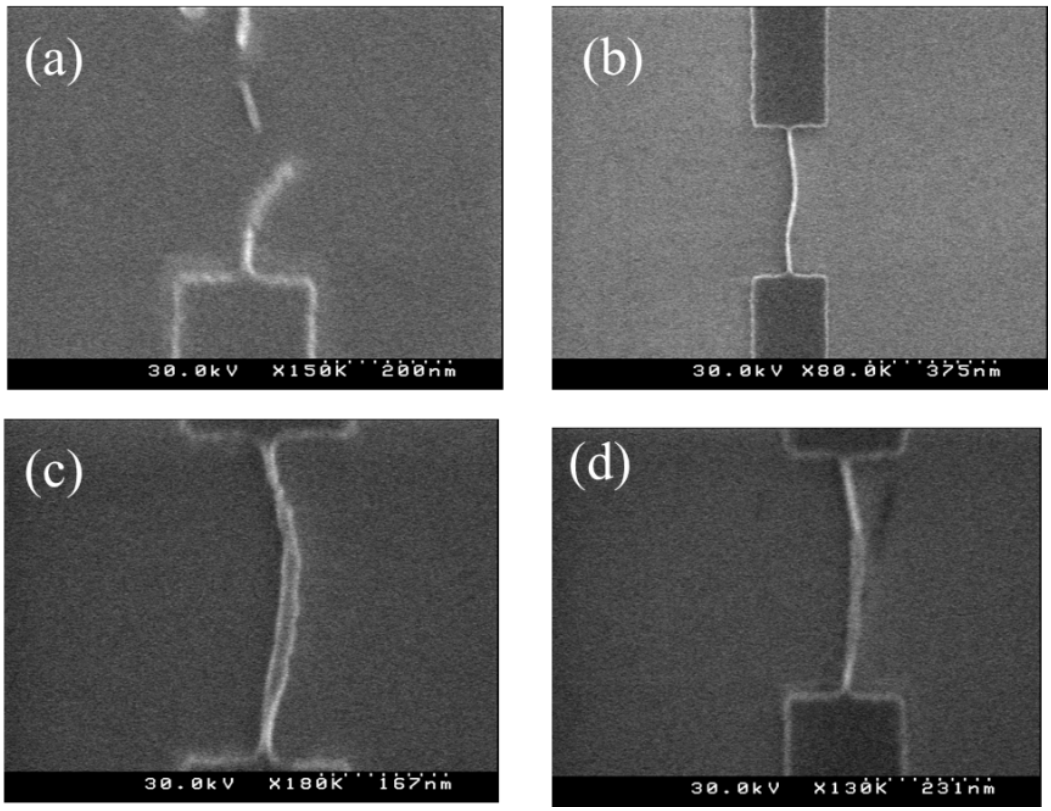


Figure 3.14. HSQ mask without baking after coating the sample with SML resist (spun at 5000 rpm for 20 sec) and then stripped Acetone.

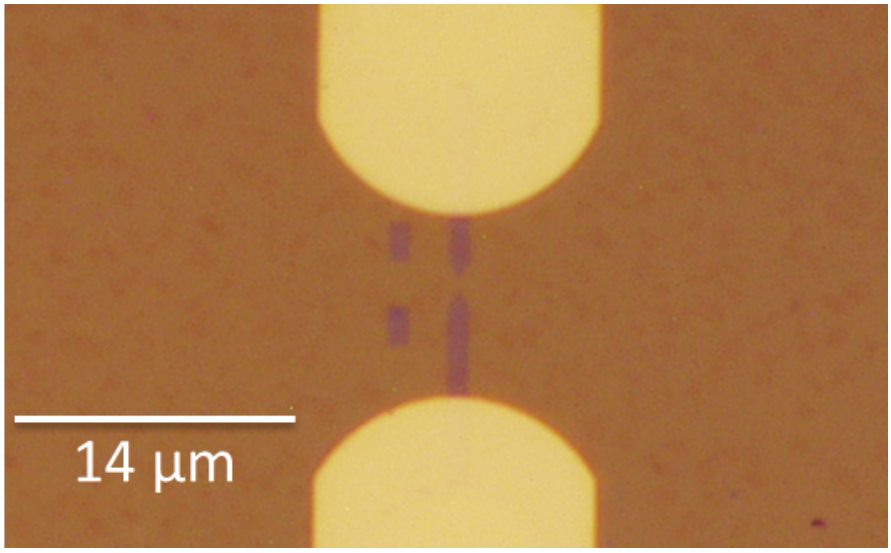


Figure 3.15. Optical microscope image of the Source – Drain contacts after lift-off, the total thickness of Cr/Au is 35 nm. It is evident that the GNR is shifted up in the Y-direction.

3.3.4 Passivation layer

The purpose of adding a dielectric layer above the hardened HSQ is to decrease (top gate to channel) leakage current. E-beam evaporation of SiO_2 with consecutive lift-off is used to pattern this film. I intentionally designed the passivation layer, so it does not only cover the GNR but partially the source and drain contacts as well. I did that to ensure that the top gate electrodes do not form a short circuit with the source or drain contacts in case

of misalignment. For EBL (I used the same recipe mentioned in3.3.1) Figure 3.16 shows the passivation layer of one of our devices. The 10 nm SiO_2 layer was evaporated with a deposition rate of 0.5 Å/sec. SiO2 lift-off is achieved in Acetone.

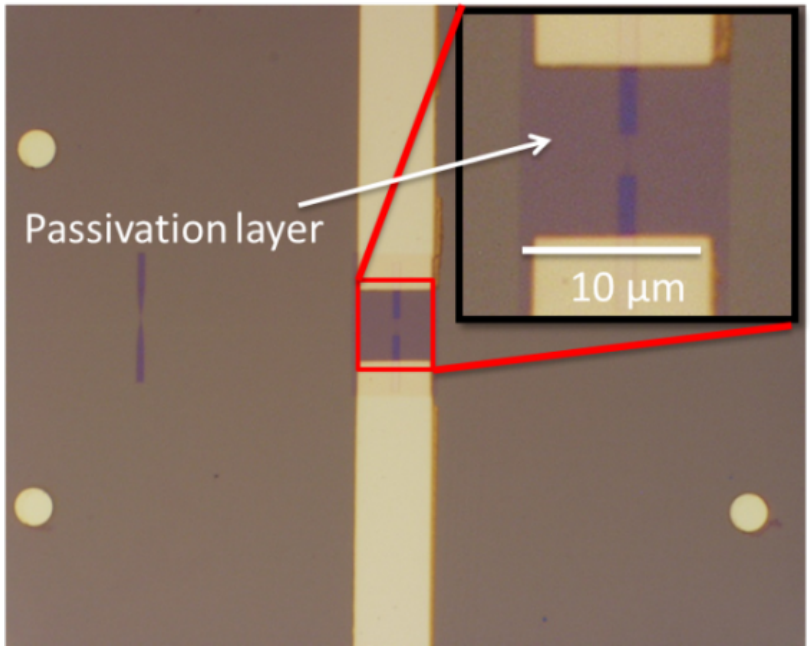


Figure 3.16. Optical microscope image illustrates the passivation layer in one of our devices. 10 nm SiO2 thermally evaporated on top of the GNR to decrease the leakage current.

3.3.5 Top Gate Fabrications

The fabrication of top gates is very challenging as the requirements for the gap between the top gates is very strict. First, I fabricated two top gate devices to realize and study the GRN *p-n* junction. Then I fabricated a triple-gate device to realize GNR-TFET operation. From the point of fabrication, both types have the same fabrication procedures, since I used the same resist (SML) to fabricate the top gates. Before using SML, I did dose test and resolution test as well, to know the optimum dose and the minimum feature that can be achieved. As will be shown later, the design of the top gates consists of several separated horizontal rectangles to decrease the effect of the backscattered electrons, which can introduce parasitic dose to the unexposed area. In this section, I will show the design layout of two and triple-gate devices.

EBL-lift off technique used to fabricate the two top gates on top of the GNR. A single layer of SML resist is spun on the sample (5000 rpm for 20 sec), resulting in a final thickness of around 100 nm. The SML resist is pre-baked at 180ºC for 2min, and E-beam espouse with a dose of 400 µC/cm2 is performed. Consecutively, the sample is developed in (MIBK: IPA, 1:3) for 30 sec and rinsed in IPA for additional 20 sec. Immediately after developing the sample loaded into the e-beam evaporation system. Cr/Au with a thickness

of 2 and 10 nm, respectively, is deposited lift off is done using hot Acetone (60ºC). From our experiments, it has shown that the SML resist is very sensitive to humidity. Very narrow gaps may disappear if the sample kept for a long time (~ 6 hrs) in the air after developing. Figure 3.17(a) shows the layout of the two-top gate device and the magnified view that each top gate is divided into two parallel rectangles. Figure 3.17(b) shows a SEM image of the device after fabrication has been completed. The separation gap of that device ≈ 55 nm and the GNR width is ≈ 22 nm.

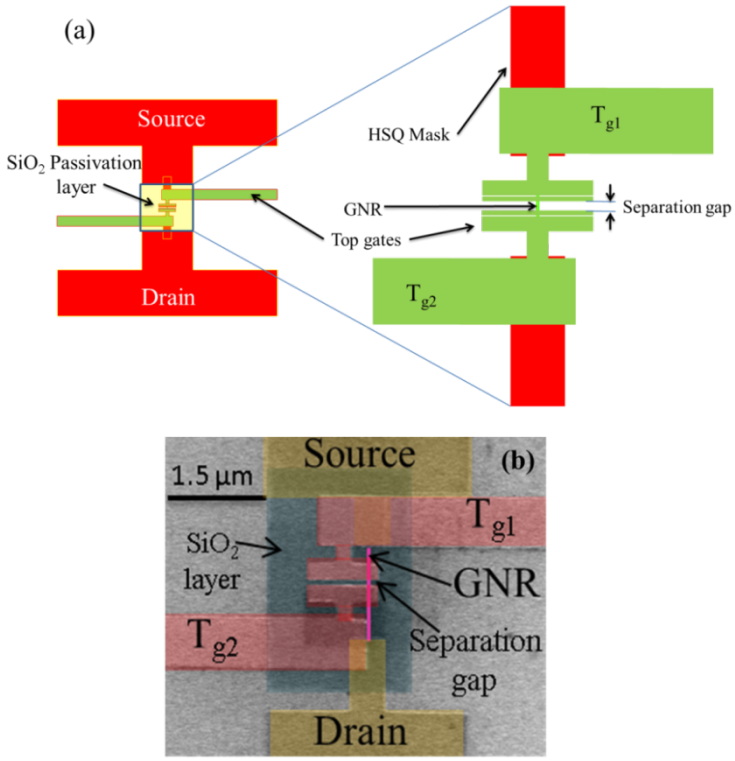


Figure 3.17. Two top gates structure (a) layout of the two top gates structure. The magnified view illustrates that the inner part of the top gates is divided into two parallel rectangles to increase the resolution in Y-direction. (b) SEM image of the two top gates device after fabrication by using SML resist.

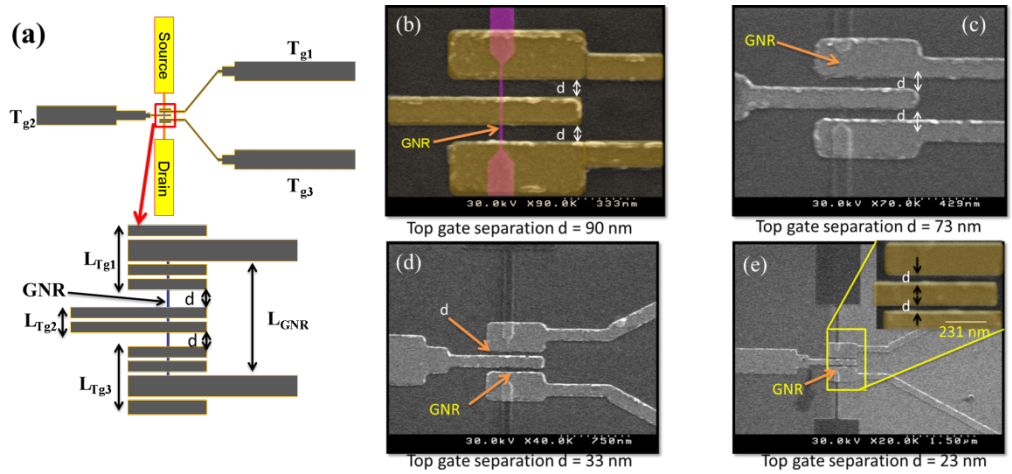


Figure 3.18.(a) the layout of the triple-gate device (b-e)) SEM images of the triple-gate device after fabrication by using SML resist. Image (e) illustrates the 23 nm gap which achieved by SML for EBL.

3.4 Summary

At the end of this chapter, I like to show the most important achievement that helped me to realize a working GNR-TFET. Improving the EBL system writing strategy is the most important and useful experience. Consequently, I acheived ~ 15 nm HSQ line. Moreover, in case of the positive resist (SML), I could reach 23 nm separation gap between the top gates. Finally, repeatedly, I achieved alignment accuracy ranging from 50 nm to 100 nm, which make the yield of the working devices larger than 75 %.

4 Sharp switching behavior in GNR *p-n* junction

The experimental study of interband quantum mechanical tunneling in graphene nanoribbons is a major step to realizing graphene tunneling-based field effect transistors (TFET). Here, I report the sharp switching behavior observed in an electrostatically controlled graphene nanoribbon p-n junction in pn and np biasing. Current modulation with a slope of 42 mV/dec over five orders of magnitude in drain current is demonstrated at 5 K. This slope is unaffected by temperature up to 50 K. The suppression of carrier transmission in the OFF state is attributed to the finite bandgap of the ~15 nm wide graphene nanoribbon channel. The reported device characteristics can be explained by band-to-band tunneling through the junction. This work is expected to offer valuable insight into BTBT in GNRs and be a valuable contribution towards competitive graphene TFETs.

4.1 Introduction

Graphene-based *p-n* junction have been studied by several groups[50]–[52], [97]–[100], [103]. In these previous reports, graphene *p-n* junctions are formed in wide graphene ribbons (zero energy gap graphene) by coupling the top and back gate to get all possible configurations of the *p-n* junction (*p-n-p* or *n-p-n*). Due to the absence of energy gap, it is impossible to confine the carriers in wide GNRs (> 100 nm) devices electrostatically. The transparency of the potential barrier between the *p*-doped and *n*-doped regions attributed to the so-called Klein tunneling (perfect transmission of the charge carriers with normal incidence onto a potential barrier) phenomenon. However, when Graphene is patterned into a narrow ribbon, and the carriers become limited to a quasi-one-dimensional (1D) system, a band gap can be opened [67]. In the current work, our GNR width is ~ 15-nm (Figure 4.1b) with an estimated E_g in the order of 44 meV. The GNR used here has been fabricated from single layer CVD graphene supported by a SiO_2/Si substrate. Two independent top gates, with separation of 40 nm, are used to define

the GNR *p-n* junction under investigation (see the device structure in Figure 4.1a). It is important to point out to the misalignment between the top gate and the GNR ($\Delta X \approx 400$ nm) as shown in Figure 4.1(b). This misalignment has a nontrivial effect on the electronic transport through the device, as I will discuss later in this chapter. To investigate the effectiveness of the electrostatic doping and the reliability of our GNR *p-n* junction, I studied the electronic transport in a wide range of temperatures (5 to 300 K).

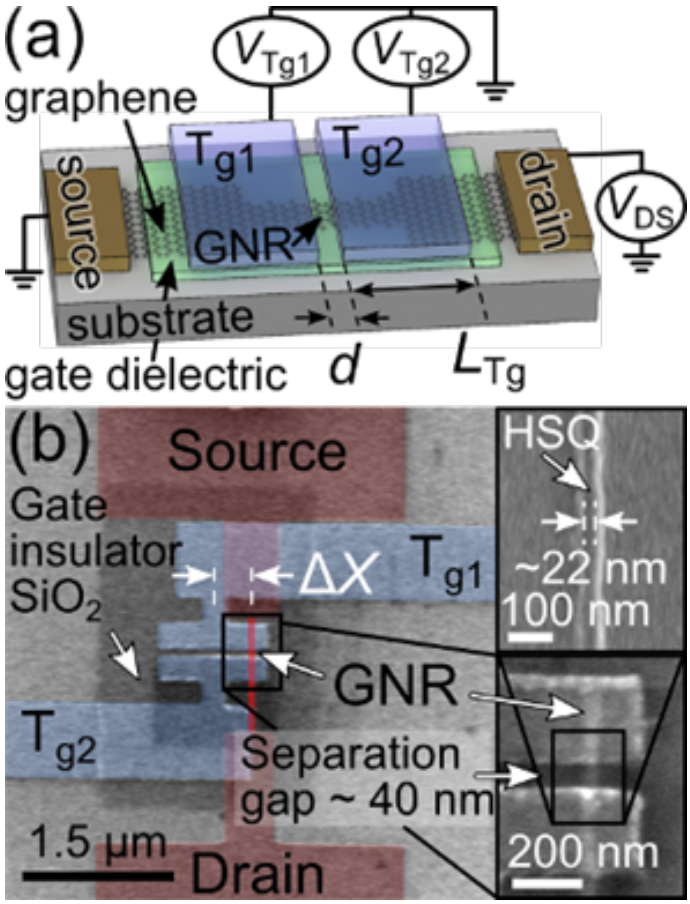


Figure 4.1. (a) The two-top gate device and dimensions (b) SEM image of the 22 nm GNR width. (c) SEM image of the two top gate device structures. Fake colors are applied for better understanding.

4.2 Energy gap opening

Energy gap opening can be directly measured from the characteristics of the back gate at low temperature[67]. As presented in Figure 4.2 (a), the drain current experience a strong suppression (transport gap) near the DNP at 4.8 K, which implies the opening of a bandgap. Inside the transport gap, a weak oscillation is observed which is attributed to the formation of multiple quantum dots due to the edge roughness [67]. As shown in the inset of Figure 4.2 (a) the drain current experience Coulomb blockade effect which substantiates the band gap opening. The bandgap of 44 meV is extracted from the Arrhenius plot of the minimum conductance as a function of the inverse of absolute

temperature[47]. From the empirical equation; W = $(\hbar\, v_f)/E_g$ ($\hbar$ is the reduced Plank constant, W is the GNR width and v_f = 10^6 m/s is the Fermi velocity)[101], estimated to be 15-nm for E_g = 44 meV.

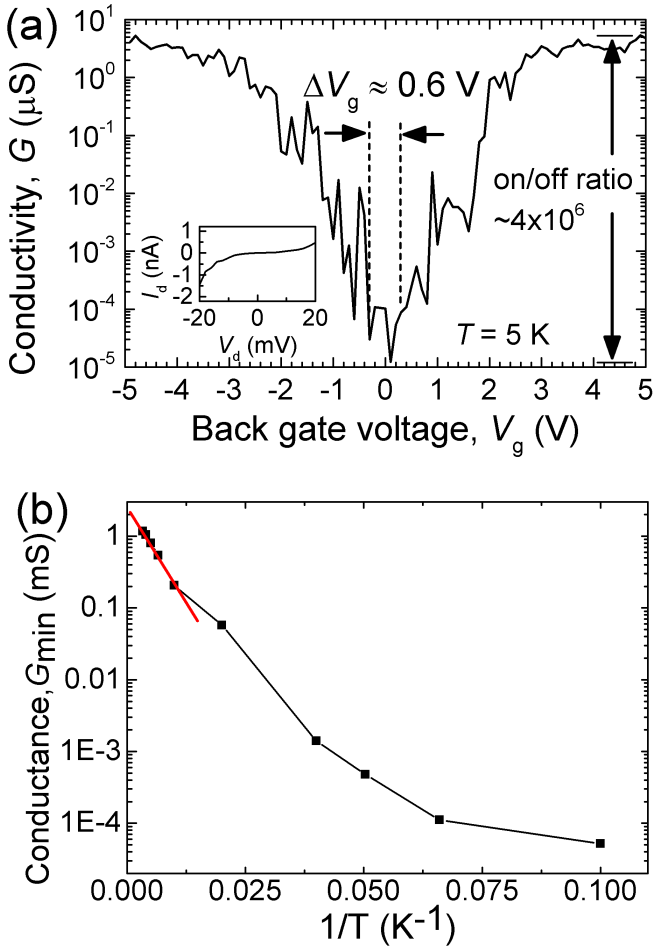


Figure 4.2. (a) back gate characteristic at 4.8 K shows a transport gap with $\Delta V_{bg} \approx 4$ V. (b) Arrhenius plot of the minimum conductance as a function of (1/T)

4.3 Individual gate characteristics

A semiconductor characterization system (KEITHLEY 4200-SCS) was used to do all the electrical measurements. All measurements were performed under vacuum in a variable temperature helium closed cycle cryocooler system. The base temperature of the cycle cryocooler system is T ≈ 4.8 K. First, I measured the drain current (I_d) as a function of drain voltage (V_d). To confirm the functionality of each gate and the performance of the GNR, the I_d measured as a function of gate voltage (V_{Tg}) at constant V_d. The room temperature measurement shown in Figure 4.3a demonstrates the ohmic behavior of the metal-graphene contact. From the back-gate modulation, it is obvious that the charge neutrality point (CNP) shifts to the left side (slight P-doping). Also from the top gates

modulation, one can notice the same shift in the CNP as well. In general, all the gates show good I_d modulation (see Figure 4.3b)

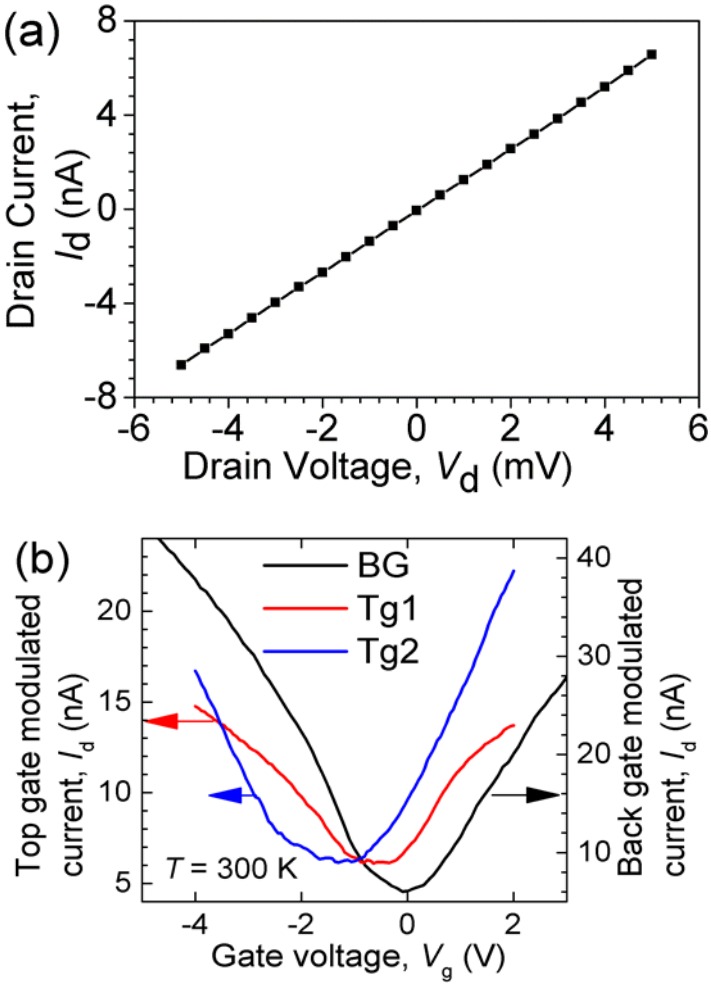


Figure 4.3. (a) I_d-V_d at 300 K. (b) Back gate (bg) modulation.

4.4 Realization of GNR *p-n* junction

To achieve all the possible coping combinations of the device, one of the top gate voltages (V_{Tg1} and V_{Tg2}) is swept from - 4V to 4V (-5V to 5V at low temperature) with the other top gate voltage stepped in the same range. V_d is fixed at 3 mV for all measurements at 25 K and above, and 12 mV below due to the high current suppression at lower temperatures. The contour plot of I_d as a function of both top gate voltages illustrates the key features of our device (see Figure 4.4). First, four distinct regions belonging to the four possible configurations (*pn, np, pp, and nn*) are clearly visible. Note that, the doping configuration is indicated by two letters (such as np), where the first letter denotes the doping below T_{g1} (positive voltage for n-doping, a negative voltage for p-doping), and the second letter denotes the doping below T_{g2}. Secondly, the low current region is slightly slanted, which means that there is a weak capacitive interaction between

the two top gates. Therefore, GNR *p-n* junction successfully realized. As depicted in Figure 4.4, the low current region due to Tg2 modulation is wider than the low current region due to Tg1 modulation. The reason behind that is the misalignment between the two top gates. Due to the misalignment, Tg1 covered a large part of the wide region of the GNR (see Figure 4.1(b)). As a result, the effective GNR width underneath Tg1 is much greater than the GNR width underneath Tg2. Moreover, the current level in the *nn* and *pp* configuration is much higher than the *np* or *pn* mode, which reflects the higher resistance of the device at *np* or *pn* mode due to the introduced potential barrier. In addition, quantitative information can be extracted from the contour plot, as I will show in the next section. Figure 4.5 shows the contour plot over a wide range of temperature (from 5 to 250K). as can be seen, even at high temperature the device shows 4 distinguished regions. The capacitive coupling between the gates is remarkable at high temperature (250K), however, the gates became more independent at a lower temperature. This may be ascribed to the moisture inside the chamber which is more effective at higher temperature

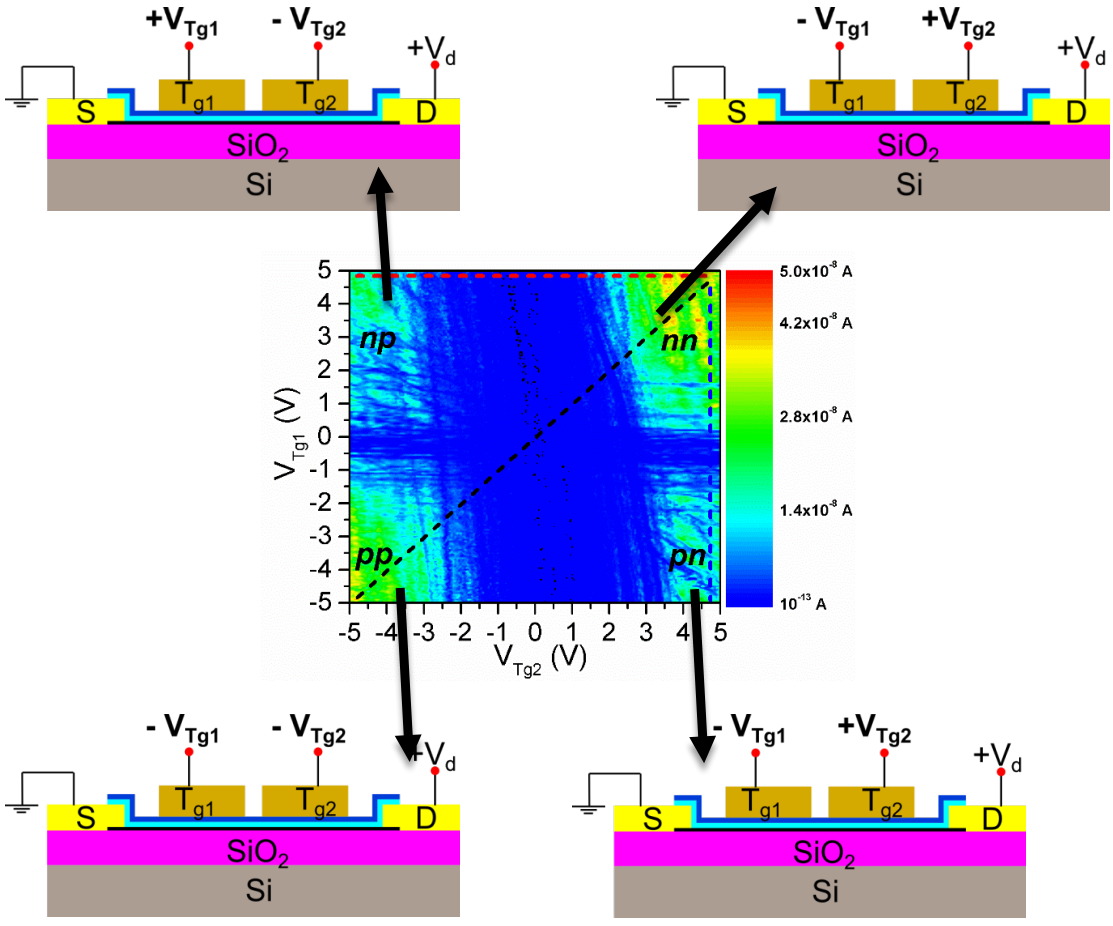


Figure 4.4. Contour plot of drain current as a function of the top gate voltages at T = 10 K. Drain voltage V_d is 12 mV. The clearly defined doping regions induced by the electrostatically doping are indicated by *np, nn, pn*, and *pp*, respectively. The three dashed lines indicate the location of the profiles in (b-d).

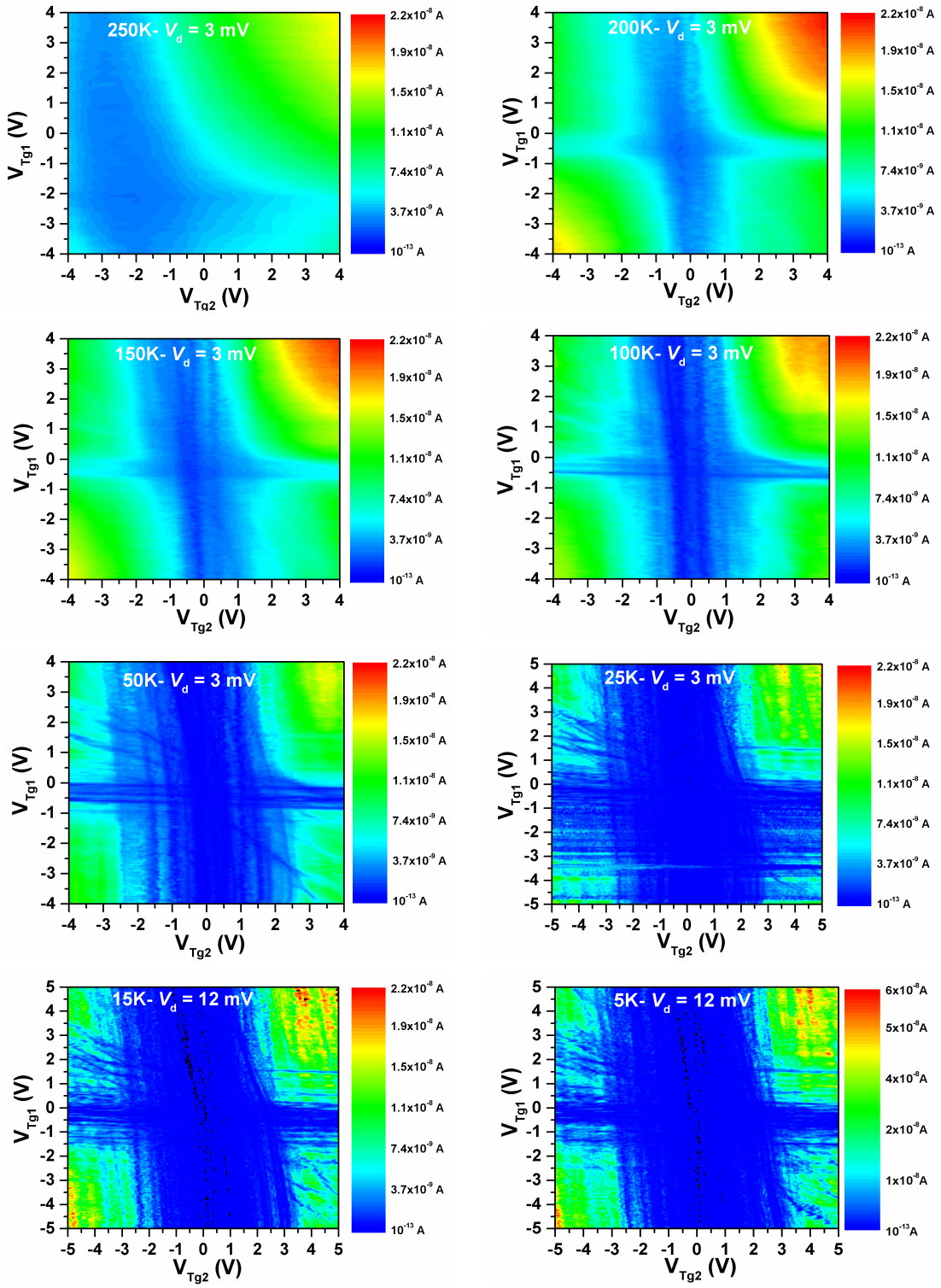


Figure 4.5. Contour plot of drain current as a function of the top gate voltages at over a wide range of temperatures from 5 to 250K. Clearly defined doping regions are observed. V_d is kept at 3 mV until 25K and increased to 12 mV at lower temperatures

4.5 Transport characteristics of GNR *p-n* junction

The drain current (I_d) at 10 K is shown for different gating configurations in Figure 4.6. When using the global back gate (Figure 4.6(a)), a symmetric modulation is observed with some random oscillation around the CNP at V_g = -0.5 V. The symmetric

modulation is consistent with the 300 K measurement shown in Figure 4.6c). When modulating by the synchronized top gates (along with the black dotted line in Figure 4.4), the symmetric characteristics are observed, as well (Figure 4.6 (b)), however, some differences exist compared to the back-gate modulation. Firstly, the ON current (V_{Tg} = +/- 5 V) is higher. As the dielectric layer between the top gates and the graphene is significantly thinner than between the substrate and graphene, the modulation at a given voltage is stronger with a higher doping level. The higher OFF current is due to the charge neutrality points (DNP) having a slight offset for the two top gates (see Figure 4.3 (b)), and the device cannot be effectively turned off for synchronized top gate voltages (i.e. while the GNR underneath one gate is completely turned off, the GNR under the other gate is still slightly ON). In contrast to these two cases, when fixing one of the top gates and sweeping the other one, a remarkable step change in the drain current is observed. For fixed V_{Tg1} = 4.9 V (Figure 4.6(c), corresponding to np biasing), the step change with a rate of ~42 mV/dec over a range five order of magnitude in drain current ($5x10^5$) is observed at $V_{Tg2} \approx$ -1 V. The OFF-state current is at least one order of magnitude lower than for the back gate modulated current. In case of a fixed V_{Tg2} = 4.9 V (Figure 4.6(d), *pn* biasing), the rate of the step change at $V_{Tg1} \approx$ -0.8 V is ~32 mV/dec but only over a range of four orders of magnitude in drain current (~$1.3x10^4$). Furthermore, the current is only very slightly affected by the V_{Tg1} outside of the suppression region.

Similar characteristics are observed at 100 K and slightly changed bias conditions, as well (compare Figure 4.7). However, two observations are made that require further elaboration. Firstly, the slope of the abrupt current change decreases with increasing temperature. Secondly, there is a clear difference between np and pn biasing, both in terms of the modulated gate voltage, but also in terms of the fixed gate voltage. For the np biasing (Figure 4.7(a)), the current is unaffected by V_{Tg1} (from 2 to 3.9 V). In clear contrast, the current is strongly affected by V_{Tg2} in the pn biasing and shows a constant current beyond the sharp switching (Figure 4.7(b)). At 10 K this effect is observable as well for the np biasing (see Figure 4.8) but strong current fluctuation and the wide transport gap due to Tg2 masks this effect for the *pn* biasing. Although the source-drain biasing direction is reversed with respect to the doping configuration for these two cases, such an asymmetry is not expected and will be discussed in the next section.

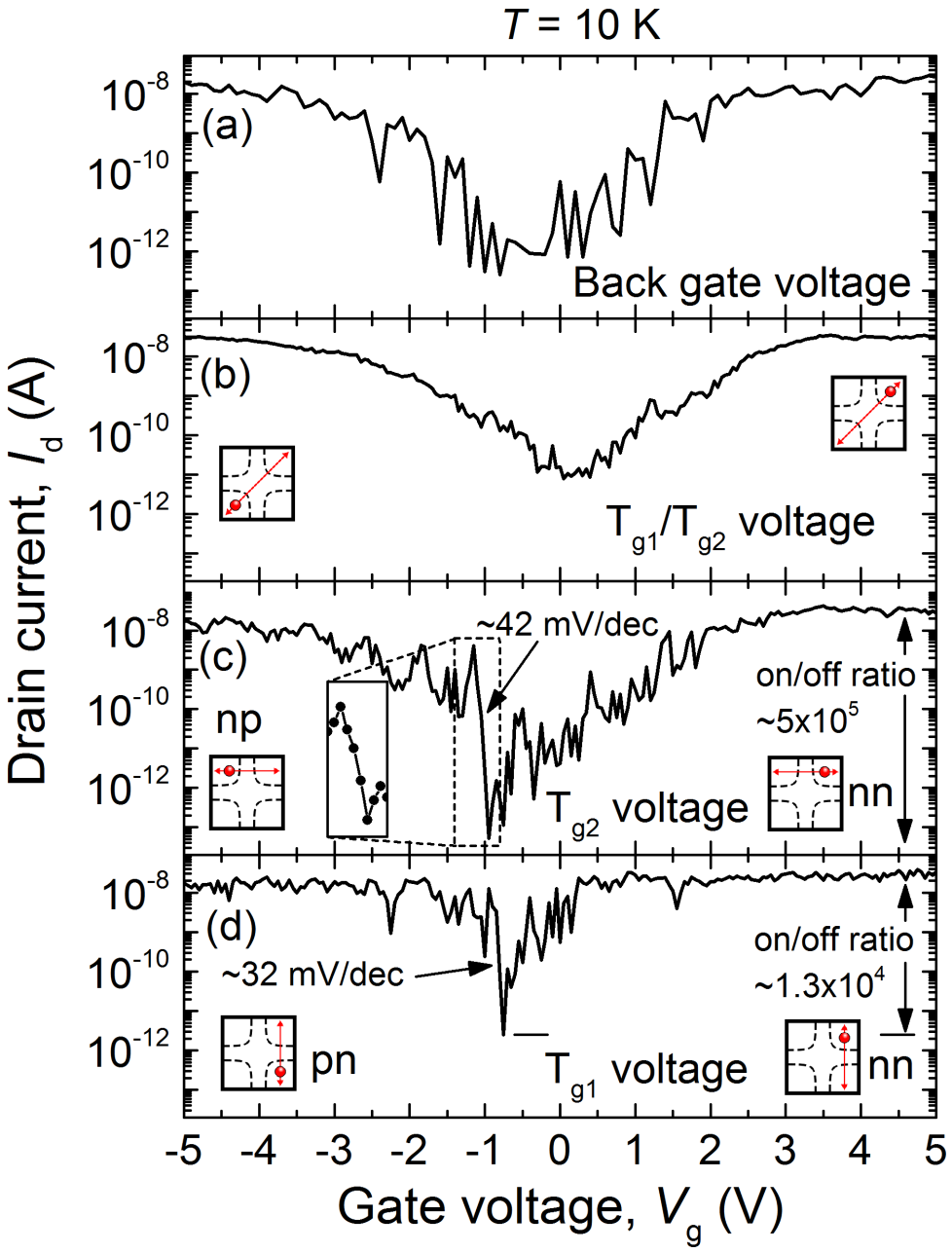


Figure 4.6. Drain current as a function of gate voltage at T = 10K and V_d = 10 mV: (a) Back gate voltage sweep. (b) Simultaneous T_{g1} and T_{g2} sweep. The GNR is modulated from nn configuration to pp configuration. (c) T_{g2} sweep at V_{Tg1} = 4.9 V. The device is switched from nn configuration to pn configuration by sweeping V_{Tg2} from 5 V to -5 V (forward biasing). Inset shows the transition region with sharp slope of 42 mV/decade over five orders of magnitude. (d) V_{Tg1} sweep at V_{Tg2} = 4.9 V (reverse biasing) showing similar characteristics with 32 mV/decade in the sharp switching region over four orders of magnitude.

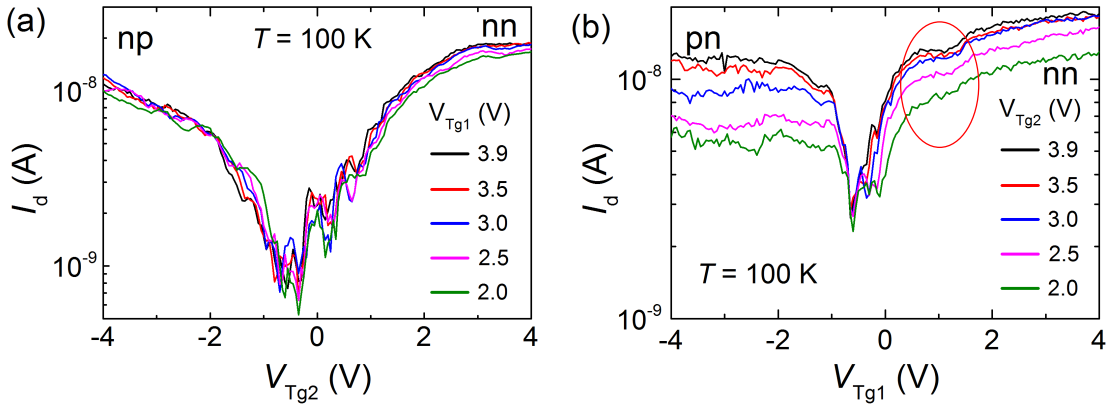


Figure 4.7. Device characteristics at 100 K for np and pn biasing conditions. (a) Drain current vs V_{Tg2} (V_d = 3 mV and variable V_{Tg1}). (b) Drain current vs V_{Tg1} (V_d = 3 mV and variable V_{Tg2}).

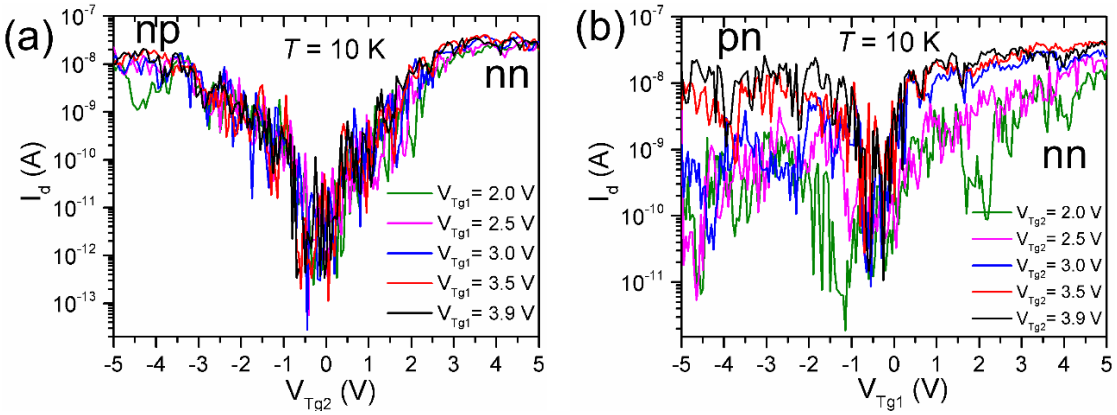


Figure 4.8. Device characteristics at 100 K for np and pn biasing conditions. (a) Drain current vs V_{Tg2} (V_d = 3 mV and variable V_{Tg1}). (b) Drain current vs V_{Tg1} (V_d = 3 mV and variable V_{Tg2}).

4.5.1 Asymmetry of forward/reverse biasing

The effect of the barrier height, which is defined as (V_{Tg1}-V_{Tg2}) (see Figure 4.9b), On the carrier transport through the device in reverse (pn configuration) and a forward (np configuration) bias is discussed next. In the case of reverse bias, the current profile was extracted at different V_{Tg2} values as shown in Figure 4.7 and Figure 4.9. The drain current saturation level increases with increasing V_{Tg2} (barrier height) as a result of the decrease of the tunnelling distance (see Figure 4.9). Furthermore, a temporary current saturation is observed at the higher potential barrier in the nn mode (red circle in Figure 4.7(b), followed by a further current increase. This current saturation may be ascribed to the strong bend of the bandgap at the higher potential barrier, which enhances the probability of the quantum mechanical tunnelling through the barrier [10]. In contrast,

for forward bias configuration (np), the current does not show any noticeable change by changing the V_{Tg1} (see Figure 4.7(a))

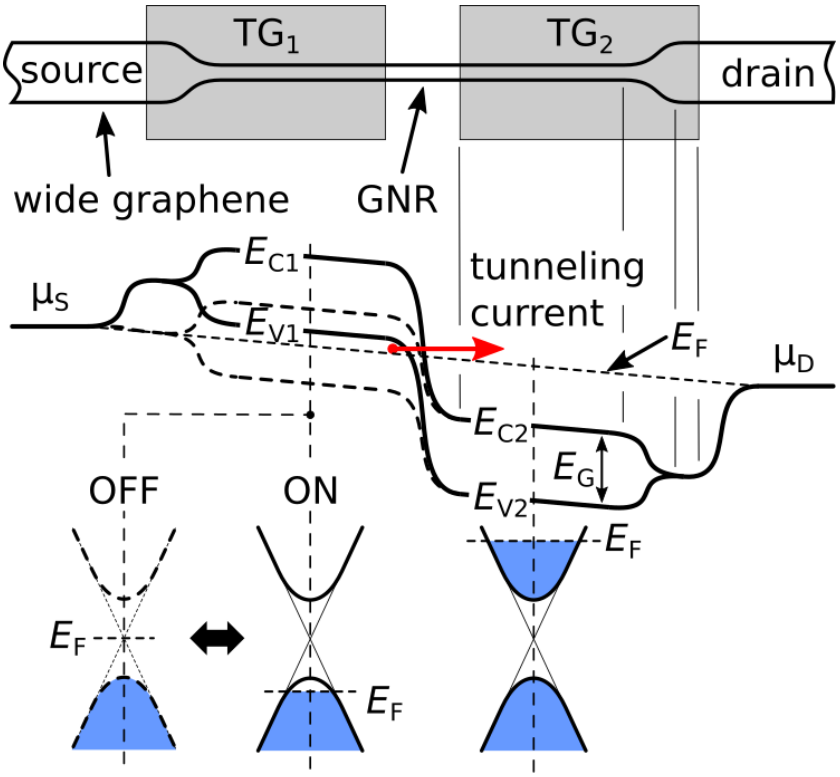


Figure 4.9. schematic diagram illustrates the interband tunnelling current in the reverse bias configuration. Solid line represents the ON-state and dotted line represent the OFF-state

The top gate modulation (I_d-V_{Tg1} and I_d-V_{Tg2}) at a different temperature having studied, to investigate the temperature dependence. Figure 4.10 (a) shows I_d-V_{Tg1} at a different temperature, in the case of reverse bias mode (pn), the carrier transport is independent of temperature. Current saturation has been observed even at high temperature (200 K), which confirms the interband tunnelling behaviour in the reverse bias. At low temperature, it can be easily noticed that a sharper slope of the current change and higher I_{ON}/I_{OFF} ratio. However, in the case of higher temperature, the thermal current contributes in the overall current so that the slope of the current change became lower. In the case of forward bias (I_d-V_{Tg2}), the current is highly dependent on the temperature, as presented in Figure 4.10 b and c. Two regimes can be recognized, low-temperature regime, and high-temperature regime. At low temperature (50 K or lower), the current experience two distinguish slopes when the junction switches from nn to np ((1) and (2) regions). By increasing the temperature, the inflection point between the two regions shifts to higher V_{Tg2} voltage and the slope decreases. At high temperatures, the second region (2) disappears from the measurement range and the current is linearly dependent on the V_{Tg2}

voltage. I do not have clear explanation for this behaviour, more investigations still needed to clarify this behaviour.

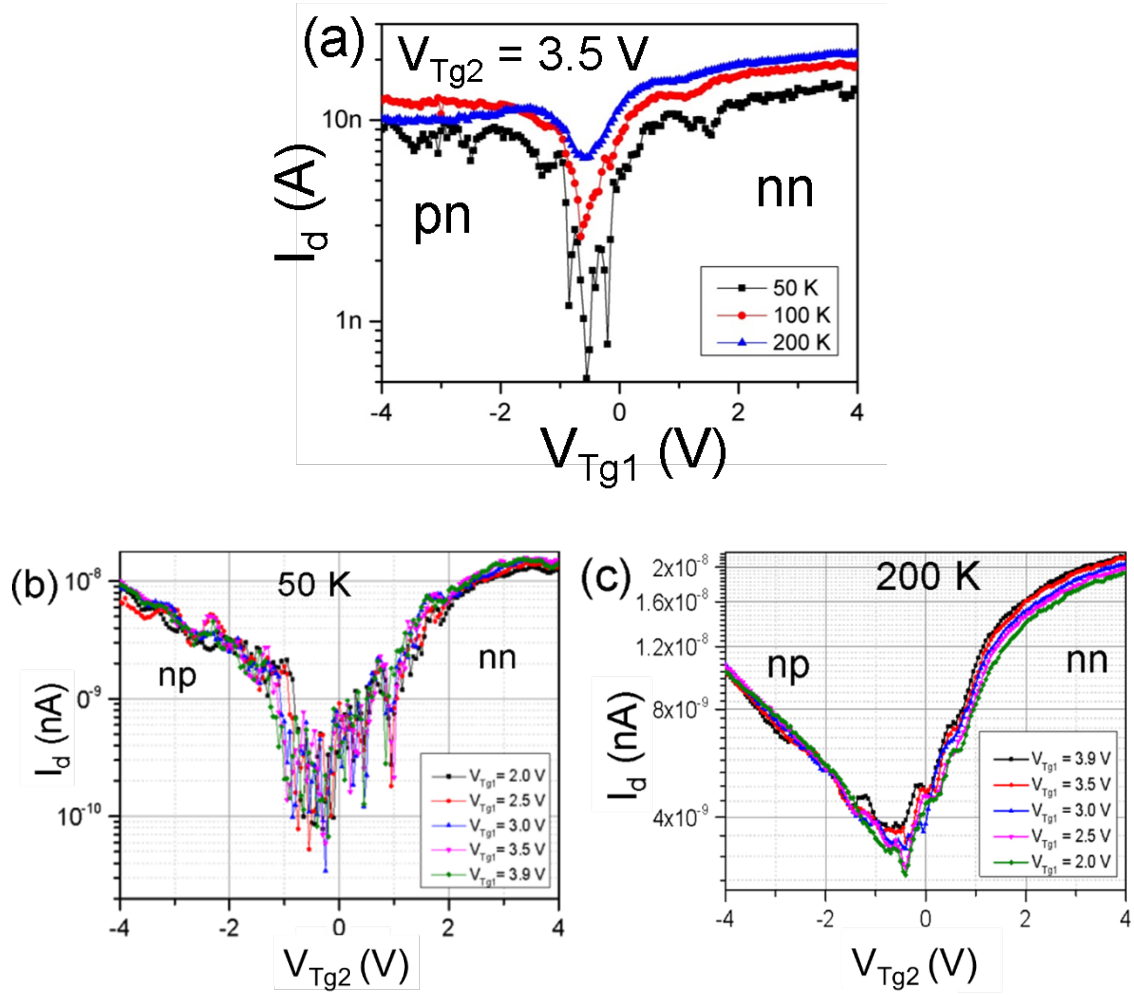


Figure 4.10. (a)I_d-V_{Tg1} at different temperatures, V_{Tg2} fixed at 3.9 V(reverse biased). (b-c) I_d –V_{Tg2} as a function of V_{Tg1} at various temperatures (forward bias). Clear inflection point appears at low temperatures. By increasing the temperature, the inflection point occurs at higher V_{Tg2} values and disappear at 200 K.

4.6 Origin of sharp switching

The sharp switching was observed in the np and pn biasing condition at low temperature (Figure 4.6(c) and (d)), when one of the gates is biased so that the valence band edge in the variable gate region is lifted into the bias window and at the same time above the conduction band edge in the fixed gate region. I can thus sketch the simplified band structure of the p-n junction as shown in Figure 4.11(a). In the uniformly nn-doped state, a large drift current is enabled. As the energy of the band edges in the T_{g2} region are shifted up, the drift current is reduced and a thermally activated leakage current dominates the transport. Finally, as the band overlap occurs, the tunnelling width W_T is abruptly reduced. As the tunnelling window is formed in the bias window (between E_{FD}

and E_{FS}), the large number of available charge carriers enables the increase of the drain current over five orders of magnitude with the sharp slope. As the tunnelling energy window is further increased (V_{Tg2} is further decreased), the sharp switching saturates because the transport through the remaining parts of the channel limit the allowed current.

4.7 Quantum confinement and Coulomb oscillation

The I_d/V_{Tg} data at low temperature shows significant peaks of comparable amplitude to the sharp switching highlighted in Figure 4.6 (c) and (d). Due to the EBL-RIE GNR formation method used in this work, the effect of edge disorder is unavoidable issue of it. The carrier transport in GNR based devices is mainly affected by the multiple quantum dots, Anderson localized states, and the disorder potential [104]–[109]. For short GNRs, the multiple quantum dots effect has a stronger effect compared to the Anderson localized states. The effect of multiple quantum dots is illustrated in Figure 4.11(b), where the band structure of a GNR with edge disorder is schematically sketched. Varying doping levels, (location of bands in respect to the Fermi level) can cause the formation of isolated quantum dots along the GNR (Figure 4.11 (b1)). Charge carriers must overcome these potential barriers between the dots, greatly influencing the current. The shape and number of the dots can change significantly with the slight change of the Fermi level (such as change of gate voltage, compare Figure 4.11(b2)), forming continuous charge puddles. At higher doping levels (higher gate voltages), this effect is strongly suppressed and the current at higher doping levels in Figure 4.6 is smooth. Also, the effect of the quantum confinement is reduced by thermal smearing, which is apparent when comparing Figure 4.6 and Figure 4.7. The current spikes in the low-current region sometimes exceed two orders of magnitude, and thus it is important to discuss if the reported sharp switching over five orders of magnitude might be due to coincidental oscillation. For this purpose, the I_d/V_d curves for the p-n junction device at different top gate biasing conditions and temperatures are plotted in Figure 4.11(c), showing a near-ohmic behavior for the np configuration. For the intrinsic state (T_{g1} and T_{g2} floating), the current level is more than two orders of magnitude lower and exhibit clear nonlinearity (see inset of Figure 4.11(c)) which is evidence of a clear Coulomb blockade effect.

4.8 Temperature dependence of switching slope

The switching slope as a function of temperature for the forward biasing condition has been extracted for various temperatures and is shown in Figure 4.12 (a). A remarkable independence on temperature is observed up to 25 K.

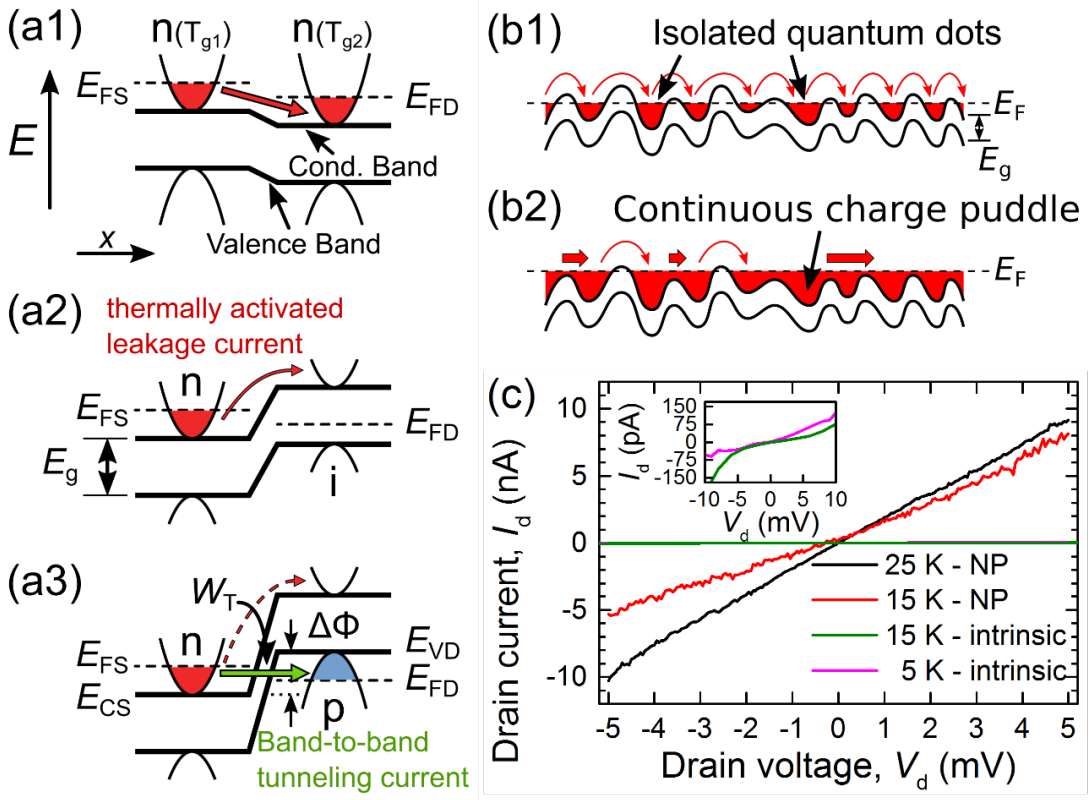


Figure 4.11 (a) Proposed band structure model of the p-n junction. (a1) In the nn configuration (V_{Tg2} = 4 V), continuous doping leads to high current. (a2) In the ni configuration, the only low thermally activated leakage current is observed together with Coulomb oscillation. (a3) When the valence band below T_{g2} crosses above the conduction band below T_{g1}, band-to-band tunneling leads to a sharp increase of current. (b) Schematic illustration of quantum dot formation in GNR with edge irregularities. The size of charge puddles varies strongly at low doping levels. (c) I_d/V_d at various temperatures and doping configurations. In the intrinsic state, clear Coulomb blockade is observed. For the np configuration, near-ohmic characteristics indicate the existence of band-to-band transport mechanism.

It is worth to mention here that the SS degradation by temperature is also observed in conventional semiconductor,[110]–[112] however, it follows a continuous increase governed by the thermal activation energy, and the remarkable temperature independence is not expected. By considering the BTBT phenomena, the transmission probability can be expressed by the WKB approximation [89]:

$$T_{WKB} \approx \boldsymbol{exp}\left(-\frac{\boldsymbol{4W_T\sqrt{2m^*}\sqrt{E_g^3}}}{\boldsymbol{3\hbar(E_g+\Delta\Phi)}}\right) \quad (\mathbf{1})$$

where W_T is the screening tunneling length, m^* is the effective mass, E_g is the energy gap, $\Delta\Phi$ is the tunneling window (i.e. the energy difference between the valence and conduction band right and left of the tunneling barrier E_{VD}-E_{CS}) and ħ is the reduced Planck constant. Hence, the SS becomes[28]:

$$SS \approx \left(\frac{\boldsymbol{\ln(10)}}{\boldsymbol{e}}\frac{\boldsymbol{3\hbar\left(E_g+\Delta\Phi\right)^2}}{\boldsymbol{4\sqrt{2m^*}\sqrt{E_g^3 W_T}}}\right) \quad (\mathbf{2})$$

As can be seen from Eq. (2), the SS modeled by the WKB approximation does not depend on temperature. By using the experimentally determined SS at low temperature, the energy gap of 44 meV and m* = 0.05 m_0 [113], a tunneling length of 8.3 nm has been calculated. If a variation of the tunneling length occurs at the junction between the p-side and n-side, the effective tunneling length at the junction is reduced [114]. For temperatures above 25 K, the experimental data shows a noticeable deviation. It should be noted that the SS due to BTBT cannot be observed directly, instead, it is derived from the transport behavior of the complete device including irregularities, source/drain leads, OFF-state current and thermally activated leakage current. The suppression of the latter is greatly reduced at higher temperature [115]–[117] when the thermal energy becomes comparable to the energy gap. In fact, in our p-n junction, a rapid increase of the off-state current of temperature is observed. Thus, when a different effect than the increase in tunneling current becomes more dominant, or the change of current due to BTBT is relatively small compared to other leakage paths, the SS degradation is predicted and the measured characteristics do not follow the model. The device resistance as a function of temperature is shown in Figure 4.12(b) for the np and in Figure 4.12 (c) for the nn configuration. The drain voltage is 12 mV (3 mV) at a low (high) temperature as mentioned earlier. The resistance increases in both cases at low temperature, which is explained by the multiple quantum dots effect. For the nn configuration, the curve follows the general trend of semiconductors, where the increase of temperature is associated with

an increase of the charge carrier concentration, which leads to a decrease in the resistance before phonon scattering leads to an increase of resistance at increasing temperature.

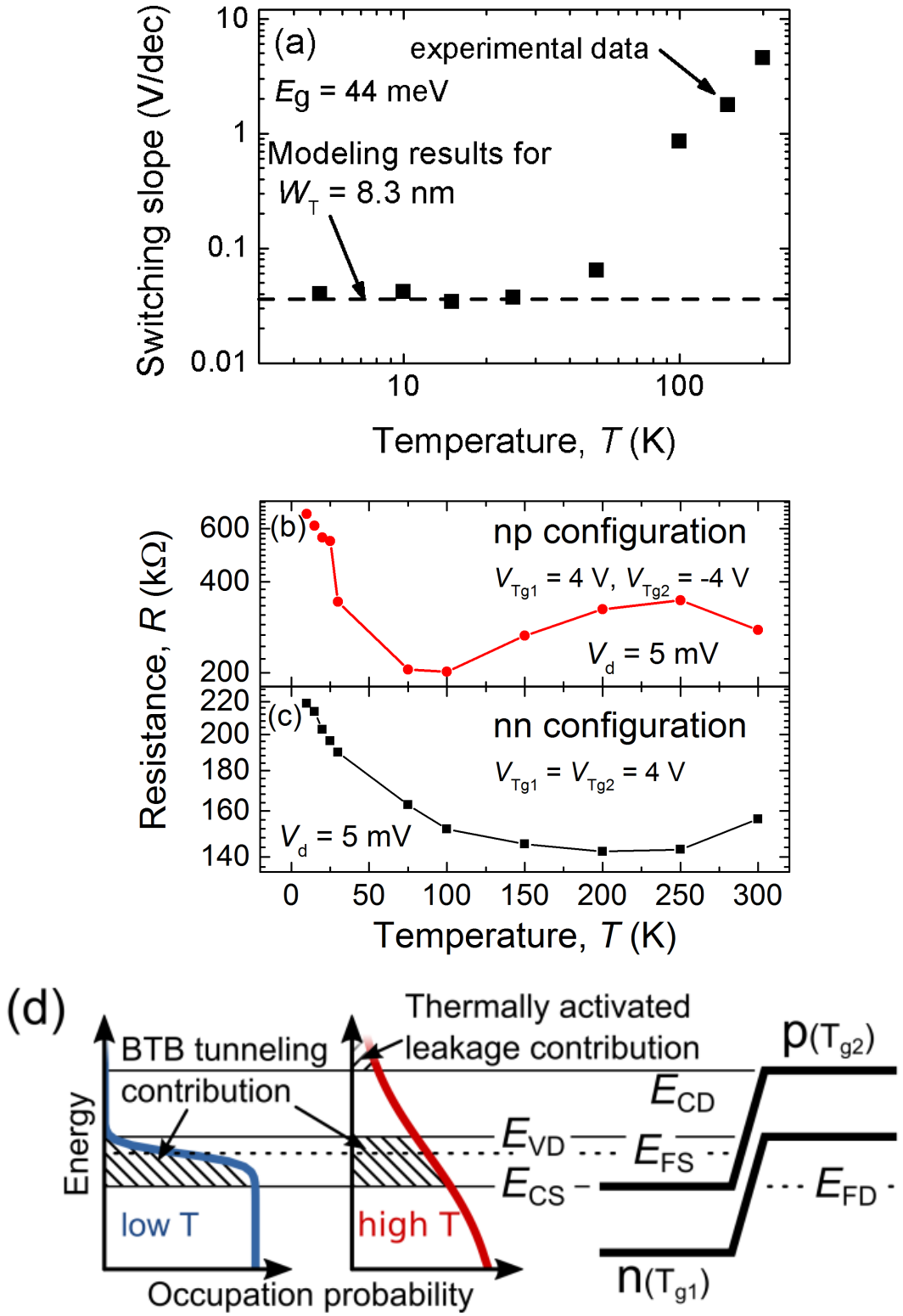


Figure 4.12 (a) Temperature dependence of switching slope and modelling results. A good agreement is found for W_T = 8.3 nm. (b+c) Device resistance as function of temperature in (b) np configuration (V_{Tg1} = 4 V, V_{Tg2} = -4 V) and (c) nn configuration (V_{Tg1} = V_{Tg2} = 4 V) showing distinctively different characteristics. (d) Sketch schematically illustrating influence of device temperature on current contributions. At higher temperature, the thermally activated leakage contribution increases (above E_{CD}).

In stark contrast, the resistance in the np configuration has a minimum at around 100 K, before increasing significantly with temperature. The origin of this increase is illustrated in Figure 4.12 (d), where the band structure of the junction in the np configuration is schematically sketched together with the source Fermi-Dirac distribution at low and high temperature, respectively. At low temperature, a larger number of carriers is available in the BTBT energy window, and the thermally activated leakage current is suppressed (due to the energy gap and low concentration above E_{CD}). With increasing temperature, however, the FD distribution smears out in a way that the total charge contribution for transport is reduced (suppression due to energy gap below T_{g2} is enhanced). The FD distribution of the carrier within the bias window changes considerably with temperature. Therefore, the tunneling current decreases by increasing the temperature [116]. Finally, above 250 K, the device resistance decreases again (see Figure 4.12 (b)). This is due to the enhanced thermally activated leakage current. Note that the absolute resistance of 300 K of ~300 kΩ in the np configuration is still considerably higher than in the nn configuration (~160 kΩ), signifying the presence of the potential barrier.

4.9 Conclusion

In this chapter, the sharp switching behavior observed in a graphene p-n junction with a finite band gap of ~44 meV shows good agreement with a device model based on band-to-band tunneling. When the channel is modulated continuously by the back or synchronized top gates, the sharp switching is not observed due to the lack of BTBT. The asymmetry between np and pn configuration is explained as a consequence of the top gate misalignment. Device simulations show that potential bumps are formed in the unmodulated channel regions, which affect the bias window differently. The current noise in the OFF-state is caused by the edge roughness induced by the reactive ion etching technique to pattern the GNR. Finally, I showed the temperature dependence of the switching slope and the device resistance, highlighting that the observed device characteristics can only be explained by BTBT.

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5 GNR Tunnel Field Effect Transistor

Here, I report a temperature independent subthreshold slope (SS) of ~ 47 mV/dec at low temperature in a triple top gate graphene tunnel field-effect transistor (TFET). The outer gates are used to define the *p* and *n*-doped regions of the ~9.4 nm wide graphene nanoribbon, while the middle gate is used to switch the device between the ON and OFF states. Due to the flexibility of electrostatic doping, the device characteristics are compared in different configurations, specifically, field-effect transistor (FET) mode and TFET mode. A minimum SS of ~ 47 mV/dec along with a saturation current density of ~ 6.1 μA/μm is realized in the case of TFET mode at 5 K. This low SS is found to be independent up to 40 K, after which an exponentially increase is observed with a slope of 8.4 V/dec at 300 K. In clear contrast, linear temperature dependence of the SS is found in the case of FET mode.

5.1 Introduction

In the previous chapter, BTBT behavior was reported in the GNR *p-n* junction with two top gates and a global back gate. However, to make the device usable as a switch with superior behavior to the silicon MOSFET, it is necessary to control the intrinsic region independently. Here I report, for the first time, band-to-band tunneling (BTBT) in a sub-10 nm GNR controlled triple top gate transistor. The device structure is schematically illustrated in Figure 5.1a. The TFET is a *p-i-n* junction in the reverse bias configuration where the intrinsic region is modulated by a gate. Since conventional chemical doping techniques of carbon-based nanostructures are challenging due to the strong C–C bonds in GNRs[118], electrostatic doping is used here to set the doping. The outer gates (T_{g1} and T_{g3}) are used to electrostatically define the *p*-doped source, and *n*-doped drain, respectively, while the middle gate (T_{g2}) is used to modulate the intrinsic channel to switch the device between the ON and OFF states. The typical band structure along the channel for the TFET-mode is shown in Figure 5.1b, where E_g is the energy gap, and λ is the tunneling width in the ON-state. The performance of the tri-gate GNR

in the TFET and FET mode is investigated over a wide range of temperatures (from 5K to 300K) experimentally. In the case of TFET mode, a constant SS of ~ 47 mV/dec is observed at low temperatures between 5 K and 40 K. Then SS gradually increased until 100 K, however, higher than 100 K the SS showed an exponential increase by increasing temperature. I found a strong correlation between I_{OFF} and SS, both showing the same trend with temperature. The current density of ~ 6.1 µA /µm is achieved at V_D = 10 mV, which is comparable to the best results of conventional semiconductor TFET [119]. The reported results highlight the great potential of GNRs in the field of TFETs and low power applications.

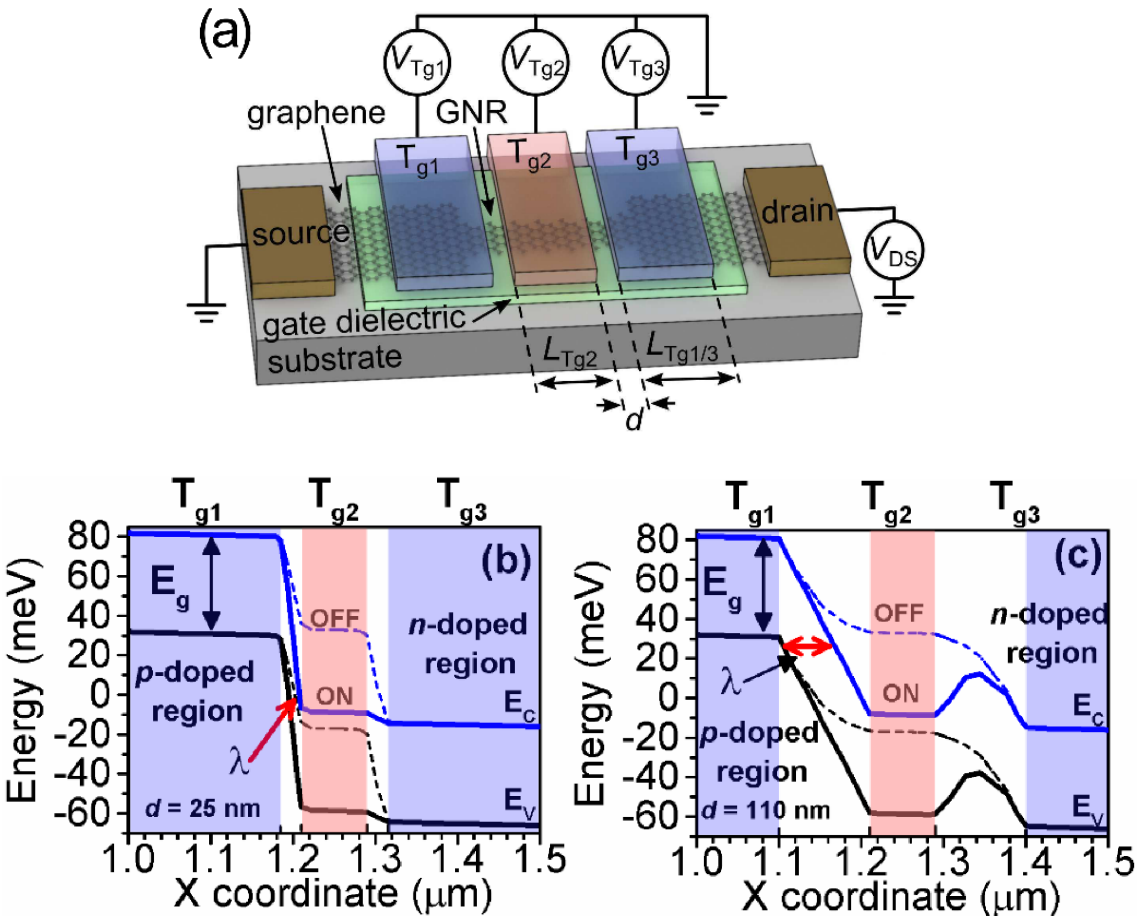


Figure 5.1 (a) Schematic illustration of the triple gate GNR-TFET device. (b+c) extracted GNR band structure with E_g of 50 meV from Silvaco TCAD 3D simulation at the ON state in case of d = 25 and 110 nm, respectively. Tg1 voltage (V_{Tg1}) and Tg3 voltage (V_{Tg3}) are fixed at – 6 V and + 6 V, respectively, and the middle gate voltage (V_{Tg2}) swept from zero (OFF state) to 6 V (ON state).

5.2 Device fabrication and characterization

T Single layer chemical vapor deposition (CVD) grown graphene sample is coated with a ~ 35 nm high-resolution negative tone e-beam resist, hydrogen silsesquioxane (HSQ) and patterned to form an etch mask defining the nanoribbon with a length of 500 nm. The narrow GNR was achieved by the reactive ion etching (RIE) technique, where oxygen plasma is used to etch away the unprotected CVD graphene, leaving the GNR protected underneath the HSQ etching mask. I optimized the RIE process in order to avoid unnecessary increase in LER. The etching time is minimized to 7 seconds under a low gas pressure of 2.6 Pa in order to achieve anisotropic lateral etching, for more details about the fabrication process refer to [120]. From Silvaco TCAD 3D simulation, I found that the top gate separation *d* should be as small as possible. By comparing devices with *d* = 25 nm and *d* = 110 nm (see Figs. 1b and c), the tunneling length (λ) is significantly reduced (which increases ON-state current) and unwanted potential bumps can form in the gap area. Here, 30 nm top gate separation is achieved, as shown in the AFM image of the fabricated device in Figure 5.2a. the narrower GNR at the center of the channel and wider graphene acting as an extension of the source and drain contacts are covered by the SiO_2 and top gates but still visible. All measurements were performed in a variable temperature helium closed cycle cryogenic refrigeration system. It is important to realize electrostatically controlled individual *p* and *n* regions in the GNR device. The functionality of the individual gates is confirmed by measuring the source drain current (I_D) as a function of the back gate as well as individual top gate voltages. The good tunability at room temperature is evident from the results in Figure 5.2b. From all gate modulations, it is obvious that the charge neutrality point (CNP) is almost zero volt, which indicates small doping of the GNR. This characteristic is crucial as it reduces the required gate voltage offsets and offers symmetric tuning. However, in back gate modulation, the CNP is shifted slightly to - 0.5V, this may due to substrate impurities at the wide graphene extension of the source and drain contacts. The extracted minimum conductance (g_{min}) in the back-gate characteristics is shown as a function of temperature in Figure 5.2c. At low temperature (5 to 20K), g_{min} is almost constant. In semiconductors, it is well known that at such low temperatures, carrier transport is dominated by tunneling rather than thermal injection[47]. However, the gradual increase of conductance with increasing temperature follows the relation $g_{min} \propto exp(-E_g/2K_BT)$. An E_g of ~ 70 meV is extracted from the slope at high temperature. Using the equation $W = (\hbar v_f)/E_g$ ($\hbar$ is the reduced Plank

constant, W is the GNR width and v_f = 10^6 m/s is the Fermi velocity)[101], the effective GNR width is estimated to be ~ 9.4 nm.

Table 1.Tri-gate device dimensions

L_{ch}	L_{Tg1}	L_{Tg2}	L_{Tg2}	d
500 nm	280 nm	70 nm	280 nm	30 nm

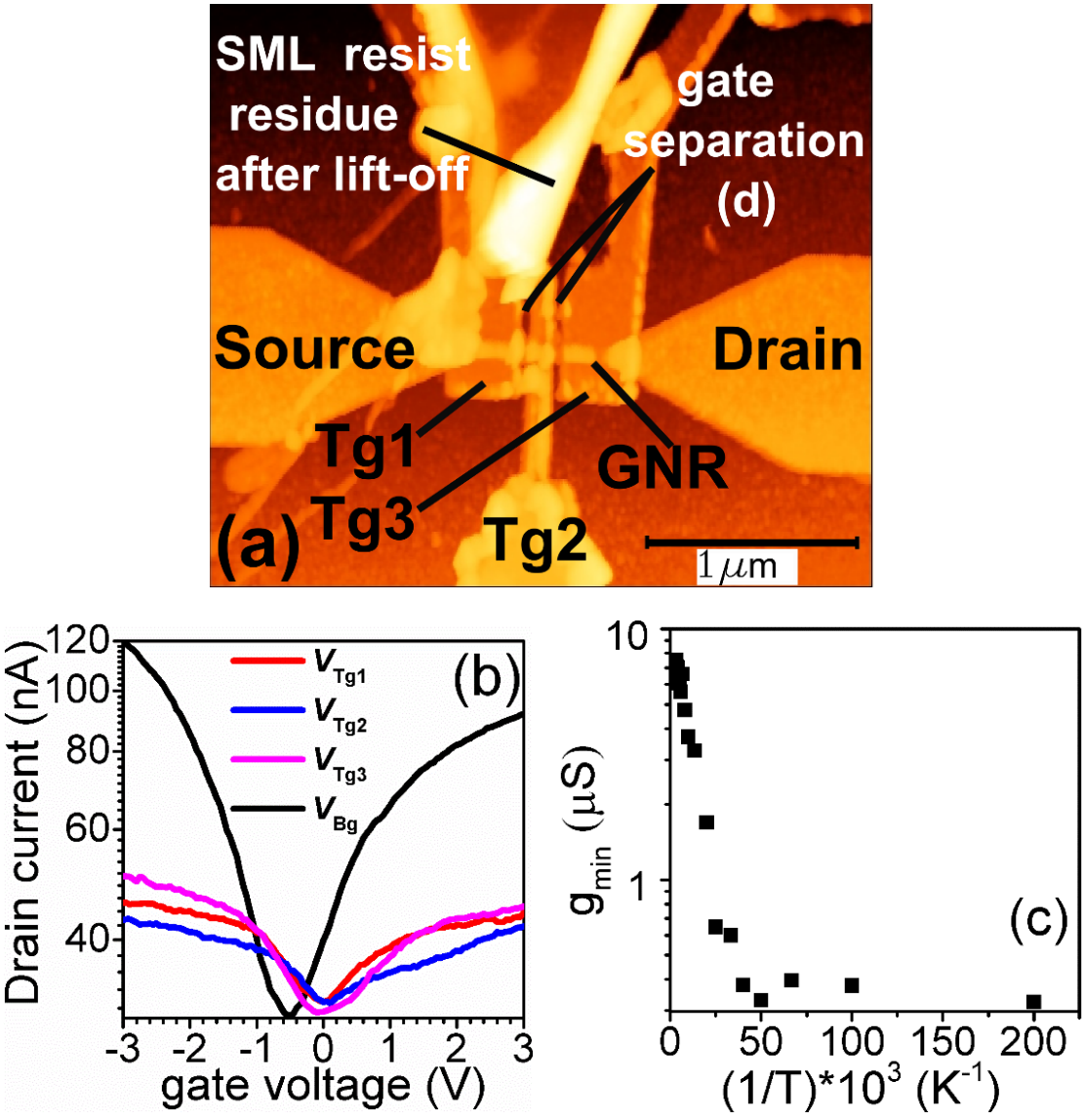


Figure 5.2 (a) AFM image of the measured device shows the separation d ~ 30 nm between the top gates above the GNR, and the HSQ etching mask of ~ 30 nm width. (b) Ambipolar characteristics at 300 K for VD = 10 mV measured for back gate and individual top gates (c) Arrhenius plot of the minimum conductance (gmin) used to extract E_g.

5.3 GNR-TFET operation

In this section, I will explain the operation mechanism of our GNR-TFET. The operation mechanism is shown below:

- At $V_{Tg2} = 0$: the conduction band edge of the channel E_a^{ch} is higher than the source valence band edge E_V^S . therefore, the electrons cannot tunnel through the very wide gap to the drain region and the device is in the OFF state,
- At $V_{Tg2} > 0$ V: The E_a^{ch} edge became lower than the E_V^S edge and the tunnelling length became much smaller and the current can tunnel to the drain region.

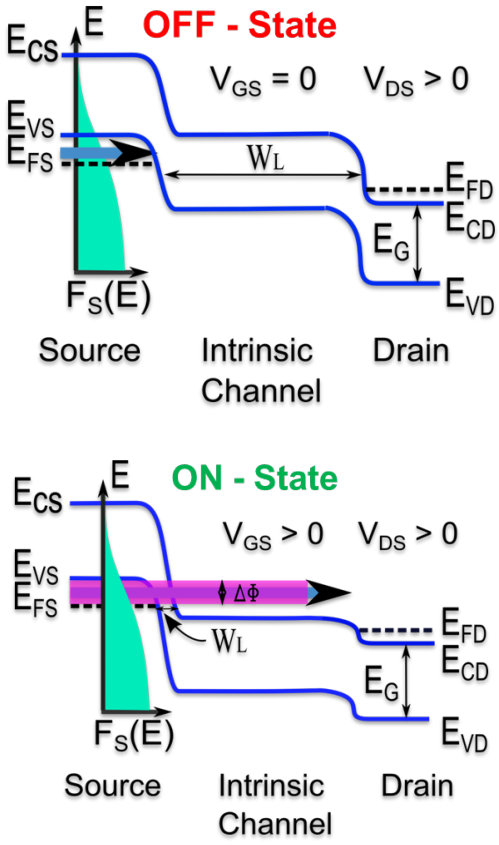


Figure 5.3. (a) Device structure of n-TFET and the corresponding energy band diagram in the OFF and ON state. FS(E) is the Fermi-Dirac distribution of electrons in the source region. WL is the minimum tunnel width, EFS/D is the source - drain Fermi level, and ΔΦis the allowed tunnel window

- At $V_{Tg2} < 0$ V: The E_a^{ch} edge should go higher than the Fermi level at the source region to open an energy window (dE), similarly like what happened in the case of positive V_{Tg2}, to allow for the electron to tunnel to the drain region. This is the reason why the slop in the negative region much lower than the slop in the positive V_{Tg2} region.

5.4 Transport characteristics

To ensure that the carrier transport characteristics through our device is due to the BTBT, I compare the characteristics of the device in the TFET (top gates) and FET (back gate) configurations, respectively. This is possible due to the flexible electrostatic doping. In TFET configuration, top gate 1 voltage (V_{Tg1}) and top gate 3 voltage (V_{Tg3}) are fixed at – 6 V and + 6 V to induce *p* and *n*-doping, respectively, while the middle gate voltage (V_{Tg2}) is swept from – 3 V to + 3 V. In the FET mode, I simply used the global back gate (Si substrate) to control the Fermi energy, while all the three top gates are floating. The back-gate voltage (V_{Bg}) is swept from – 3 V to + 3 V. In all measurements shown here the source-drain voltage (V_D) is fixed at 10 mV ($V_D < E_g/2$) to decrease the ambipolarity and I_{OFF}[121]. Figure 3 shows the carrier transport characteristics in both modes. As can be seen in Figure 5.4a, in the case of FET mode, the drain current (I_D) shows clear ambipolar behavior with high I_{ON}/I_{OFF} ratio of ~ $2.5x10^3$. Clear current spikes are observed around the CNP (V_{Bg} ~ 0.7 V), which can be attributed to the multiple quantum dots effect[105], [107], [109]. The shift of CNP from ~ 0V at 300K (compare Figure 5.2b) to 0.7 V at 10 K is due to charge impurities. In contrast, in the TFET mode I_D shows a steep current jump followed by a remarkable current saturation (I_{ON}) when V_{Tg2} is swept in the positive direction (*n*-type conduction), see Figure 5.4b. However, when V_{Tg2} is swept to the negative direction (*p*-type conduction), no sharp transition is observed and the I_D experiences clear oscillations followed by current saturation. These oscillations are observed only at low temperatures. Their intensity gradually decreases until disappearing at higher temperatures. This may attribute to the multiple quantum dots effect[122], which has a significant effect when the charging energy of the dots is lower than the thermal energy. The observed asymmetry of *n*-type conduction ($+V_{Tg2}$ sweep) and *p*-type conduction ($-V_{Tg2}$ sweep) can be attributed to the asymmetry of the source-drain doping

level[123]. If the *n*-type doping level in the drain region (controlled by Tg3) is lower than the *p*-type doping level in the source region (controlled by Tg1) the tunneling length (λ) of holes increases. This due to the increase of the electrostatic screening length for low doping level[123]. However, this explanation apparently conflicts with the symmetric gate voltages applied (- 6 V, + 6 V) to both source and drain regions, respectively. This conflict can be resolved by considering the effect of LER. Due to the LER the edges of the bandgap (valence band edge and conduction band edge) are not at the same energy level along the channel, therefore, the relative position of the Fermi level to the bandgap edges (doping level) will not the same even if the applied gate voltages are symmetric.

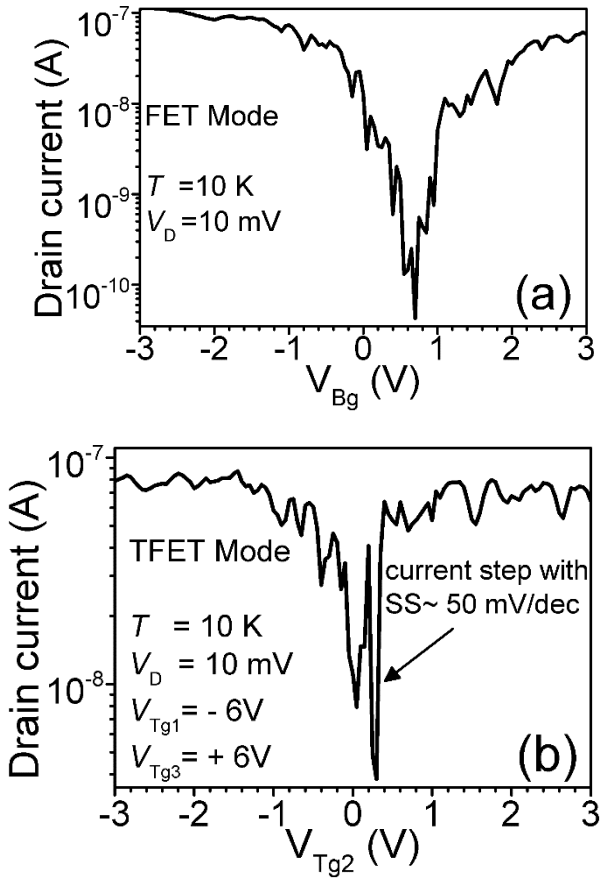


Figure 5.4 (a) Drain current as a function of the back-gate voltage (FET mode). Top gates are floating. (b) TFET mode: The middle gate voltage (V_{Tg2}) is swept from -3 V to 3 V, while the V_{Tg1} and V_{Tg3} are fixed at -6 V and 6 V, respectively.

Although the I_{ON} is nearly the same in both configurations, the I_{OFF} in the TFET mode is significantly increased and the I_{ON}/I_{OFF} ratio is decreased to ~20 (100 times lower). Even though a significant difference of drain current behaviour between the two modes is noticed, it is not sufficient to attribute the sharp current transition to BTBT above all doubt: Firstly, our device shows a large OFF-state current at low temperature, and secondly, the device in FET configuration shows a remarkable step current transition at low temperature as well. However, the clearly different transfer characteristics between

the two modes indicate that the carrier's injection mechanisms are different. Therefore, to clarify the difference between the two modes, the temperature dependence of the SS next will be discussed.

5.5 Temperature dependence of subthreshold slope

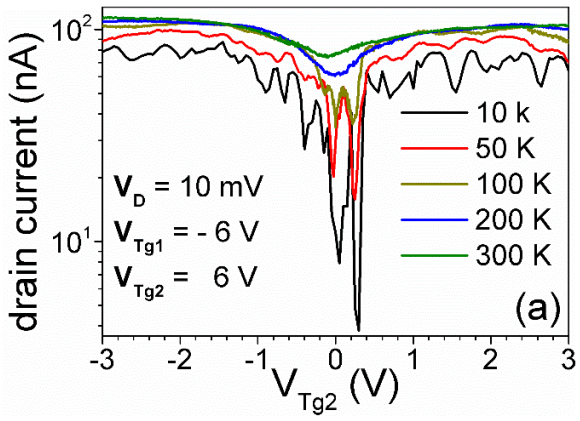
The SS of TFET should be robust against temperature variations when the source-Tg1 barrier is sufficiently high compared to the thermal distribution. In contrast, it is well known that the standard FET is characterized by the linear temperature dependence of the SS ($2.3*K_BT/q$). The SS is shown here extracted from the I_D -V_{Tg2} (V_{Bg}) curves according to the relation[10],

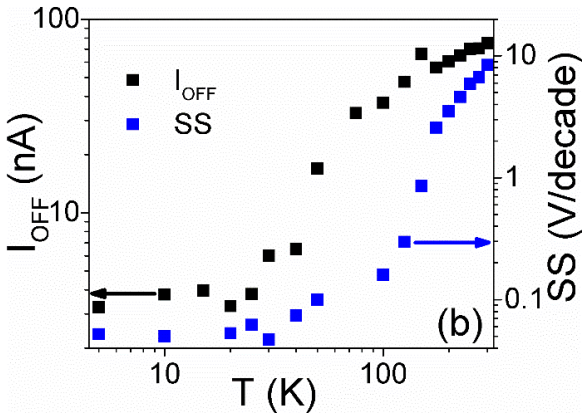
$$SS = (\frac{d \log I_D}{dV_g})^{-1} \qquad (1)$$

Where I_D is the drain current and Vg is the applied gate voltage. The I_D -V_{Tg2} characteristics of our device operated in TFET mode between 10 and 300 K are shown in Figure 5.5a. At low temperature, the current has a sharp slope (SS ~ 47 mV/dec). By increasing the temperature, the current transition slope decreases (larger SS). The extracted values of SS from the I_D-V_{Tg2} curves in Figure 5.5b show temperature independence up to 40 K, followed by a gradual increase with temperature up until 100 K (SS ~ 180 mV/dec). Above 100 K, an exponential increase of SS is observed, finally reaching 8.4 V/dec at 300 K. Interestingly, I_{OFF} shows a very similar trend with temperature (see Figure 5.5b). On the other hand, in the FET mode, the SS shows linear temperature dependence over the whole range of temperatures (10 to 300 K), similar to the thermal limit of the MOSFET (see Figure 5.5c). For temperatures up to 100 K, the SS in the FET mode (700 mV/dec) exceed the one of the TFET mode (180 mV/dec). However, at 300 K the SS for the FET mode is lower (3V/dec). This remarkable inversion of the SS, together with the temperature independence at low temperature in the TFET configuration is a substantial evidence that the drain current does not originate from the thermionic emission and is due to BTBT.

Temperature dependence of SS was theoretically predicted for a graphene TFET[124]. The dependence is attributed to the change of the Fermi distribution (FD) with temperature in the highly doped source region. However, due to the narrow energy gap of our device and the LER, which was not considered in[124], other possibilities should be taken into consideration besides the effect of FD. One of the main possible reasons for the SS degradation with temperature is the narrow band gap of ~70 meV, accompanied

with the effect of LER. The LER is expected to cause a further reduction in the energy gap by creating tunneling leakage channels. This increases the tunnel leakage current as well as the effect of thermally activated current[114]. This explanation is supported by the behavior of the I_{OFF} with temperature which is very like the SS (see Figure 5.5b). At low temperature (5 ~ 40 K), the effect of thermally activated leakage current can be ignored due to the low thermal energy compared to the high built in the potential barrier of the *p-i-n* structure in the TFET mode. Therefore, the main source of the high OFF state leakage at low temperature is the direct tunnel leakage current from the highly *p*-doped source to the channel. That explains why the SS is independent of temperature in the range from 5 to 40 K. In addition, at a higher temperature, due to the narrow E_g and the tunnel leakage channels, the carriers in the *p*-doped source region are excited thermally to the conduction band of the source or the channel. Consequently, the I_{OFF} increases exponentially with temperature.





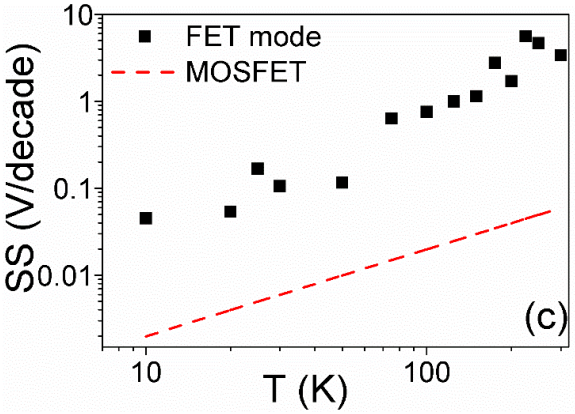


Figure 5.5 (a) I_D-V_{Tg2} at different temperatures for TFET mode. V_{Tg1} and V_{Tg3} are fixed at – 6 V and + 6 V, respectively, and V_D is 10mV. (b) The extracted values of I_{OFF} and SS from I_D-V_{Tg2} curves in (a). (c) SS as a function of temperature of our device in FET mode and the thermal limit of the MOSFET

5.6 Summary

In summary, I successfully realized band-to-band tunneling in a tri-gate GNR-TFET with a temperature independent subthreshold slope of ~ 47 mV/dec when operating below 40 K. Furthermore, a current density of 6.1 μA /μm by using only 10 mV drain voltage is reported. However, the I_{ON}/I_{OFF} ratio is relatively low because of the high OFF-state current, primarily due to a small band gap of approximately 70 meV for the 9.4-nm-wide GNR channel. Although the current device shows low performance, with a further decrease in the GNR channel width to the single-nanometer regime, an enhanced band gap will improve both the SS and ON/OFF ratio.

6 Summary and future work

6.1 conclusion

In this thesis, I demonstrated for the first time, a successfully working GNR-TFET. I achieved a minimum SS of 47 mv/dec and I_{ON} ~ 6.1μA/μm. By using EBL-RIE technique, I could pattern a GNR with ~ 9.4 nm width. Consequently, a GNR with ~ 70 meV energy gap is realized. To achieve that, I developed the EBL writing strategy to minimize the proximity effect which deteriorates the resultant resolution of the EBL system. High-resolution EBL resist, HSQ, and SML used here to get the minimum features as possible.

GNR-TFET, in principle, is a reverse biased *p-i-n* junction. Therefore, our first steps were fabricating a GNR *p-n* junction and study the electronic transport at different doping levels and different temperatures. I successfully realized a GNR *p-n* junction by fabricating two top gates on top of GNR with 15 nm GNR width. Our fabricated devices showed a distinct four regions that belong to the different combination of (pn, np, pp, nn) the top gates polarities. A current saturation noticed clearly at the reverse bias and not observed at the forward bias. This behavior is repeated in a wide range of temperatures ranging from 5K to 250 K. a steep current transition with slope 42 mV/dec is realized at low temperature up to 40 K. This sharp switching behavior only can be explained by considering interband tunneling.

After the successful demonstration of the BTBT current existence in the two top gates *p-n* junction, I fabricated a three top gates device to confirm the TFET operation. I measured for the first time a TFET based GNR. I successfully realized band-to-band tunnelling in a tri-gate GNR-TFET with a temperature independent subthreshold slope of ~ 47 mV/dec when operating below 40 K. Furthermore, a current density of 6.1 μA /μm by using only 10 mV drain voltage is reported. However, the I_{ON}/I_{OFF} ratio is relatively low because of the high OFF-state current. With a further decrease in the GNR channel width to the single-nanometer regime, an enhanced band gap will improve both the SS and ON/OFF ratio.

6.2 Future work

In the current work, the average SS is still larger than the MOSFET limit (60mV/dec) and the I_{ON}/I_{OFF} ratio still very low as well. Therefore, many improvements still needed to get a reliable GNR-TFET with high performance.

GNR-TFET can be improved by focusing on two parallel ways as follow:

6.2.1 GNR edges issue

Effects of disorder in GNR edges are a well-known issue. What I would like to concentrate on is how to make the GNR edges smoother. Using EBL-RIE technique to fabricate the GNR cause a very high degree of roughness, even using positive resist (limited resolution) or negative resist (high resolution). Here, I propose the idea of using HIM milling beside the EBL (see Figure 6.1a and b). This can be realized in two steps:

- Fabricate a wide GNR by EBL-RIE technique ≈ 30 nm
- Mill, the GNR to the desired width, using HIM milling

Using this way a much smoother narrower and wider energy gap are expected.

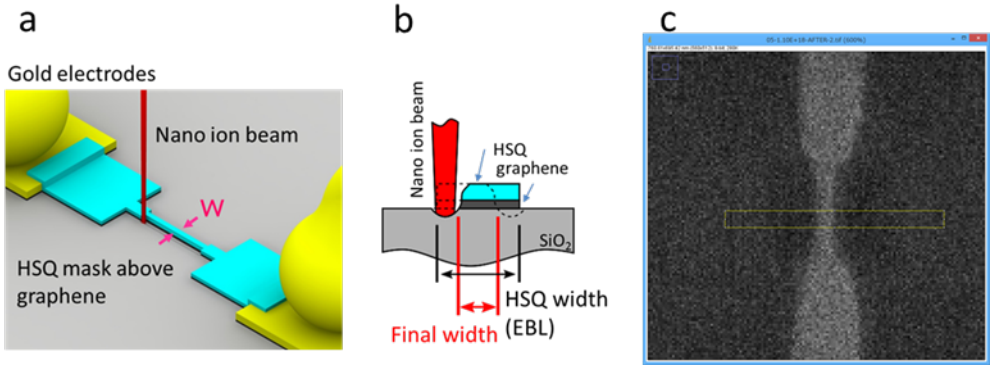


Figure 6.1.(a,b) schematic diagrams show GNR milling process, (c) SEM image of ~ 6 nm GNR. Reproduced with permission from "Marek E. Schmidt".

6.2.2 The geometry and electrostatics of GNR-TFET

In this section, I would like to give a brief description of what can be done to improve our GNR-TFET performance based on literature reviews and my ideas. The following parameters should be taken into consideration during the design and fabrication of the GNR-TFET.

Table 2. Critical Parameters for ON-Current Enhancement in TFET

ON Current Enhancement Parameters	Feasibility	Parameter Type
1. Low energy gap (E_G) 2. Low effective mass (m*) 3. Channel thin body	Satisfied in GNR	Material Parameters
4. High-k dielectric permittivity 5. Low dielectric thickness 6. Double gate channel control 7. Appropriate source/drain metal contacts	Deliberate design& Fabrication technology	Electrostatic Parameters

Table 3. Critical Parameters for OFF-Current Suppression in TFET

OFF Current Suppression Parameters	Feasibility	Parameter Type
1. Drain voltage < (E_G/q)		Electrostatic Parameters
2. Low drain doping level	• In case of GNR (low top gate voltage)	
3. Hetero-structure	• Source with low E_G • Drain and channel with higher E_G	
4. Hetero-structure dielectric engineering	• High-k dielectric in source-channel junction • Low-k dielectric at the channel-drain junction	
5. Underlap the top gate at the channel-drain junction	• Shift the top gate away from the channel-drain junction	

6.2.3 Novel Design For high-performance GNR-TFET

Based on our understanding of the TFET operation and according to the advanced technology available in JAIST and our collaborators, I proposed the following GNR-

TFET design. In this design, I take into consideration most of the parameters that can boost the device performance (see Table 2). I intended to use the EBL-RIE and HIM milling techniques to achieve high-performance GNR-TFET. The advantage of this design is mixing different technologies to overcome the limitations. For example, EBL-RIE can produce GNR with widths lower than 20 nm but with very high edge roughness that can suppress the ON current significantly. On the other hand, HIM milling can pattern the GNR to < 10 nm directly, but higher doses can cause swelling of the substrate and problem of current drift at the longer time of exposure. These problems mean it is hard to use HIM to pattern large scale device to sub-10 nm scale. Therefore, I decided to use the EBL-RIE technique to pattern the GNR to relatively small dimensions then using HIM to go further sub-10 nm scale. The device design and fabrication process flow explained below (see Figure 6.2). In this design, I deposit large b pad of Aluminum using EBL- lift off technique. Then the Al pad will be divided to three pads which will be the metal of the local gates. After that, the sample should be kept in H_2O vapor rich environment at high temperature (~160ºC) to form an aluminum oxide layer of ~ 4 nm. Then the CVD graphene should be transferred on top of the alumina and fabricate the source-drain contacts. To decrease the device resistance, I will fabricate the source contact from Palladium and the drain from chromium. In the next step, the EBL-RIE technique will be sued to pattern the GNR to ~ 35 nm the HIM will be performed to pattern the GNR to < 10 nm. Also, one can fabricate heterostructure to increase the ON current and decrease the OFF current at the same time. The advantages of this design are:

- **Flexibility**: different high k dielectric other than Al_2O_3can be tested. For example, one can deposit Au and HfO_2 at the same step (step 3 in Figure 6.2). Therefore the local gate stack will be (Au/HfO_2) instead of (Al/ Al_2O_3). h-BN can be used as a local back gate dielectric to boost the mobility.
- **Large scale integration**: the same local back gates can be used to control a huge number of devices at the same time.
- **Easy inetgration for digital application**. GNR-TFET inverter shown in Figure 6.3

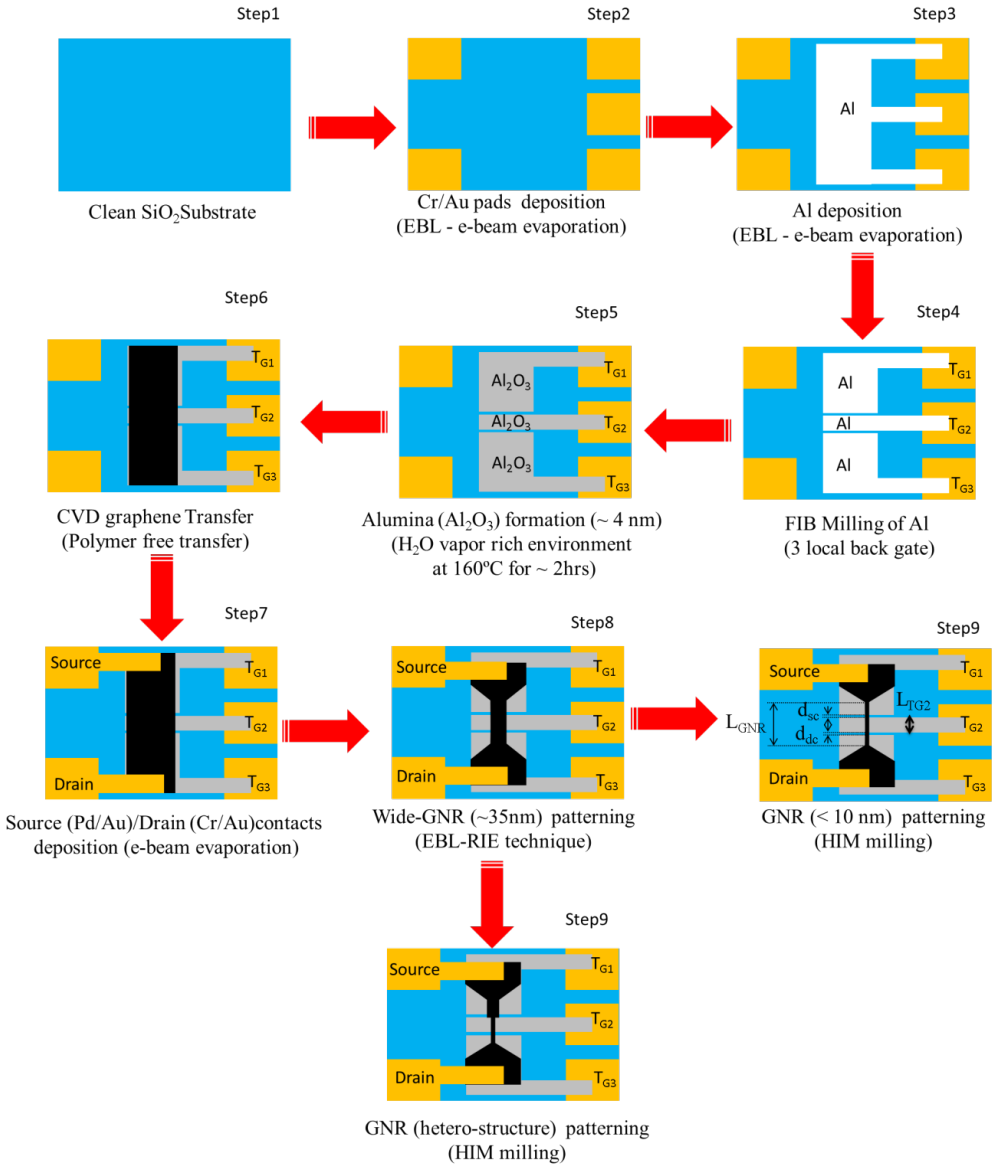


Figure 6.2. Fabrication flow process of a novel high-performance GNR-TFET. L_{GNR} is the GNR channel length. L_{TG2} is the middle gate length. d_{sc} and d_{dc} are the source-channel and drain-channel separation gap, respectively.

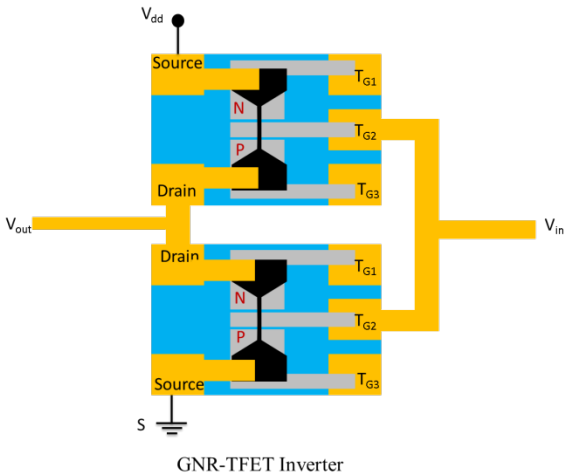


Figure 6.3. Schematic representation of GNR-TFET inverter.

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8 List of Publications

Journal Publications

1- **Ahmed M. M. Hammam**, M.E. Schmidt, M. Muruganathan, H. Mizuta, **Sharp switching behaviour in graphene nanoribbon p-n junction**, Carbon. 121 (2017) 399–407. doi:10.1016/j.carbon.2017.05.097.

2- **Ahmed M. M. Hammam**, M.E. Schmidt, M. Muruganathan, Shunei Suzuki, H. Mizuta, **Sub-10 nm graphene nano-ribbon tunnel field-effect transistor**, submitted

International conference:

1 Shunei Suzuki, **Ahmed M. M. Hammam**, Marek E. Schmidt, Manoharan Muruganathan and Hiroshi Mizuta, ***Sub 0.5 V bias voltage operation of a triple-topgate graphene tunnel field effect transistor***, to be presented in Simulation of Semiconductor Processes and Devices (SISPAD 2017), Kamakura, Japan, 7-9 September, 2017

2 H. Mizuta, **A. Hammam**, J. Kulothungan, S. Suzuki, M. E. Schmidt, J. Sun and M. Muruganathan, **Recent progress of graphene-based nanoelectronic devices and NEMS for challenging applications (Invited Talk)** The International Conference on Solid-State and Integrated Circuit Technology (ICSICT2016), Hangzhou 25-28 October, 2016

3 H. Mizuta, **A. Hammam**, J. Kulothungan, S. Suzuki, M. E. Schmidt, J. Sun and M. Muruganathan, **Graphene-based nanoelectronic and nano-electro-mechanical (NEM) devices for challenging applications (Invited Talk)** Nanonet International Workshop 2016, Prague, 30 August - 2 September 2016

4 H. Mizuta, **A. Hammam**, S. Suzuki, J. Kulothungan, M. E. Schmidt, J. Sun and M. Muruganathan, **Recent progress of graphene-based nanoelectronic and NEM device technologies for advanced applications (Keynote Speech)** The 2th IEEE International Conference on

Semiconductor Electronics (IEEE-ICSE2016), Kuala Lumpur, 17-19 August, 2016

5 **A. Hammam**, M. E. Schmidt, M. Muruganathan and H. Mizuta, **Graphene tunnel transistors for ultra-low-power applications**. Nanoelectronics & Nanotechnology Group Annual Conference 2016 "Sensors", Southampton, 1 July 2016

6 M. E. Schmidt, O. Takechi, M. Muruganatan, **A. Hammam**, T. Kanzaki, S. Ogawa and H. Mizuta, **Recent progress in helium-ion-based nanofabrication for advanced graphene device applications (Invited Talk)** The 1st International Conference on Helium Ion Microscopy and Emerging Focused Ion Beam Technologies (HEFIB 2016), Luxembourg City, 8-10 June, 2016

7 H. Mizuta, T. Iwasaki, S. Suzuki, O. Takechi, **A. Hammam**, J. Sun, M. E. Schmidt and M. Manoharan, **Downscaled graphene devices for low-power nanoelectronics and advanced sensing (Invited Talk)** IISc-JAIST Joint Workshop on. Functional Inorganic and Organic Materials, Nomi, 7-8 March, 2016

8 **Ahmed M. M. Hammam**, M. E. Schmidt, M. Muruganathan and H. Mizuta, **electrostatically defined Graphene P-I-N Junction using Nitrogen Focused Ion Beam Milling,** the 5th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO 2015), Niigata, 16 –19 June 2015.

9 Hiroshi Mizuta, Takuya Iwasaki, Shunei Suzuki, **Ahmed Hammam**, Jian Sun, Marek E. Schmidt and Manoharan Muruganathan, **Recent progress of graphene nanoelectronic and NEM device technologies for advanced applications** (Invited Talk). Nano Information Processing an international conference and workshop 2015, Cambridge, UK, 14-16 December 2015

10 Hiroshi Mizuta, Takuya Iwasaki, Shunei Suzuki, **Ahmed Hammam**, Jian Sun, Marek E. Schmidt and Manoharan Muruganathan, **Downscaled graphene nanoelectronic and NEM devices for advanced applications** (Invited Talk). The 2nd Malaysia-Japan Joint Symposium on Nanotechnology, Ishikawa, Japan, 10-12 November 2015.

Domestic conference:

1 Marek Schmidt, **Ahmed Hammam**, Manoharan Muruganathan, Shinichi Ogawa and Hiroshi Mizuta, **Helium ion milling of HSQ covered graphene: Control of substrate swelling and imaging disorder,** 第 77 回応用物理学会秋季学術講演会 2016 年 9 月 13 日-16 日　朱鷺メッセ　新潟県新潟市

2 **Ahmed Hammam**, Marek Schmidt, Manoharan Muruganathan, Hiroshi Mizuta, **Triple Gate Graphene Nanoribbon Field Effect Transistor (TG-GNRFET)**, The 63rd JSAP Spring Meeting, 2016.

3 **Ahmed Hammam**, Marek Schmidt, Manoharan Muruganathan, Hiroshi Mizuta, **Electrostatically Controlled P-I-N Junction in Graphene Nanoribbon Devices**, The 76th JSAP Autumn Meeting, 2015.

4 Manoharan Muruganathan, **Ahmed Hammam**, Wenzhen Wang, 岩崎拓哉, Marek Edward Schmidt, 水田博, 'グラフェンナノリボンを用いたトンネルトランジスタの研究', COI-T プログラム「オンデマンド・ライフ＆ワークを全世代が享受できる Smart 社会を支える世界最先端 ICT 創出 COI 拠点」平成 25 年度成果報告会, Poster Presentation, Tokyo, March 18, 2014