JAIST Repository
https://dspace.jaist.ac.jp/

Title	効率的耐故障集積回路のための時間・空間冗長最適化に関する研究
Author(s)	呉，政訓
Citation	
Issue Date	2018-03
Type	Thesis or Dissertation
Text version	ETD
URL	http://hdl.handle.net/10119/15322
Rights	
Description	Supervisor:金子　峰雄，情報科学研究科，博士

JAIST
JAPAN
ADVANCED INSTITUTE OF
SCIENCE AND TECHNOLOGY

Japan Advanced Institute of Science and Technology

Abstract

Due to the downsizing of VLSIs, several reliability issues have become more explicit. Among the issues, soft-error induced degradation is one of the dominant contributors to faults on modern VLSIs. Soft-error is a transient fault which is triggered by cosmic ray induced neutron and alpha rays from radioactive contaminants in IC package materials. Soft-error lasts only short time but it can affect several spatial points simultaneously.

Approaches to dealing with soft-errors are roughly divided into the following three groups: i) approaches on the device level such as selecting of IC packing materials and improving of well structures; ii) approaches on the circuit level such as a flip-flop with additional circuits for error detection, error recovery and error avoidance; iii) approaches on the system level which includes multiple module redundancy such as concurrent error detection and triple modular redundancy. Most semiconductor designs rely on computer aided design systems and implementation of reliability on semiconductor devices on higher design level is important at the viewpoint of optimization. Nevertheless, because there is no dominant approach with a single level for soft-error tolerance and such a single level scheme imposes high overheads in terms of power, performance and chip area, a higher level approach should be assisted by approaches on other levels. Thus, it is assumed that several approaches are implemented across distinct levels in this research although the author focuses on the system level approach via high-level synthesis. As a result of high-level synthesis, fault-tolerance is implemented to datapath circuits in register-transfer level (RTL).

This dissertation proposes a method to synthesize application specific soft-error tolerant datapaths via high-level synthesis. To guarantee reliability and high real-time property, the proposed method is based on the triple redundancy of computation algorithms, which are to be realized as datapath circuits. The method reduces time overhead originated in redundancy, and at the same time, it realizes datapaths that keep multiple component soft-error tolerance. In order to mitigate time overhead, error detection parts with comparison and error correction parts with retry share resources speculatively (speculative resource sharing). Operations in the retry parts are not executed as long as no error detected. During this period, resources bound to those operations in the retry parts are in an idle state. If it is assumed that the probability of the recurrence of soft-errors in a short period is low enough, operations which are executed as retry and other operations which are executed simultaneously can share resources.

To use hardware resources more efficiently, a tripled data flow graph of a computation algorithm is partitioned into several connected subgraphs. However, the more comparison-operations are selected, the more subgraphs are partitioned. As a result, latency of the datapath improves because fine-grained subgraphs are relatively easier to fulfill the speculative resource sharing condition than coarse-grained ones. On the other hand, latency may become larger as increasing the number of comparison-operations. Thus, deciding insertions of comparison-operations is an important factor in design optimization.

In order to reduce an excessively applied fault-tolerance and mitigate time overhead for the executions of retry parts which are a disadvantage of comparison-retry (C-R)

schemes, the author introduces spatial/temporal adjacency constraint between datapath components considering a concept of localities of soft-errors. If a single soft-error has a spatial and temporal boundary, and its influence is limited against multiple component errors, several components can be executed at the same time. Majority-voting (M-V) schemes have a disadvantage that third copies should be always executed, while third copies in C-R schemes need not be executed as long as no error has occurred. Moreover, M-V mechanisms require more hardware resources although datapaths to which those schemes are implemented can achieve small latency. Because of introducing adjacency constraint, an M-V mechanism for error masking and correction instead of a C-R mechanism, and the three copies in every subgraphs can be executed concurrently. On the other hand, an advantage of C-R based error correction mechanisms is that the mechanism can reduce power consumption contributed by idling of retry parts, in case no error is detected. Nevertheless, the executions of retry parts cause time overhead, which is a drawback of the C-R mechanisms. In order to merge the advantages of both C-R schemes and M-V schemes, the author proposes a combination of the two error correction schemes to take advantage of the strengths of each scheme. In addition, a heuristic algorithm to find a latency-optimized integration of the two schemes is suggested.

It is found that the proposed method can reduce latency in several different applications without deterioration of reliability and chip area compared with a conventional C-R scheme. In addition, the experimental results show that the proposed method is more effective when a computation algorithm possesses higher parallelism and a small number of resources is available.

Key words: fault-tolerance, soft-error, multiple component error, high-level synthesis, datapath synthesis, datapath optimization, triple algorithm redundancy, concurrent error detection, comparison-retry scheme, majority-voting scheme, speculative resource sharing, adjacency constraint, mixed error correction scheme, check variable selection, integer linear programming.