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High-performance oxide thin film transistor fully fabricated by a direct rheology-imprinting

Phan Trong Tue,[1,2,a] Kazuhiro Fukada,[2] and Tatsuya Shimoda[1,2]
[1]School of Materials Science, Japan Advanced Institute of Science and Technology 1-1 Asahidai, Nomi-shi, Ishikawa 923-1211, Japan
[2]Japan Science and Technology Agency, ERATO Shimoda Nano-Liquid Process Project 2-13 Asahidai, Nomi-shi, Ishikawa 923-1211, Japan

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Operation of all oxide thin-film transistors fully fabricated by a direct rheology-imprinting technique was demonstrated. In the device, a highly conductive amorphous La-Ru-O ($8 \times 10^{-3}\,\Omega$ cm) was used as the gate and source/drain electrodes. Indium oxide and amorphous La-Zr-O were utilized as the semiconducting channel and gate insulator, respectively. Silsesquioxane-based SiO_2 was used both as a mask and as a passivation layer for the channel. The obtained "on/off" current ratio, field-effect mobility, threshold voltage, and subthreshold swing factor were approximately 10^7, 8.4 $cm^2\,V^{-1}\,s^{-1}$, −0.18 V, and 80 mV/decade, respectively. *Published by AIP Publishing.*
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Among various solution-based approaches, direct printing is a promising low-cost technique for fabricating oxide thin-film transistors (TFTs). The printing technique offers several advantages in manufacturing electronics such as a direct writing of materials, reduction of material waste, and reproducibility with a high-resolution, which are not affordable by other solution-based approaches.[1–6] While many printed organic TFTs have been reported,[1,2,4,5] relatively few studies, associated with directly printed oxide TFTs, have been pursued.[7–9] In addition, previous works have mainly been focused on printing of metal oxide semiconductors as the channel layer, while other layers such as gate, source/drain (S/D) electrodes, and channel etch stopper/passivation were fabricated by other techniques. Ultimately, in order to inherit advantages of direct printing, oxide TFTs should totally be printed.

In a previous report, we introduced a printing method, so-called nano-rheology imprinting (nRIP) for metal-oxide patterns within the sub-micrometer range.[10] The nRIP method, which is a type of direct thermal imprinting, uses the rheological properties of oxide precursor gels that are imprinted at an elevated temperature. We have reported the nRIP-TFTs with a sub-micrometer channel length.[10] However, the materials, device structure, and fabrication process still have several limitations. First, the TFT channel area was defined by dry-etching with the top-contact S/D electrode as a mask. This means that the channel was directly exposed to the etching plasma, resulting in its severe damage. Second, without a channel passivation, the device experienced unstable operation due to absorptions of either water or oxygen molecules in the air ambient on the channel surface. One possible solution is to use a material that plays a dual role as a hard mask for channel patterning and as a passivation layer. In this regard, silsesquioxane-based SiO_2 appears as a good candidate because of its high plastic deformation ability, which is beneficial for nRIP patternability and its good passivation properties.[11] Third, the RuO_2 and amorphous In-Zn-O films were used as the S/D electrodes and the channel layer, respectively, leading to a poor ohmic contact owing to a large difference in their work functions. In order to improve the contact, insertion of a highly conductive indium-tin-oxide (ITO) layer inbetween the S/D electrodes and channel layer would be effective. Fourth, the TFT structure exhibits poor downscaling ability because the RuO_2 electrodes would be broken during sintering because of its crystallization and grain growth. In this case, the use of an amorphous material may help to avoid the breaking caused by crystallization. One possible amorphous oxide material that also has high conductivity is LaRuO (LRO).[12] It was found that the plastic deformation ability was greatly improved by adding La to Ru to allow for the formation of a nano-sized gel pattern by nRIP (nRIP-LRO). The gel pattern was converted to an amorphous LRO structure without breaking during sintering. As a result, a nRIP-LRO narrow line with a width of a few tens of nanometers, which can be utilized as electrodes in TFTs,[13] was able to be achieved. According to these considerations, in the present work, we propose oxide materials and device structures to boost up the device performance. In particular, nRIP-LRO was utilized for both gate and S/D electrode patterns. In order to improve the conductivity of the gate electrode and the ohmic contact between the S/D and channel layer, spin-coated RuO_2 and ITO thin layers were inserted to fabricate the LRO/RuO_2 and LRO/ITO stacked structure for the gate and S/D electrodes, respectively. Silsesquioxane-based SiO_2 was patterned by nRIP (nRIP-SiO_2) for channel masking and passivation. As a result, oxide TFTs could be fully printed by the direct nRIP method in air ambient. High performance nRIP-TFTs was achieved with an "on/off" current ratio, a subthreshold swing (S) factor, and a channel mobility (μ) of approximately 10^7, 80 mV/decade, and 8.4 $cm^2\,V^{-1}\,s^{-1}$, respectively. The device also exhibited stable operation when stored in air ambient.

A schematic of the device fabrication process is described in Fig. 1. A bottom-gate bottom-contact TFT

[a]Author to whom correspondence should be addressed: phan-tt@jaist.ac.jp

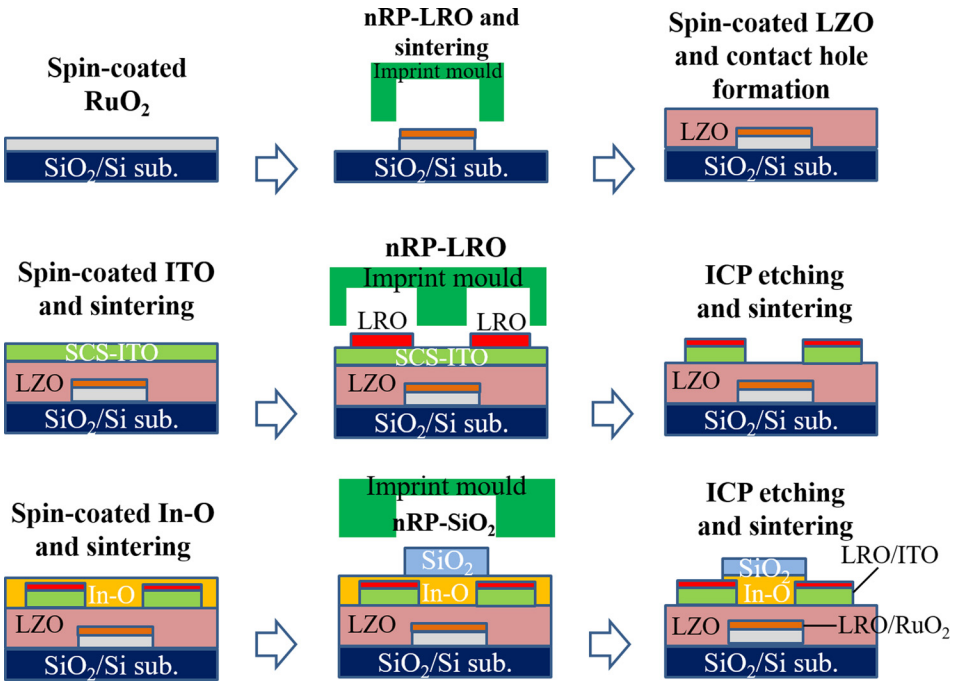

FIG. 1. Fabrication process of nRP-oxide TFTs.

structure was used. For the gate electrode, a RuO_2 layer was formed by spin-coating on a SiO_2/Si substrate. Then, LRO (La/Ru = 50/50) was patterned by nRIP followed by physical dry-etching and sintering. In detail, first, the LRO gel film was prepared by spin-coating the LRO precursor (0.35 mol/kg) onto the RuO_2/SiO_2/Si substrate at 1500 rpm, followed by drying at 100 °C in air. Second, demoulding treatment was conducted on the mould and the sample surface by using the silane coupling agent HD-1100TH (Daikin Industries). A Si mould with gate electrode patterns was used. Third, the sample was imprinted at a pressure of 20 MPa at 175 °C for 5 min by using the nanoimprint apparatus ST-50 (Toshiba machine). Finally, demoulding was performed at 100 °C. For the gate insulator, an amorphous La-Zr-O (La/Zr = 1/1) film was formed by spin-coating followed by contact hole patterning and sintering. For the S/D electrodes, first, the combustion-synthesized ITO layer was spin-coated, followed by an annealing at 500 °C. Next, LRO was patterned by nRIP using the same conditions as for the LRO gate electrode. The channel layer was formed by spin-coating In_2O_3 precursor solution (0.2 mol/kg) followed by annealing. The channel resistivity and carrier density were approximately 1.2 Ω cm and 2.0×10^{18} cm^{-3}, respectively. After that, the silsesquioxane-based SiO_2 ($[R\text{-}SiO_{3/2}]_n$, S05-018 product with a molecular weight of 1800 from AZ Electronic Materials Corp., Japan) passivation layer was patterned by nRIP (nRIP-SiO_2) in the same manner as done for the LRO but with different imprinted and demoulding temperatures of 210 and 50 °C, respectively. The details of the processing condition and time for the demoulding treatment before nRIP are described in the supplementary material. The nRIP-SiO_2 pattern was subsequently used as a hard mask for patterning the channel area. A summary of the materials, film processing conditions, and thickness of each layer of the fabricated nRIP-oxide TFT is given in the supplementary material (Table S1). More details of the material precursor solution design, nRIP process, sintering conditions, and their characterization can be found in our previous reports[10,13–17] and the supplementary material (Figs. S1–S6).

Figure 2 shows the optical microscopy images of the fabricated nRIP-oxide TFT array (24 × 24 transistors) corresponding to the gate electrode and contact holes [Fig. 2(a)], S/D drain electrodes [Fig. 2(b)], and channel/passivation patterns [Fig. 2(c)]. All patterns were well-defined and faithful to the nRIP mould design with a high alignment accuracy and uniformity over a large area of 20×20 mm^2. Optical microscopy images and thickness profiles of the nRIP mould before and after nRIP are shown in Fig. S7 (supplementary material), which confirm that the nRIP process is not based on a layer transfer but a plastic deformation. The shrinkage percentage of nRIP-LRO and nRIP-SiO_2 before and after

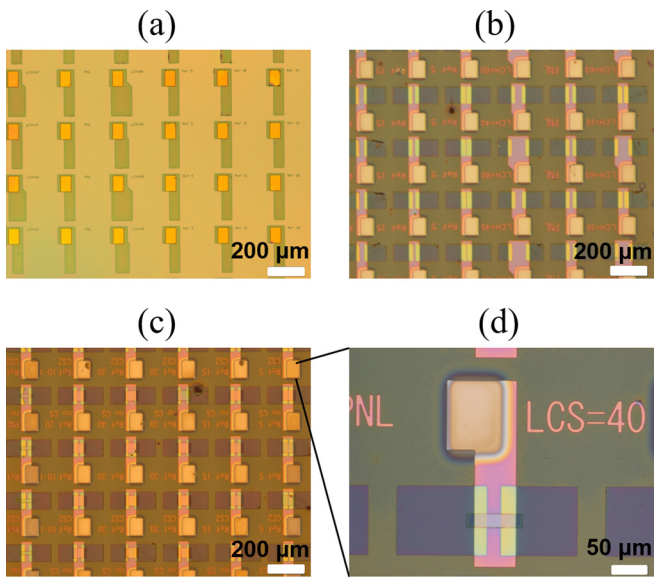

FIG. 2. (a) Gate electrode and contact hole patterns, (b) S/D patterns, (c) passivation/channel patterns, and (d) a fabricated nRP-TFT with W/L = 120/40 μm.

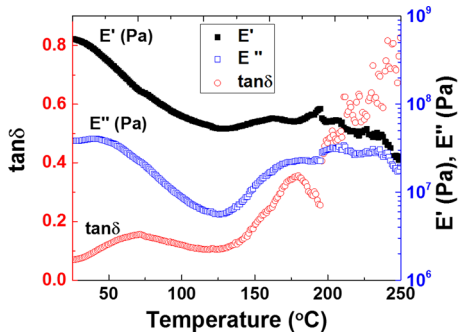

FIG. 3. Viscoelastic property of the silsesquioxane gel. The G' and G'' values represent the elastic and viscous moduli, respectively, and $\tan\delta$ is the ratio of G'' to G'.

sintering was found to be less than 10% in the lateral direction (Figs. S8–S10, supplementary material).

The silsesquioxane has cage-like or polymeric structures with Si-O-Si linkages and tetrahedral Si vertices. The molecules are unusual because they feature an inorganic silicate core and an organic exterior, which are similar to metal-acetylacetonate cases to some extent. The silica core confers rigidity and thermal stability, whereas the organic shell allows imprinting feasible. The viscoelastic properties of the silsesquioxane gel were measured using a rheometer UBM E-4000-DVE (UBM corporation) in a tensile mode to confirm the softening phenomenon and to evaluate the viscoelastic transformation temperature. A viscoelastic transformation, which is similar to a glass transition, was clearly observed (Fig. 3). In particular, the silsesquioxane gel had $\tan\delta$ values that increased from 120 °C and peaked at approximately 180 °C, which indicated that the gel was more easily softened at the peak temperature. When the gel is imprinted, a softening phenomenon occurs at a certain temperature during heating, thereby allowing the semi-solid to be "rheologically imprinted". The dramatic softening of the semi-solid gel means a decrease in the cohesion force of the imprinted material, which could be brought about by decomposition and gasification of the organic shell of the metal-oxide network. Generated organic gases would further decrease the cohesion forces by passing through the structure to the outside. As a result, dramatic softening like an avalanche occurs, which also causes the metal oxide condensation in imprinting. By selecting appropriate metal-organic precursors whose gel states undergo a viscoelastic transformation during heating at a certain pressure, similar to a glass transition, it was able to fabricate well-defined patterns without the significant deformation of imprinted features during post-annealing.[10] This made our approach distinct from common imprinting techniques that generally experience a large shrinkage of patterns during the post-annealing.[18,19]

Figure 4(a) shows atomic force microscopy (AFM) images of a typical nRIP-oxide TFT. The inset shows a surface line profile across the S/D and channel layers. At the magnification, sharp patterns and clean surfaces without residues were able to be achieved by the nRIP and etching processes. The thicknesses of the S/D and channel/passivation layers were found to be 110 nm and 305 nm, respectively. Figure 4(b) presents a high-resolution transmission electron microscopy (HRTEM) image and elemental distribution microscopy image measured across the InO/LZO interface region. An atomically flat In_2O_3 channel/LZO insulator interface was obtained with almost neither void nor defect formation. This clean and flat interface would provide a good channel for electron transportation, and hence, enhanced TFT performance is expected due to a less electron carrier scattering. The elemental distribution image suggests a highly dense and uniform structure throughout the LZO layer. Figure 4(c) shows a depth line profile across the In_2O_3/LZO interface region, indicating that the thicknesses of the In_2O_3 and LZO layers were approximately 20 nm and 100 nm, respectively. The achieved constant line profile revealed uniform composition distribution across the whole structure. Elemental interdiffusion was not observed

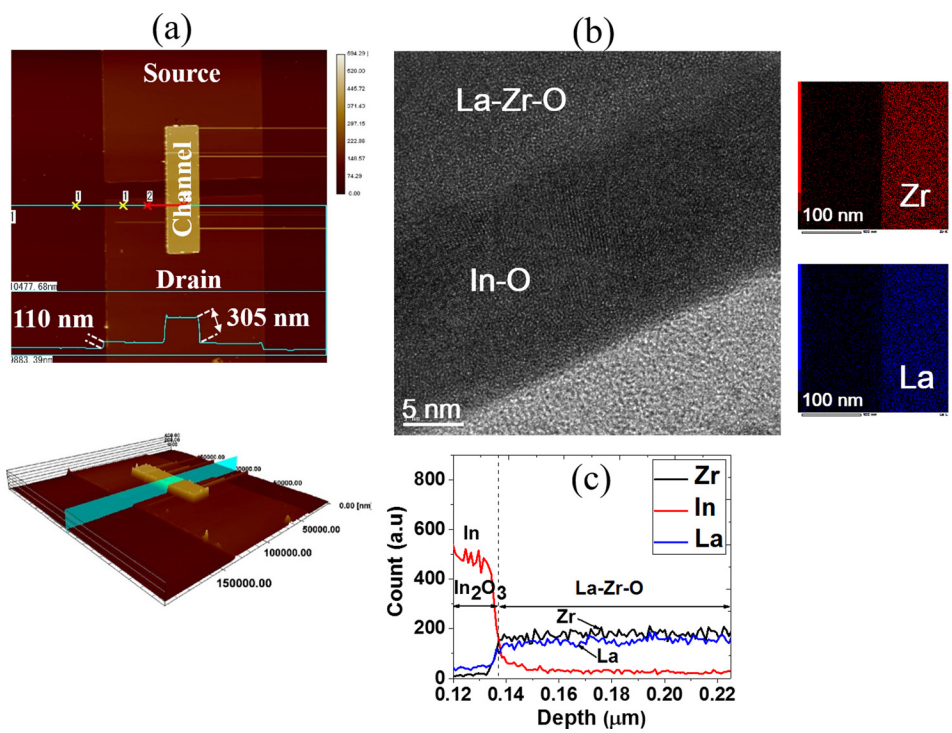

FIG. 4. (a) AFM images of the fabricated nRP-TFT with W/L = 120/40 μm, (b) HRTEM image and elemental analysis at the In_2O_3/LZO interface, and (c) Depth profile across the In_2O_3/LZO region.

across the interface, which is in a good agreement with the HRTEM analysis. The La/Zr elemental ratio was almost 1/1 and remained consistent in the whole LZO layer, which is the same as the designed molar ratio of La and Zr in the precursor solution.

Figure 5 shows transfer and output characteristics of the fabricated nRIP-oxide TFTs with the channel width (W) of 60 μm and different channel lengths (L) from 5 to 50 μm measured at a drain voltage (V_D) of 1.5 V. Typical n-type characteristics were observed for all devices [Fig. 5(a)]. With the increase in L, the saturated "on" current decreased, while the "off" current, threshold voltage, and subthreshold swing (SS) factor remained almost constant. The SS-factor and channel mobility (μ) were determined empirically from the transfer and output characteristics using the following equations:

$$SS = \frac{dV_G}{d(\log I_D)}, \tag{1}$$

$$I_D = \frac{1}{2}\mu C \frac{W}{L}(V_G - V_T)^2, \tag{2}$$

where C is the capacitance per unit gate area and V_G and V_T are the applied gate voltage and threshold voltage, respectively.

The obtained "on/off" current ratio, SS-factor, and μ were 10^7, 80 mV/decade, and 8.4 $cm^2\ V^{-1}\,s^{-1}$, respectively. The small SS-factor and high μ could be attributed to good channel/insulator interface properties.[20] A relatively large "off" current was caused by the gate to source leakage current since the high-k LZO was used as the gate insulator. The leakage current issue would be resolved by optimizing the La/Zr molar ratio and film processing (solvothermal treatment and UV/ozone assisted annealing) for their precursor solutions and gel films, respectively. The details of LZO optimization for TFT application would be published elsewhere.[21] In addition, a hysteresis loop of approximately 2.0 V was observed in the transfer curves. This value is similar to that of other solution-processed oxide TFTs reported in literatures.[22] The hysteresis might be originated from defects and/or impurities existing in the both channel and insulator layers.[16] The output characteristics of the fabricated device exhibited a linear characteristic at small V_D and saturated characteristic as V_D exceeded V_G [Fig. 5(b)]. The contact resistance (R_c) between the In_2O_3 channel and S/D electrodes was estimated by transmission-line measurements (TLMs) using the patterns with varying channel lengths as shown in Fig. S11 (supplementary material). The normalized

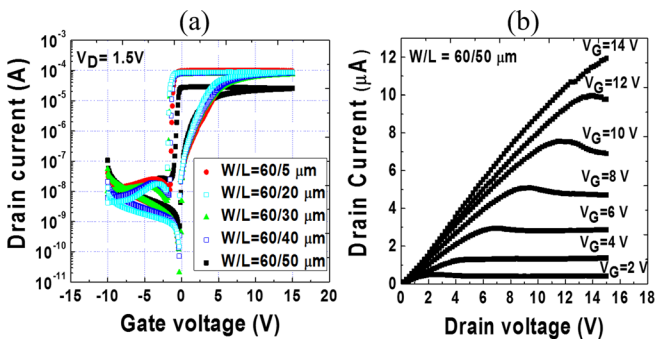

FIG. 5. (a) Transfer and (b) output characteristics of the fabricated nRP-TFT.

R_c values of the devices based on the channel width with and without the ITO buffer layer were approximately 64 kΩ and 158 kΩ μm, respectively. These values agree with the reported ones for the common metal and metal oxide contact in oxide-based TFTs.[23] The result indicated that an improved ohmic contact was achieved by the insertion of the ITO buffer layer. A decrease in the saturated current might be related to the insufficient conductivity of the S/D electrode. However, further investigation is needed to confirm this phenomenon. Finally, the operation stability was tested by measuring the transfer characteristic without post-annealing after 60-day-storage under atmospheric air ambient. A negligible change in the transfer characteristic was observed, indicating that the fabricated device is resistant to effects from the ambient such as water and oxygen absorption[24] (Fig. S12, supplementary material). This implies that the SiO_2 layer is effective for passivating the oxide channel surface.

In conclusion, we report on fabrication and characterization of oxide TFTs by using all nRIP processes in air ambient. Operation of the fabricated device was confirmed with the "on/off" current ratio, S-factor, and μ of approximately 10^7, 80 mV/decade, and 8.4 $cm^2\ V^{-1}\,s^{-1}$, respectively. The improved performance of the nRIP-TFT could be achieved due to: (1) The integration of the silsesquioxane-based SiO_2 layer which had good nRIP pattern-ability and played dual roles as masking materials and passivation. (2) The use of highly conductive amorphous LRO for gate and S/D electrode patterning, which could avoid pattern breaking during sintering. (3) In contrast to the top-contact TFT structure, the bottom-contact ones allowed for more uniform S/D patterns to be printed on a flat insulator layer. The proposed nRIP-oxide TFTs would be interesting for low-cost, high-density, and large-area printed electronics such as flat-panel display and field-effect-transistor based sensor applications.

See supplementary material for additional information about characterization (TG-DTA, XRD, electrical conductivity, etching rate, etc.) of oxide materials used in this work, such as LRO and SiO_2 thin films. It also shows optimization of nRP process for the silsesquioxane (SiO_2) material. In addition, data of contact resistance and TFT stability are also provided.

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[1]A. C. Arias, S. E. Ready, R. Lujan, W. S. Wong, K. E. Paul, A. Salleo, M. L. Chabinyc, R. Apte, R. A. Street, Y. Wu, P. Liu, and B. Ong, Appl. Phys. Lett. **85**(15), 3304 (2004).
[2]K. E. Paul, W. S. Wong, S. E. Ready, and R. A. Street, Appl. Phys. Lett. **83**(10), 2070 (2003).
[3]T. Shimoda, Y. Matsuki, M. Furusawa, T. Aoki, I. Yudasaka, H. Tanaka, H. Iwasawa, D. Wang, M. Miyasaka, and Y. Takeuchi, Nature **440**(7085), 783 (2006).
[4]H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, Science **290**(5499), 2123 (2000).
[5]J. Z. Wang, Z. H. Zheng, H. W. Li, W. T. S. Huck, and H. Sirringhaus, Nat. Mater. **3**(3), 171 (2004).

[6]P. Beecher, P. Servati, A. Rozhin, A. Colli, V. Scardaci, S. Pisana, T. Hasan, A. J. Flewitt, J. Robertson, G. W. Hsieh, F. M. Li, A. Nathan, A. C. Ferrari, and W. I. Milne, J. Appl. Phys. **102**(4), 043710 (2007).
[7]D. H. Lee, Y. J. Chang, G. S. Herman, and C. H. Chang, Adv. Mater. **19**(6), 843 (2007).
[8]Y. Nakamura, S. Matsumoto, S. Arae, Y. Sone, and Y. Hirano, Ricoh Technical Report No. 39 (2014), p. 07.
[9]D. Kim, Y. Jeong, K. Song, S.-K. Park, G. Cao, and J. Moon, Langmuir **25**(18), 11149 (2009).
[10]T. Kaneda, D. Hirose, T. Miyasako, P. T. Tue, Y. Murakami, S. Kohara, J. Li, T. Mitani, E. Tokumitsu, and T. Shimoda, J. Mater. Chem. C **2**(1), 40 (2014).
[11]M. Janeta, L. John, J. Ejfler, and S. Szafert, RSC Adv. **5**(88), 72340 (2015).
[12]J. Li, E. Tokumitsu, M. Koyano, T. Mitani, and T. Shimoda, Appl. Phys. Lett. **101**(13), 132104 (2012).
[13]K. Nagahara, D. Hirose, J. Li, J. Mihara, and T. Shimoda, Ceramics Int. **42**(6), 7730 (2016).
[14]P. T. Tue, J. Li, T. Miyasako, S. Inoue, and T. Shimoda, IEEE Electron Dev. Lett. **34**(12), 1536 (2013).
[15]Y. Murakami, J. Li, D. Hirose, S. Kohara, and T. Shimoda, J. Mater. Chem. C **3**(17), 4490 (2015).
[16]P. T. Tue, S. Inoue, Y. Takamura, and T. Shimoda, Appl. Phys. A **122**(6), 623 (2016).
[17]P. T. Tue, T. Miyasako, J. Li, H. T. C. Tu, S. Inoue, E. Tokumitsu, and T. Shimoda, IEEE Trans. Electron Devices **60**(1), 320 (2013).
[18]O. F. Göbel, M. Nedelcu, and U. Steiner, Adv. Funct. Mater. **17**(7), 1131 (2007).
[19]R. Ganesan, J. Dumond, M. S. M. Saifullah, S. H. Lim, H. Hussain, and H. Y. Low, ACS Nano **6**(2), 1494 (2012).
[20]S.-H. K. Park, C.-S. Hwang, D.-H. Cho, S. M. Yoon, S. Yang, C. Byun, M. Ryu, J.-I. Lee, O. S. Kwon, W.-S. Cheong, H. Y. Chu, and K. I. Cho, .SID Symp. Dig. Tech. Pap. **40**(1), 276 (2009).
[21]J. Li, P. Zhu, P. T. Tue, S. Inoue, and T. Shimoda, "Hybrid cluster precursors of the LaZrO insulator for transistors: lowering the processing temperature," J. Mater. Chem. C (submitted)
[22]W. Xu, D. Liu, H. Wang, L. Ye, Q. Miao, and J.-B. Xu, Appl. Phys. Lett. **104**(17), 173504 (2014).
[23]S. Y. Lee, Trans. Electr. Electron. Mater. **16**(3), 139 (2015).
[24]J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, Appl. Phys. Lett. **93**(12), 123508 (2008).