A study on a Wave-Pipeline processor involves feedback circuits

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Abstract

Clock period minimization is one of the most important problem for processor design.

The Wave-Pipeline, is not required that synchronous clock timing on each latch, so that clock period can be shorter drastically. However, most circuits with feedbacks causes difficult clock scheduling problem.

Otherwise, the Semi-Synchronous circuit is proposed for physical placement and routing in LSI design. Semi-Synchronous circuits and Wave-Pipeline circuits have the same feature that is not required synchronous clock timing constraint. This paper presents the Semi-Synchronous Pipeline which introduces Semi-Synchronous circuits design technique to Wave-Pipeline circuits.

1 Introduction

Both Semi-Synchronous circuits and Wave Pipeline circuits do not required synchronous clock timeng for each latch. Wave-Pipeline that involves feedbacks circuits such as forwarding unit can be regarded as Semi-Synchronous circuits. In this paper, the author proposes Semi-Synchronous Pipeline which shorten clock period by inserting delay buffers and dividing pipeline stages.

2 Semi-Synchronous Pipeline

Wave Pipeline is a kind of Pipeline that does not require each latch synchronous. Semi-Synchronous circuits shorten clock period by inserting delay intentially to the clock tree. The author conbining two circuit design concepts, Wave-Pipline and Semi-Synchronous circuits.

3 Behavior of Semi-Synchronous Pipeline

Semi-Synchronous Pipeline has constraints of delay between latches. Constraint graph is able to be constructed by these constraints.

4 How to design of Semi-Synchronous circuit

The author proposes an algorithm of Semi-Synchronous Pipeline design. Also, the author shows buffer insertion algorithm to shorten delay difference between each latches.

5 A trial design of Semi-Synchronous Pipeline Processor, WAVIST

The author designed a tiny processor named **WAVIST** because of verification of Semi-synchronous Pipeline. **WAVIST** is a 8bit RISC Pipeline Processor, with basic instructions, movement data operations between memories and registers, arithmetic operations, logical operations, and jump operations.

The author applied Semi-Synchronization algorithm to **WAVIST**. Experimental results shows that clock period is improved down to 77.3%.