Analysis of steep switching characteristics in graphene tunnel field effect transistors for application to the low power circuit

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1. Introduction

Tunnel field effect transistors (TFETs) have been studied as a promising candidate for the beyond CMOS era devices due to their low OFF current and a possibility of the subthreshold swing (SS) below 60 mV/dec at the room temperature. Recently, TFETs based on various semiconductors have been demonstrated and some TFETs achieved *SS* of less than 60 mV/dec with high ON/OFF ratio [1]. However, these TFETs could not achieve sufficiently high ON current (2 orders smaller than conventional MOSFET) due to the high tunnel resistance and low carrier mobility. To tackle this low ON current issue, graphene has been proposed as the channel material [2]. The low effective mass and atomically thin body result in extremely high carrier mobility, and a finite band gap can be realized by controlling the width of the graphene nanoribbon (GNR). However, the design guideline of device structure has not been reported because the studies of GTFETs is still in the early stages.

2. Objective

In this work, we aim to clarify the essential factors of device characteristics from the atomic scale, and also clarify the requirements to achieve high device performance: SS < 60 mV/dec and ON/OFF ratio > 10^8 at the room temperature. Moreover, I develop the compact model and then evaluate the logic circuit performance when applying the GTFETs.

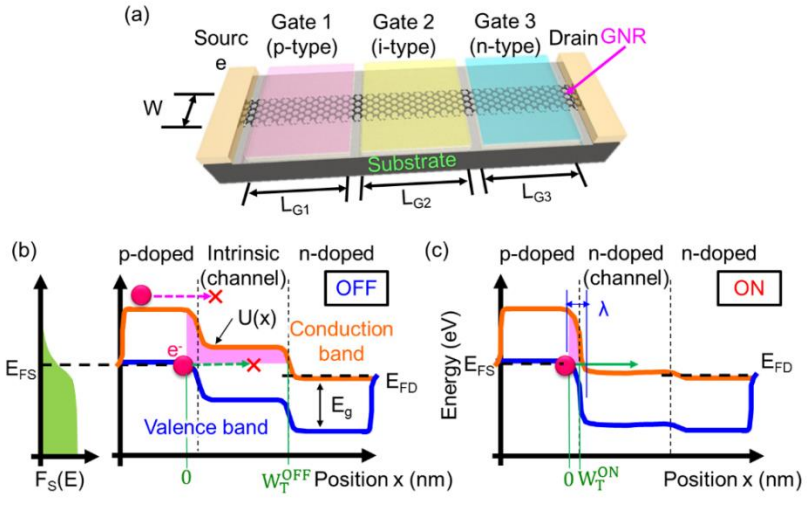

Fig. 1 Schematic of the triple-top gate graphene TFET structure. Potential diagram of the GFET in the (b) OFF state and (c) ON state. W_T, λ and U(x) are the tunneling length, the screening length in tunnel junction and the potential profile, respectively. Pink shaded areas show the potential barrier experienced by charge carriers at the upper end of the bias window. $E_{FS/D}$ and F_s(E) are the Femi energy in each electrode and the Fermi distribution function of the source side.

3. Computation method and device structure

Schematic of GTFETs structure is shown in Fig. 1. Generally, the TFETs consists of p-doped, channel and n-doped regions (Fig. 1a). In the OFF state, the source to drain direct tunneling (S-D tunneling) leakage is exponentially decreased in the channel region (Fig. 1b). The thermionic leakage current is decreased by the p-doped region. At the ON state, the band-to-band tunneling (BTBT) will occur and it leads to an abrupt switching (Fig. 1c). In order to form the p-i-n junction, the electrostatic doping method is necessary and therefore we chose the triple-top gate structure [3].

We used the self-consistent NEGF simulations based on the Slater-Koster tight-binding (SKTB) model that is implemented in the AtomistixToolKit (ATK). All the calculations assume ballistic transport.

4. Results and discussion

Source-drain bias voltage dependence of device characteristic is shown in Fig. 2. The analyzed structure has 0.9 nm wide GNR and 10 nm long gate length. For this calculation, I choose the gate 1 voltage so that the BTBT occurs at the Fermi-energy of the source side. The ON current of 1282.1 μA/μm, OFF current of <1pA/μm and ON/OFF ratio of 7×10^9 are achieved at V_{DS} = 0.5 V (Fig. 2a to 2c). The SS of 28.5 mV/dec is achieved. Focus on the V_{DS} dependence of *SS*, the *SS* is found to be relatively stable at $V_{DS} \geqq 2k_BT$ and drastically increases below $2k_BT$ (Fig. 2d). It is attributed to the difference of the quasi-Fermi energy in source and drain. When the bias voltage is large, F_{DS} (= F_S(E) - F_D(E), $F_{S/D}$(E) is the Fermi distribution function in the source and drain regions) in the tunneling energy window is almost 0.5 due to the weak influence from the drain side. Whereas, when the bias voltage is small, the Fermi distribution functions overlap, leading to a decrease in F_{DS}. As a result, the ON current decreases with decreasing V_{DS}, and consequently, the *SS* increases rapidly at the low bias voltage. Furthermore, I developed an analytical model and it shows good agreement with the extracted *SS* values (red line in Fig. 2d).

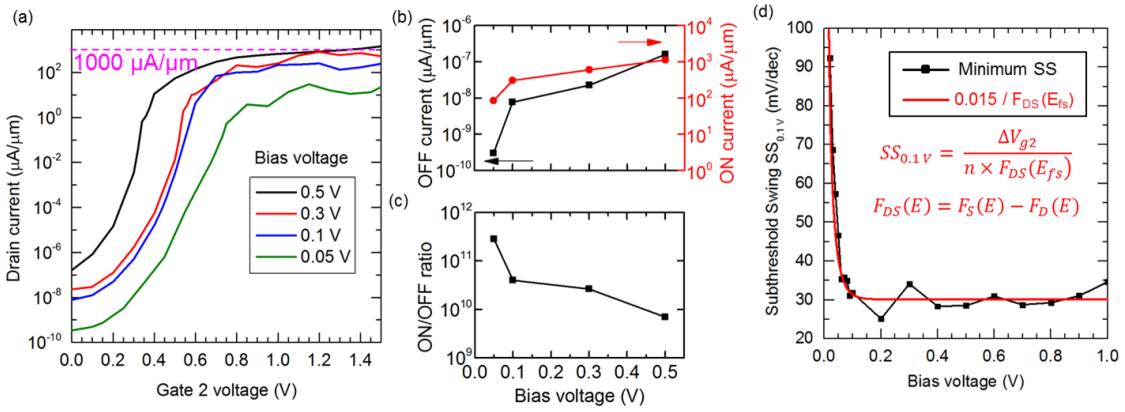

Fig. 2 Source-drain bias dependence of device characteristics. (a) Transfer characteristics at different bias voltages. Bias voltage dependence of (b) OFF and ON currents, (c) ON/OFF ratio. (d) The subthreshold swing as a function of bias voltage.

In order to clarify the requirement of device dimensions for abrupt *SS*, I developed the analytical model of *SS* which including the influence of the S-D tunneling and thermionic leakage (Fig. 3). This analytical model well reproduces the experimental result [4] (Fig. 3a). The Requirement for SS < 60 mV/dec at room temperature is shown in Fig. 3b. This result shows that requirements of device dimension to achieve the SS < 60 mV/dec are as follows: the GNR width ≦ 8.6 nm and channel length ≧ 43 nm. Moreover, to achieve the ON/OFF ratio of 10^8, GNR with ≧ 420 meV and channel length ≧ 50 nm is needed. The limitation of the band gap depends on the thermionic leakage, whereas, the channel length limitation is determined by the S-D tunneling leakage.

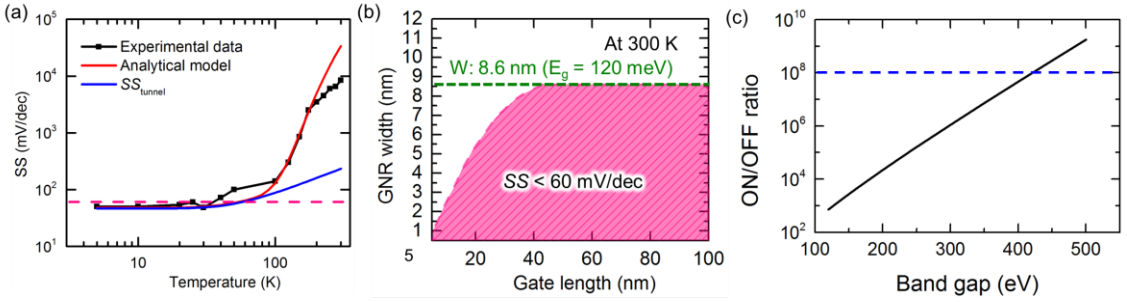

Fig. 3 Requirement of device dimension. (a) Comparison of the developed analytical model and experimental result. (b) Requirement for steep SS. (c) ON/OFF ratio as a function of band gap. In this analysis, S-D tunneling significantly smaller than thermionic leakage.

Fig.4 shows the energy consumption as a function of circuit delay. This analysis utilizes the Smart Spice with Verilog-A code. As a result, GTFETs give two-order smaller energy consumption than conventional MOSFET and spin devices with the delay of less than 1 psec.

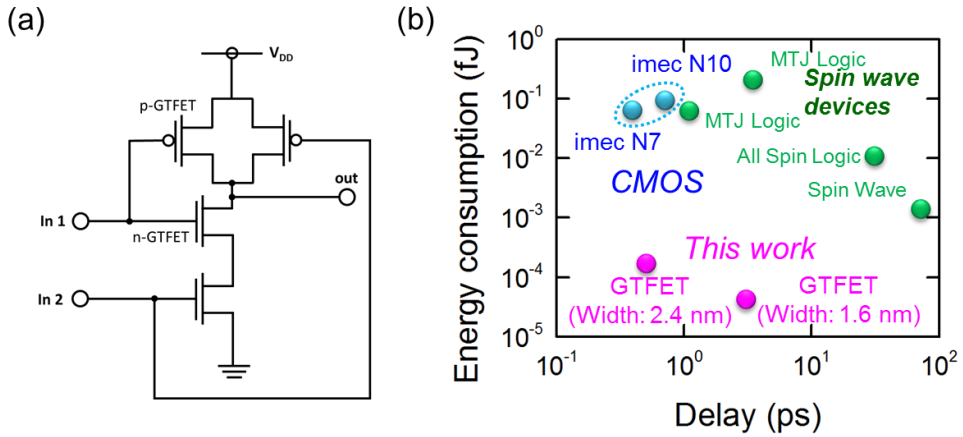

Fig. 4 Energy consumption and delay in NAND. (a) NAND circuit model. (b) Comparison of GTFETs and conventional devices.

5. Research significance

The studies of GTFETs is still in the early stages. Hammam *et al*. successfully demonstrated experimentally the BTBT in the GTFET with triple-top gate. They observed the *SS* of 50 mV/dec at *T* = 10 K. Furthermore, the band gap of 70 meV is not sufficient to realize the *SS* < 60 mV/dec at room

temperature and thus the narrower GNR is needed. However, the requirement of device dimension for the sub-thermal switching has not been reported. In addition, the performance of the logic circuit with GTFETs has not been understood yet.

This work revealed the device characteristics of GTFET and requirements of device dimension. Moreover, the performance of the logic circuit with GTFETs is evaluated. These results are important in order to fully exploit the potential of the GTFET and is expected to contribute further to the development of beyond CMOS ultra-low-power circuits.

Reference

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Publication

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Conference

1. S. Suzuki, A. M. M. Hammam, M. E. Schmidt, M. Muruganathan and H. Mizuta, Scaling effect on device performance in graphene tunnel field effect transistors**,** IEEE NANO, 168, Cork, Ireland, July. 2018. (Including peer review)
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