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Description	

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Progression of rapid potential-induced degradation of n-type single-crystalline silicon photovoltaic modules

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This study addresses the progression of potential-induced degradation (PID) of photovoltaic modules using n-type single-crystalline silicon cells. In a PID test in which a voltage of −1000 V was applied to the cells, the modules started to degrade within 10 s, and degradation saturated within 120 s, suggesting that PID is caused by positive charge accumulation in the front passivation films. We propose that these positive charges originate from positively charged K centers formed by extracting electrons from K centers, which explains the rapid degradation and its saturation behavior. We obtained some simulated and experimental results supporting this hypothesis.

Front-emitter, n-type crystalline silicon (c-Si)-wafer-based photovoltaic (PV) cells have recently attracted attention owing to their potential for achieving high efficiencies.[1–3] The solar cells have an n-type base, which has a high minority-carrier lifetime owing to the small capture cross sections of minority carriers; this causes them to have high open-circuit voltages (V_{oc}). Additionally, it is known that n-type c-Si wafers do not show light-induced degradation, which suggests n-type c-Si solar cells should be highly stable. Therefore, n-type front-emitter PV cells should be suitable for use in large-scale PV systems.

To ensure the long-term stability and high reliability of PV systems, it is important to understand the possible degradation behaviors of deployed PV modules. Potential-induced degradation (PID) has been identified as one of the most important reliability issues, especially in large-scale PV systems.[4–6] PID is associated with a high system voltage and occurs owing to high electric potential differences between the grounded frames and cells.

Hara *et al.*[7] have reported that under negative bias, n-type front-emitter PV modules undergo PID characterized by reductions in short-circuit current density (J_{sc}) and V_{oc}. Degradation is also reportedly caused by surface recombination of minority carriers and occurs readily even under a small voltage bias of −50 V or at room temperature.[7] The performance losses of PID-affected n-type front-emitter c-Si PV modules can be recovered by applying a positive bias,[7] which is also the case for conventional p-type c-Si PV modules[4]. However, to the best of our knowledge, a detailed time-dependent analysis of this type of degradation has not yet been reported. The findings of this study may therefore significantly improve not only our understanding of the time dependence but also of the PID mechanism itself.

In this letter, we report the time dependence of the PID of n-type front-emitter single-crystalline Si (sc-Si) PV modules using a rapid indoor PID test. Additionally, we also discuss the mechanism of this PID on the basis of the obtained results.

Commercial n-type, front-emitter sc-Si solar cells that contain silicon nitride (SiN_x)/silicon dioxide (SiO_2) passivation stacks and a diffused p^+ front emitter were cleaved into 20 × 20 mm^2 sized pieces. Interconnector ribbons were soldered onto the busbars of the front and rear silver electrodes. We prepared PV modules composed of conventional tempered cover glass/ethylene-vinyl acetate copolymer encapsulant/n-type cell/ethylene-vinyl acetate copolymer encapsulant/typical backsheet [poly(vinyl

fluoride)/poly(ethylene terephthalate)/poly(vinyl fluoride)] in a module laminator. The lamination process used in this study was the same as that used in a previous study.[8] The cover glass had a size of 45 × 45 mm^2 and contained alkali metals such as sodium.

The PID tests were performed by applying a voltage of −1000 or −1500 V to shorted interconnector ribbons with respect to an aluminum plate placed on the cover glass of the modules in a dry chamber maintained at 85 °C and approximately 2% relative humidity. We carried out the PID tests for three identical modules under each condition. We use the term "PID stress" here to refer to such voltage and temperature stresses.

Current density–voltage (J–V) measurements were conducted under one sun illumination of the modules before and after the PID tests. J_{sc}, V_{oc}, fill factor (FF), and maximum output power (P_{max}) were obtained from the J–V data. External quantum efficiency (EQE) measurements were also carried out before and after the PID tests. In a preliminary experiment, we found that the PID of n-type front-emitter sc-Si PV modules strongly saturated within several minutes under a voltage of −1000 V and at a temperature of 85 °C. Based on this result, we performed short-time PID tests ranging from several seconds to several minutes to study the progression behavior of the degradation in detail.

Shown in Fig. 1 are the dependences of $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ of the n-type front-emitter sc-Si PV modules on PID-stress duration, where the subscript 0 indicates the initial value. $J_{sc}/J_{sc,0}$ and $V_{oc}/V_{oc,0}$ decrease as the PID-stress duration increases, resulting in a reduction in $P_{max}/P_{max,0}$. As shown in Fig. 2, these reductions are accompanied by a noteworthy reduction in EQE in the short wavelength region, indicating that the degradation is attributed to enhanced surface carrier recombination. Interestingly, the degradation occurs within 10 s and the reductions in all the parameters are strongly saturated within 120 s. Similar saturation behavior is also seen in the EQE in Fig. 2, suggesting a strong saturation of the enhancement of the surface recombination. In terms of long-term stability, the considerably rapid degradation may become an extremely important issue; however, it is even more important for understanding the degradation mechanism. The degradation of the n-type front-emitter sc-Si PV modules is conspicuously rapid even compared with that of conventional multicrystalline Si[9], amorphous Si thin-film[9], n-type rear-emitter c-Si[8], and Cu(In,Ga)Se_2 thin-film[9] PV modules (note that these previous results[8,9] were obtained from PID tests under the same conditions).

Naumann *et al*. have revealed that the PID of conventional p-type c-Si PV modules is limited by the drift of positive sodium ions (Na^+).[10,11] Similarly, it has been proposed that the degradation of n-type rear-emitter c-Si and $Cu(In,Ga)Se_2$ thin-film PV modules is likely caused by Na^+ drift.[8,9] On the basis of these previous findings, the extremely high degradation rate clearly indicates that the degradation is not associated with Na^+ drift—instead, it appears to be based on positive charge accumulation in the front passivation films. This is because the drift time for Na^+ across 80 nm SiN_x films is in the order of several tens of minutes[12]; diffusion-driven processes therefore cannot explain the extremely rapid degradation rate that is actually observed.

One candidate for the origin of the positive charges are K centers, which are dangling bonds of Si atoms backbonded to three N atoms.[13] There are neutral, positively charged, and negatively charged K centers (K^0, K^+, and K^-, respectively), typically with a surface density of several 10^{12} cm^{-2} in SiN_x deposited by plasma-enhanced chemical vapor deposition, and it is well known that the charge states of the K centers can be manipulated via externally applied voltages.[14,15] If electrons are extracted from these K^0 and K^- centers by high negative biases during the PID tests, the net charge of the passivation films is shifted toward a positive value. Positively charged states attract minority carriers, i.e., electrons, in the p^+ emitter and enhance recombination via surface states. The maximum number of K^+ centers is limited by the total number of K centers (K^0, K^+, and K^- centers), which may explain the saturation behavior of the degradation. K^+ centers with a density of several 10^{12} cm^{-2} can be formed within 120 s, because a leakage current with a current density of approximately 0.1 μA/cm^2 flows between the cells and Al plates during the PID tests and positive charges can be piled up on the front surface of the cells with a density of up to approximately 7.5×10^{13} cm^{-2} for 120 s. The leakage current density was calculated from the measured electric resistance between the Al plate placed on the cover glass and the cells. Note that just a fraction of the charges can contribute to charge accumulation in SiN_x films and most reach the silver electrode or the interconnector ribbon (owing to the electric field concentration), where they are neutralized.

We carried out a device simulation with the numerical simulation software PC1D 5.9[16] to confirm whether the expected surface positive charges with a surface density of several 10^{12} cm^{-2} could give rise to degradation that is characterized by drops in V_{oc} and J_{sc}

accompanied by a significant reduction in quantum efficiency in the short wavelength region. Figure 3 shows the calculated *J–V* data and internal quantum efficiencies (IQEs) with and without surface charges at densities of 2×10^{12} cm^{-2} and 4×10^{12} cm^{-2}. The values of the surface density in this calculation were set on the basis that a net positive charge of 4.6×10^{12} cm^{-2} was achieved by corona charging in a previous study[15]. Note that the densities of K centers in SiN_x films vary depending on the deposition conditions.[17] Our simulation included an n-type base doping of 3×10^{16} cm^{-3} and an emitter doping of 10^{19} cm^{-3}. The front-surface recombination velocity was set to 10^4 cm/s. As shown in panels (a) and (b) of Fig. 3, the cells with positive charges exhibited relatively large drops in V_{oc} and J_{sc} accompanied by a significant reduction in IQE in the short wavelength region, which is consistent with experimental results presented by Hara *et al*.[7] This indicates that the rapid degradation and subsequent degradation saturation can be consistently explained by assuming that positive charges originate from K^+ centers formed by extracting electrons from K^0 and K^- centers.

The SiO_2 films underlying the SiN_x films may play an important role in the charge accumulation process. In a previous study,[15] it was shown that externally injected positive charges in SiN_x films directly deposited on c-Si substrates dissipate via charge transfer between the SiN_x films and the substrates, sometimes within 10 min. Thin SiO_2 films prevent such charge transfer when inserted underneath the SiN_x films.[14,15] The SiO_2 films in our PV cells may therefore assist the SiN_x films to retain their positive charges. It is also possible that PID resistance is changed by modifying the properties of SiO_2 films or by exchanging them for other films, such as Al_2O_3 films[18].

On the basis of our hypothesis, the saturation value of the degradation should be independent of the applied voltage if the positive charges originate from the K^+ centers, because the number of positive charges is limited by the total number of K centers. To verify this, we performed PID tests under two different voltage conditions. As shown in Fig. 4, the degradation rate strongly depends on the voltage; by contrast, the saturation value of $P_{max}/P_{max,0}$ is unchanged even when the applied voltage was increased from −1000 to −1500 V. These findings are thoroughly consistent with our hypothesis.

We also performed a PID recovery test by applying a positive bias of +1000 V to a PV module degraded by a PID test where a negative bias of −1000 V was applied for 120 s. On

the basis of our hypothesis, degraded modules should completely recover their performance losses within several minutes, because the recovery process can also be thought of as a charge extraction process. As shown in Table I, the degraded module completely recovers its performance loss within 120 s. This result may support our hypothesis.

In summary, we have investigated the time dependence of the PID of n-type sc-Si PV modules. By using a PID test we found that PID of n-type front-emitter sc-Si PV modules occurs within 10 s and the reductions of all parameters are strongly saturated within 120 s. This very rapid degradation implies that the PID of n-type sc-Si PV modules is not associated with sodium drift but based on positive charge accumulation in the front passivation films. Assuming that the positive charge accumulation originates from K^+ centers formed by the extraction of electrons from K^0 and K^- centers, the rapid degradation and its saturation behavior can both be explained. The device simulation based on the hypothesis reproduces the actual degradation behavior reported in previous work. Moreover, the voltage-independent saturation value of P_{max} and the rapid recovery of the PID are consistent with our hypothesis. In future, we will investigate the correlation between the actual K center density in the front SiN_x films and the degree of degradation to further test our hypothesis.

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Figure Captions

Fig. 1. Dependences of $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF$_0$, and $P_{max}/P_{max,0}$ of the n-type front-emitter sc-Si PV modules on negative-bias PID-stress duration. The PID tests were performed in a dry environment, and the applied voltage and temperature during the PID tests were −1000 V and 85 °C, respectively. Each data point shows the mean value for three modules, and each error bar corresponds to the standard deviation of the mean. The solid lines are guides to the eye.

Fig. 2. EQEs of the n-type front-emitter sc-Si PV modules (a) before and after the PID tests for (b) 5 s, (c) 10 s, (d) 20 s, (e) 30 s, (f) 60 s, (g) 120 s, and (h) 180 s. The PID tests were performed by applying a voltage of −1000 V in a dry environment at 85 °C.

Fig. 3. PC1D-calculated one-sun-illuminated *J*–*V* (a) and IQE characteristics (b) of n-type front-emitter solar cells with and without positive surface-charges at densities of 2×10^{12} cm^{-2} and 4×10^{12} cm^{-2}.

Fig. 4. Dependence of the progression behavior of PID of n-type front-emitter sc-Si PV modules on the applied voltage. The tests were performed in a dry environment at 85 °C. Each data point shows the mean value for three modules, and each error bar corresponds to the standard deviation of the mean. The solid lines are guides to the eye.

Table I. $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, FF/FF_0, and $P_{max}/P_{max,0}$ of the n-type front-emitter sc-Si PV module after the PID test where a negative voltage of −1000 V was applied for 120 s and those after the following recovery test where a positive voltage of +1000 V was applied for 120 s.

Condition	$J_{sc}/J_{sc,0}$	$V_{oc}/V_{oc,0}$	FF/FF_0	$P_{max}/P_{max,0}$
After PID test	0.90	0.95	1.01	0.87
After recovery test	1.01	1.00	1.00	1.01

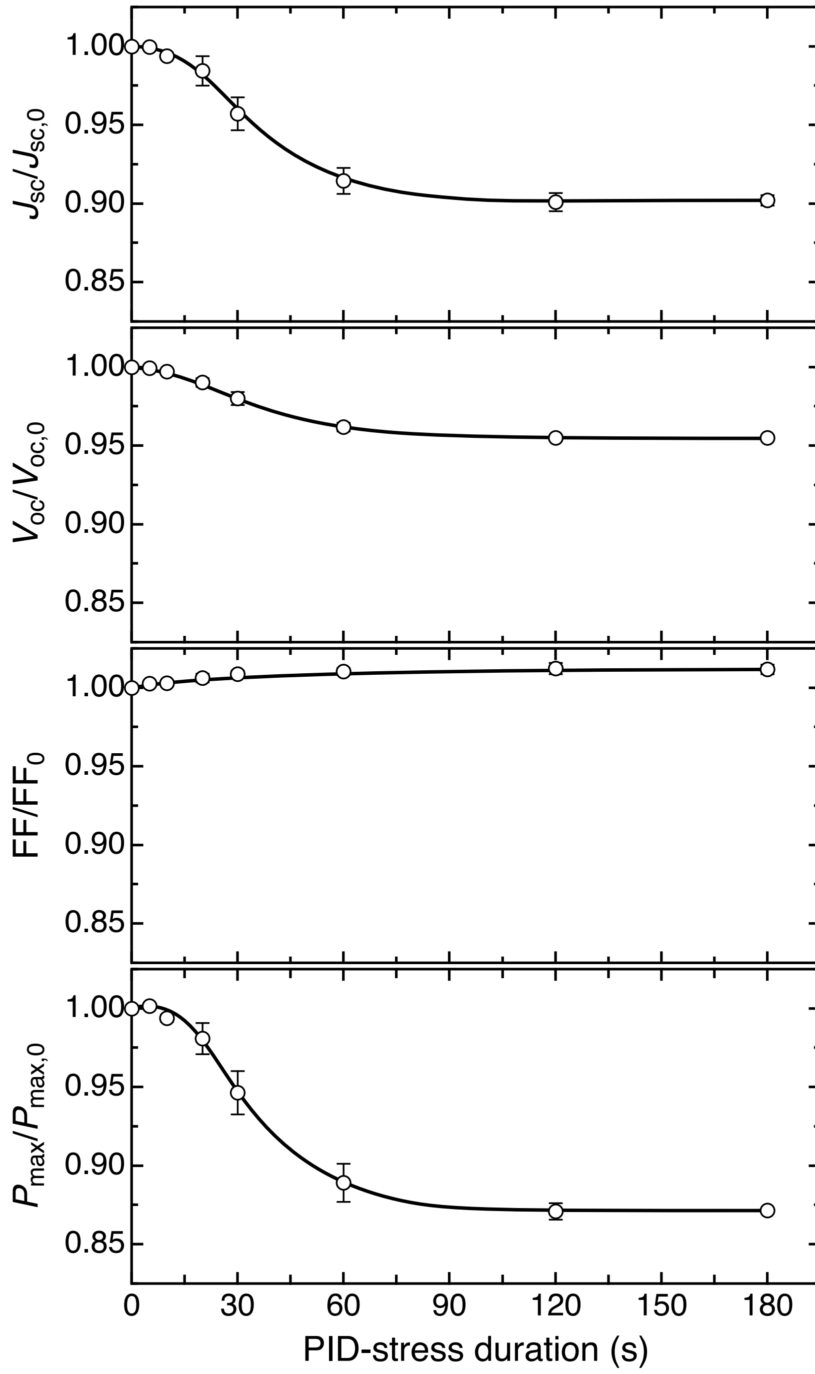

Fig. 1

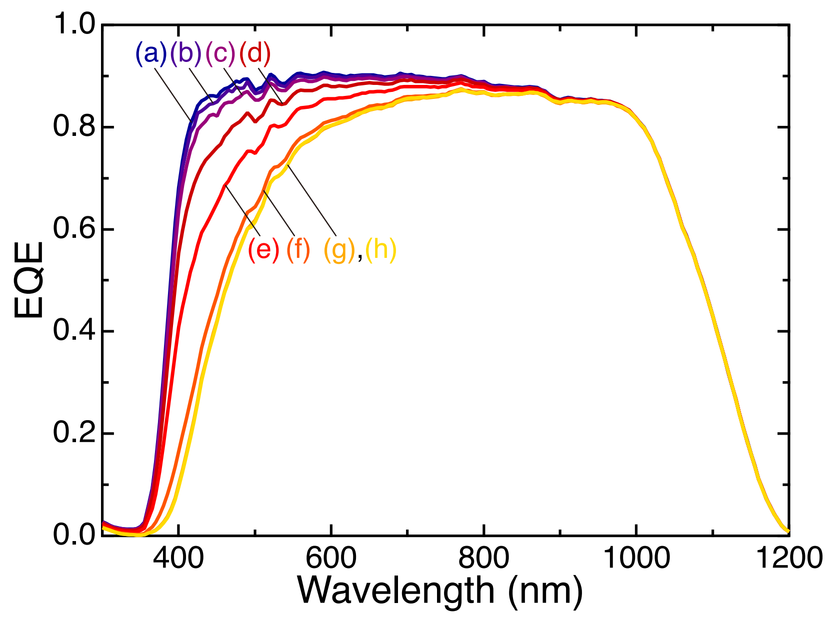

Fig. 2

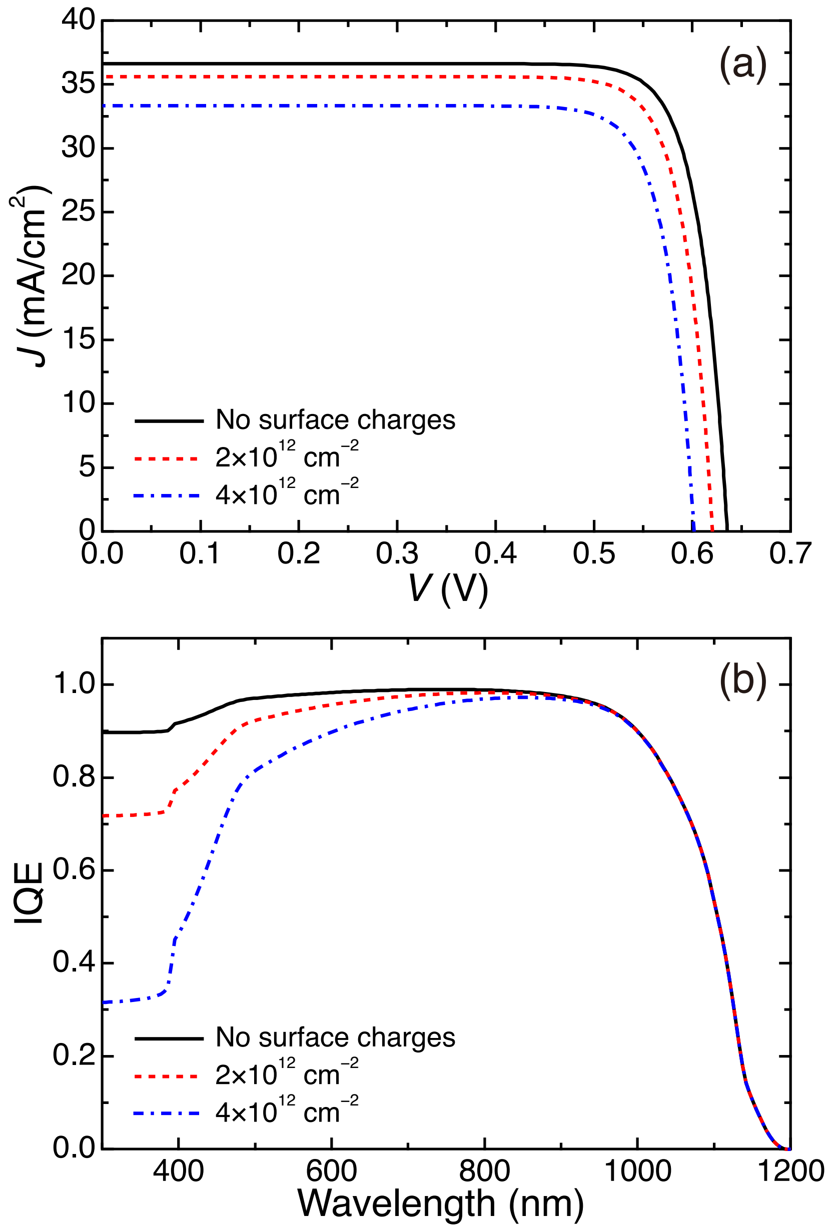

Fig. 3

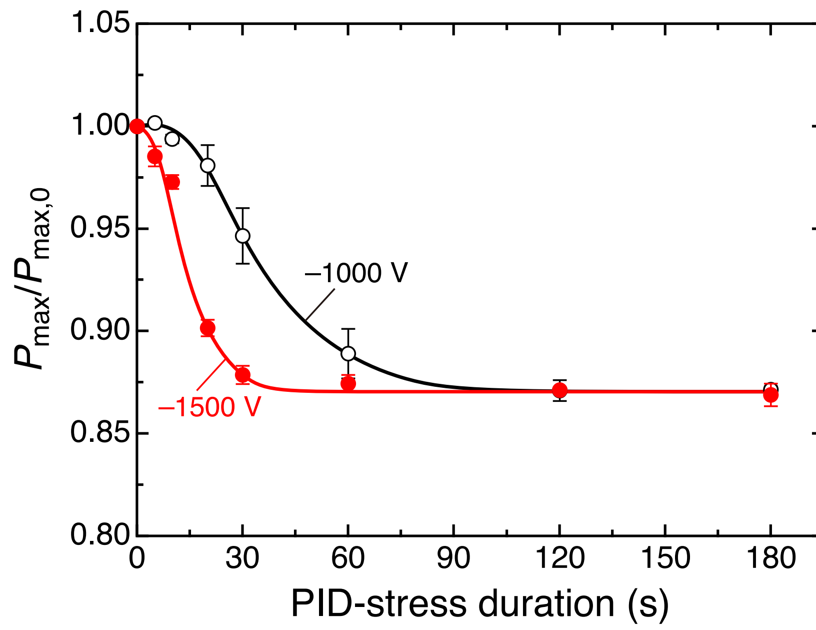

Fig. 4