Title	Direct observation of changes in the effective minority-carrier lifetime of SiNx-passivated n-type crystalline-silicon substrates caused by potential-induced degradation and recovery tests
Author(s)	Nishikawa, Naoyuki; Yamaguchi, Seira; Ohdaira, Keisuke
Citation	Microelectronics Reliability, 79: 91-95
Issue Date	2017-11-05
Type	Journal Article
Text version	author
URL	http://hdl.handle.net/10119/16134
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Description	

Direct observation of changes in the effective minority-carrier lifetime of SiN_x-passivated n-type crystalline-silicon substrates caused by potential-induced degradation and recovery tests

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Abstract

We directly observed reductions in the effective minority-carrier lifetime (τ_{eff}) of n-type crystalline silicon (c-Si) substrates with silicon-nitride passivation films caused by potential-induced degradation (PID). We prepared PID-test samples by encapsulating the passivated substrates with standard photovoltaic-module encapsulation materials. After PID tests applying −1000 V to the c-Si samples from the glass surface, the τ_{eff} was decreased, which probably pertains to Na introduced into the c-Si. After PID tests applying +1000 V, the sample, on the other hand, showed a considerably rapid τ_{eff} reduction, probably associated with the surface polarization effect. We also performed recovery tests of predegraded samples, by applying a bias opposite to that used in a degradation test. The τ_{eff} of a sample predegraded by applying +1000 V was rapidly completely recovered by applying −1000 V, while those of predegraded by applying −1000 V show only slight and insufficient τ_{eff} recovery.

Keywords: Potential-induced degradation; Surface polarization effect; n-type crystalline silicon photovoltaic module; Effective minority-carrier lifetime; Silicon nitride passivation film

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1. Introduction

n-type crystalline-Si (c-Si)-wafer-based photovoltaic (PV) cells are receiving a lot of attention because of their high conversion efficiencies caused by high minority-carrier lifetime [1]. In addition, these cells are tolerant of light-induced degradation compared to conventional p-type c-Si PV cells. Aluminum-alloyed rear-emitter (RE) n-type c-Si PV cells [2–5] are particularly promising in terms of mass production because they can be fabricated through a low-cost fabrication process which has been already widely used in the production of conventional p-type c-Si PV cells. Therefore this kind of PV cell is suitable for use in very large-scale (VLS) PV systems.

Potential-induced degradation (PID) [6–9] has been considered one of the most crucial reliability issues in VLS PV systems. PID is caused by potential differences between cells and grounded module frames, and is known to lead to catastrophic failure of PV modules. Thus it is very important to understand the PID behaviors and mechanisms of deployed PV modules.

There are several reports regarding PID of n-type c-Si PV modules [10–17]. We have reported the degradation of the open-circuit voltage (V_{oc}) and the fill factor of RE n-type c-Si PV modules under a negative-bias application, which results in ~7% reduction in the maximum output power compared to the initial value [10]. (Herein, we use the terms "negative bias" and "positive bias" for biases that produce samples with negative and positive potentials with respect to the front surface of the cover glass, respectively.) In an earlier study [11], Naumann et al. have observed a similar kind of degradation in interdigitated back-contact (IBC) c-Si PV cells. Moreover, RE n-type c-Si PV modules are known to show moderate degradation in the V_{oc} under positive bias [10], which may occur with the same degradation mechanism as the surface polarization effect proposed in pioneering work by Swanson et al [12]. The surface polarization effect occurs also in PV modules with n-type c-Si PV cells with a p^+ front emitter [13–15]. These two kinds of degradation occurring in RE n-type c-Si PV modules should be both correlated with reductions in effective minority-carrier lifetimes (τ_{eff}); however, no one has directly observed changes in τ_{eff} caused by PID. The findings may improve the understanding of PID in RE n-type c-Si PV modules.

In this work we conducted PID tests for c-Si substrates whose both sides were passivated with silicon nitride (SiN_x) films to investigate τ_{eff} changes caused by PID stress. We also investigated the effects of applying a bias opposite to that used in PID tests on the τ_{eff} of samples degraded by PID tests. This study was conducted to elucidate PID occurring

in PV modules with both-side-contacted RE n-type c-Si PV cells; however, its findings can be readily extended to PID phenomena in PV modules with n-type IBC c-Si PV cells with the front surface passivated with a SiN_x film. This is because their front-side surface passivation configuration is very similar to that of our samples used in this study.

2. Experimental procedure

We prepared samples schematically illustrated in Fig. 1(a) to clarify the effects of PID stress on the τ_{eff} of n-type c-Si-wafer-based PV cells including RE n-type c-Si PV cells. These samples involved both-side SiN_x passivation films and an n-type float-zone c-Si substrate. 4-inch, ~300-μm-thick, phosphorus-doped c-Si wafers with a resistivity of 1–5 Ω·cm and a bulk minority-carrier lifetime of >10 ms were cleaved to 20 × 20-mm^2-sized substrates. After the standard RCA cleaning of the substrates, their rear sides were coated with a liquid phosphosilicate glass (PSG) source (Tokyo Ohka Kogyo SC-913) by spin coating, and the substrates were subsequently annealed at 850 °C for 25 min in N_2 atmosphere to form n^+-doped layers. These rear n^+ layers were formed to easily provide Ohmic contact to screen-printed silver electrodes. Posterior to the removal of remaining PSG layers, we deposited SiN_x films with a thickness of ~75 nm and a refractive index of ~2.0 on the both sides of the substrates by catalytic chemical vapor deposition (Cat-CVD) [18, 19]. Cat-CVD SiN_x films were deposited at SiH_4 and NH_3 flow rates of 8 and 300 sccm, respectively, at a pressure of 15 Pa, and at substrate holder and catalyzer temperatures of 300 and 1800±50 °C, respectively. Their thickness and refractive index were determined by ellipsometry using the 632.8 nm line of a He-Ne laser. We conducted screen printing of silver pastes on the rear n^+ layers, followed by firing through in a tube furnace at 800 °C to provide Ohmic contact to the substrates.

Interconnector ribbons were soldered onto the busbar of the silver electrodes. Fabricated were stacks composed of conventional tempered cover glass/ethylene-vinyl acetate copolymer (EVA) encapsulant/passivated c-Si/EVA encapsulant/backsheet [poly(vinyl fluoride) (PVF)/poly(ethylene terephthalate)/PVF], where the "passivated c-Si" means the sample passivated with both-side SiN_x as shown in Fig. 1(a). Module-like structures schematically illustrated in Fig. 1(b) were fabricated by laminating the stacks in a module laminator. Our lamination process consisted of two steps: a degassing step for 5 min and an adhesion step for 15 min. The stacks were placed with the cover-glass side down on a stage maintained at 115 °C during lamination. The PID tests for module-like samples shown in Fig. 1(b) were performed by applying a negative bias of −1000 V or a positive bias of

+1000 V to the rear-side contact of the samples with respect to an aluminum plate placed on the top of the cover glass at 85 °C. To ensure contact between the aluminum plate and the cover glass, an electrically conductive rubber sheet was inserted between them. The τ_{eff} lateral mapping data (not shown) of the samples were obtained by microwave-detected photoconductive decay measurements using a KOBELCO LTA-1510EP apparatus, before and after the PID tests. All the τ_{eff} values reported throughout this paper are the maximum τ_{eff} values in τ_{eff} mappings of samples. For the samples subjected to the PID tests, we also performed recovery tests by applying a bias opposite to that used in the degradation tests. For example, a sample was subjected to the PID test applying −1000 V and, subsequently, was subjected to the recovery tests applying +1000 V. Humidity was not controlled during all the PID and recovery tests; however, relative humidity in a similar setup [20] is known to become very small (> roughly 2% RH) at 85 °C.

3. Results and discussion

Shown in Fig. 2 are changes in the τ_{eff} of the investigated samples subjected to PID-tests in which a negative bias of −1000 V was applied. The τ_{eff} first increases rapidly, then gradually decreases with increasing PID-stress duration, and seems to saturate within around 110 h. Generally, negative biases with respect to the cover glass lead to sodium (Na) introduction into PV cells and positive charge accumulation in the front passivation films. In this case, the latter is not detrimental because positive charges in the front passivation films repel minority carries—holes—away from the surface and rather should improve the τ_{eff} of the samples. The τ_{eff} improvement observed in the initial stage of the PID test is probably related to the positive charge accumulation in the SiN_x. The successive degradation of τ_{eff} should be correlated with the former phenomenon—Na introduction. The degradation behavior seems to be qualitatively consistent with that of the V_{oc} of RE n-type c-Si PV modules undergoing PID [10]. According to previous studies regarding PID in conventional p-type c-Si PV modules [21–23], Na positive ions pass through the front SiN_x passivation films, induce the formation of stacking faults in the surface region of the Si layer, and simultaneously decorate the stacking faults, with assistance from a negative bias. These Na-decorated stacking faults behave as shunts when they intersect the p–n junction interface [21, 22]. In RE n-type c-Si PV modules, such Na-decorated stacking faults, on the other hand, do not behave as shunts because these cells have no p–n junction on the front side. Instead, these Na-decorated stacking faults can act as additional recombination centers in RE n-type c-Si PV modules; thereby, their V_{oc} are reduced [10,

24]. A similar model has been proposed to explain PID in n-type IBC c-Si PV cells [11]. The τ_{eff} reductions observed in our samples are consistent with these proposed hypotheses and can explain the reason behind reductions in the V_{oc} in prior studies [10, 11]. As for the saturation behavior, it has been reported that the PID of RE n-type PV modules tends to saturate [10], and thus, the saturation behavior in the lifetime reduction appears to be consistent with the previous results; however, duration needed to saturate the τ_{eff} reduction largely differs from that needed to saturate V_{oc} reductions. A possible reason for this is that there are differences in the properties of SiN_x films and/or c-Si substrates. We should also mention that Na ions tend to accumulate at SiN_x/Si interface under negative-bias PID stress in conventional p-type PV modules [21, 22]. The same phenomenon probably occurs also in our samples used in this study, which can be another reason for the enhancement in the surface recombination of minority carriers.

Fig. 3 shows τ_{eff} changes caused by PID tests in which a positive bias of +1000 V was applied. In this case, the τ_{eff} rapidly degrades and saturates within several minutes. This observation probably results from the surface polarization effects proposed by Swanson et al. [12], caused by negative-charge accumulation in the front SiN_x passivation films. Such negative charges attract minority carriers—holes—in the vicinity of SiN_x/c-Si interface, and, thereby, surface recombination via surface defect states is activated. The rapid degradation and the subsequent saturation are similar to the results of previous work regarding PID in front-emitter n-type c-Si PV modules [14]. The result in Fig. 3 also explains previously reported, slight degradation in RE n-type PV modules under positive bias [10]. Our both-side-passivated sample used in this study, however, tends to be substantially affected by the charge accumulation, compared to the PV modules used in the previous study [10]. This is because the passivated c-Si has a low doping density of 10^{15}–10^{16} /cm^3, which makes it susceptible to charge accumulation in the passivation films. (Actual devices generally have a heavily doped surface region with a doping density of 10^{19}–10^{21} /cm^3, reducing the effect of charge accumulation.)

PID-affected p-type c-Si PV modules and some kinds of n-type c-Si PV modules are known to recover from the degradation by applying an opposite bias to that applied during their degradation [7, 13, 15, 25, 26]. To evaluate such a recovery effect, we also conducted the recovery tests of the samples that were, in advance, degraded in PID tests in which a negative bias of −1000 V was applied for 177 h. After the PID tests, the recovery tests were performed by applying a positive bias of +1000 V. Fig. 4 shows the τ_{eff} of the degraded sample as a function of the duration of the positive bias application. The τ_{eff} of the samples

first further decreases slightly by applying +1000 V, probably due to negative-charge accumulation in the SiN_x films. The samples then exhibit a slow and slight τ_{eff} recovery; however, the τ_{eff} after a >140-h recovery test is severely far from the initial τ_{eff} value. The exact reason for the insufficient recovery of τ_{eff} is still an open question. In a previous study [25], it has been reported that a positive bias leads to the outdiffusion of Na from stacking faults and leaves stacking faults without Na. On the basis of the observation, the lifetimes should be recovered in a certain extent, by the application of +1000 V. As mentioned above, our samples, however, tend to be susceptible to charge accumulation because of their low doping density. Therefore, even if Na outdiffusion occurs and carrier recombination via the Na impurity states is suppressed, our samples are instead strongly affected by the negative charge accumulation caused by the application of +1000 V, and the τ_{eff} was strongly limited by field-enhanced recombination via surface states. This may explain the reason behind the incomplete τ_{eff} recovery in our samples. There is also a possibility that such stacking faults remaining near the surface of the c-Si substrates behave as recombination centers and reduce the τ_{eff}. (Note that there are no or few stacking faults before stressing. The formation of stacking faults is known to occur together with the incorporation of Na, during the application of a negative bias [23].) To understand this phenomenon, we will have to perform detailed analyses.

We also performed the recovery tests of the sample that was, in advance, subjected to PID test in which a positive bias of +1000 V was applied for 30 h. After the PID test, the recovery tests were conducted by applying a negative bias of −1000 V to the sample. The sample exhibits τ_{eff} exceeding the initial value after the recovery tests for a minute. This recovery is most likely caused by the detrapping of negative charges accumulated in SiN_x during the degradation test. The overcompensation in the τ_{eff} may be due to the accumulation of positive charges with a density exceeding the initial charge density. However the τ_{eff} decreases again by further application of the negative bias, which probably pertains to Na introduction into the surface region of the n-type c-Si substrate.

Finally, we discuss the tolerance of RE n-type PV modules against PID stress based on the experimental results obtained in this study, as well as our previous work [10]. The rapid decrease in τ_{eff} under a positive bias application, originating from charge accumulation in a surface SiN_x layer, will take place also in the RE n-type cells of out-door PV modules. We have, however, separately confirmed quite small performance deterioration of RE n-type PV modules under a positive-bias application [10]. Furthermore, this PID can be easily recovered by applying an opposite bias, as demonstrated in Fig. 5. We thus expect that the

PID of RE n-type modules under a positive bias does not become significant matter in a field application. On the other hand, the PID of RE n-type PV modules under a negative-bias stress will be more harmful for the actual field application. The performance degradation of RE n-type PV modules by a negative-bias application will not recover significantly by the application of an opposite bias, based on the results shown in Fig. 4. However, the degree of the performance degradation of RE n-type PV modules by negative-bias application has been estimated to be only ~7% in relative [10], and it will be suppressed more by using encapsulant with higher volume resistivity, as in the case of p-type conventional PV modules [6]. We thus emphasize that RE n-type PV modules have high tolerance against PID and are suitable for usage in VLS PV systems.

4. Conclusions

In summary, we directly observed reductions in the τ_{eff} of SiN_x-passivated c-Si substrates caused by PID stress. In the case of the PID tests applying a negative bias of −1000 V, the τ_{eff} of the samples gradually decreased with increasing PID-stress duration and saturates within 110 h. These τ_{eff} reductions may pertain to the formation of Na-decorated stacking faults. On the other hand, the τ_{eff} of a sample rapidly decreased and subsequently saturated within several minutes in the PID tests applying a positive bias of +1000 V, which is due to the surface polarization effect. A sample degraded under the positive bias rapidly recovered their recombination losses by applying a negative bias of −1000 V. In the recovery test under a positive bias of +1000 V, the samples degraded under the negative bias rather showed further reductions in their τ_{eff}, which is most likely due to negative-charge accumulation in the front SiN_x passivation films, and subsequently exhibited only slight and insufficient τ_{eff} recovery.

Acknowledgments

This material is based upon work supported by the New Energy and Industrial Technology Development Organization (NEDO). The authors would like to thank Dr. Atsushi Masuda of National Institute of Advanced Industrial Science and Technology for providing the encapsulants and the backsheets. The authors would also like to thank Yutaka Komatsu of Japan Advanced Institute of Science and Technology for his assistance.

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Figure Captions

Fig. 1. Structures of (a) the passivated and screen-printed n-type c-Si substrate samples and (b) the module-like encapsulated samples (not to scale).

Fig. 2. Dependence of the τ_{eff} of the samples on PID-stress duration. The voltage was set to −1000 V. The data points are the mean values for three samples.

Fig. 3. Dependence of the τ_{eff} of the sample on PID-stress duration. The voltage was set to +1000 V. These data points were obtained from measurements for the one sample.

Fig. 4. Recovery behavior of the τ_{eff} of the samples by the application of a positive bias of +1000 V. The samples were predegraded by the PID tests in which a negative bias of −1000 V was applied. The data points are the mean values for three samples. The dotted line shows the mean of the initial τ_{eff} for the three samples.

Fig. 5. Changes by the recovery tests in the τ_{eff} of the degraded sample. The sample was, in advance, subjected to the PID test in which a positive bias of +1000 V was applied for 30 h, and subsequently, underwent the recovery tests in which a negative bias of −1000 V was applied. These data points were obtained from measurements for the one sample. The dotted line corresponds to the initial τ_{eff}.

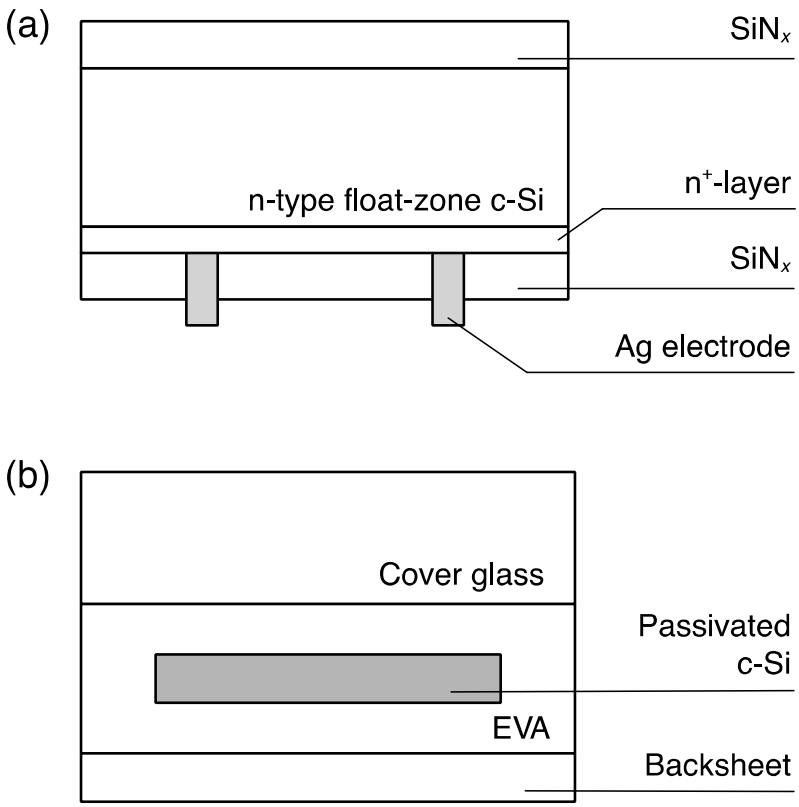
(a)
SiN$_x$
n-type float-zone c-Si
n$^+$-layer
SiN$_x$
Ag electrode
(b)
Cover glass
Passivated
c-Si
EVA
Backsheet

Fig. 1.

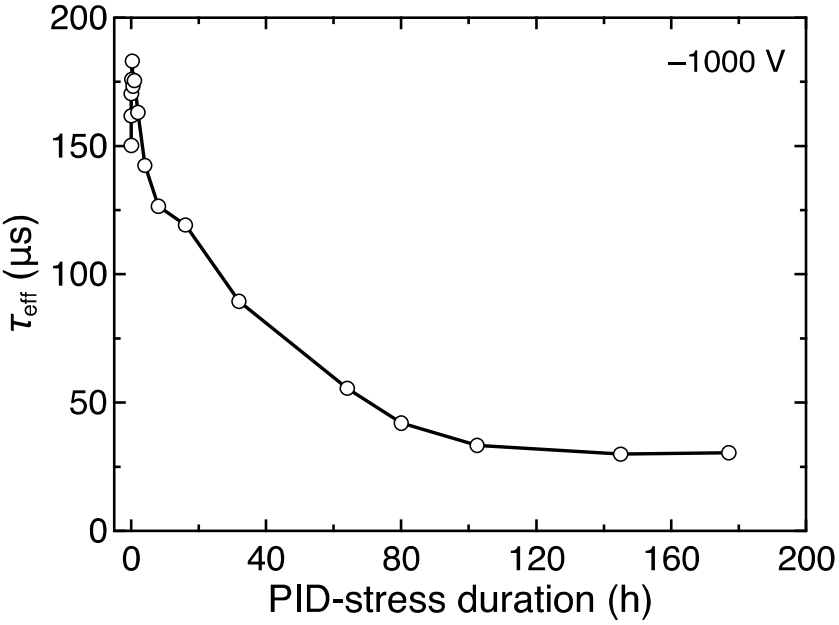
200
150
100
50
0
τ_{eff} (µs)
–1000 V
0
40
80
120
160
200
PID-stress duration (h)

Fig. 2.

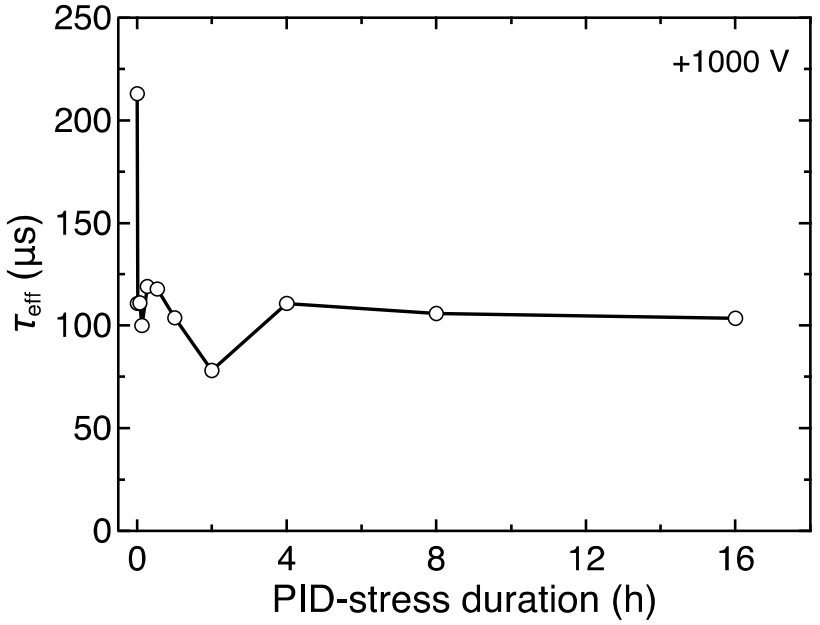
+1000 V
τ_{eff} (µs)
250
200
150
100
50
0
0
4
8
12
16
PID-stress duration (h)

Fig. 3.

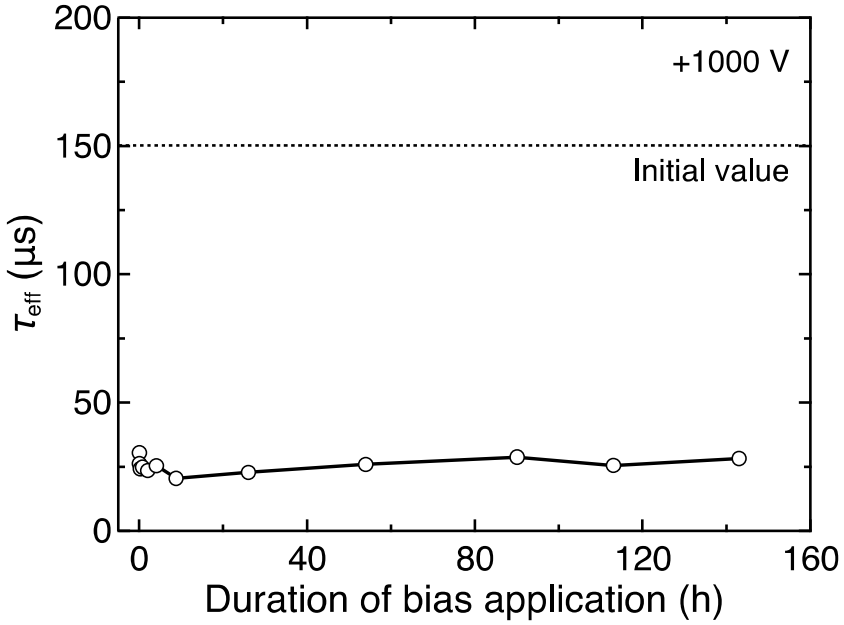
200
150
100
50
0
τ_{eff} (μs)
+1000 V
Initial value
0
40
80
120
160
Duration of bias application (h)

Fig. 4.

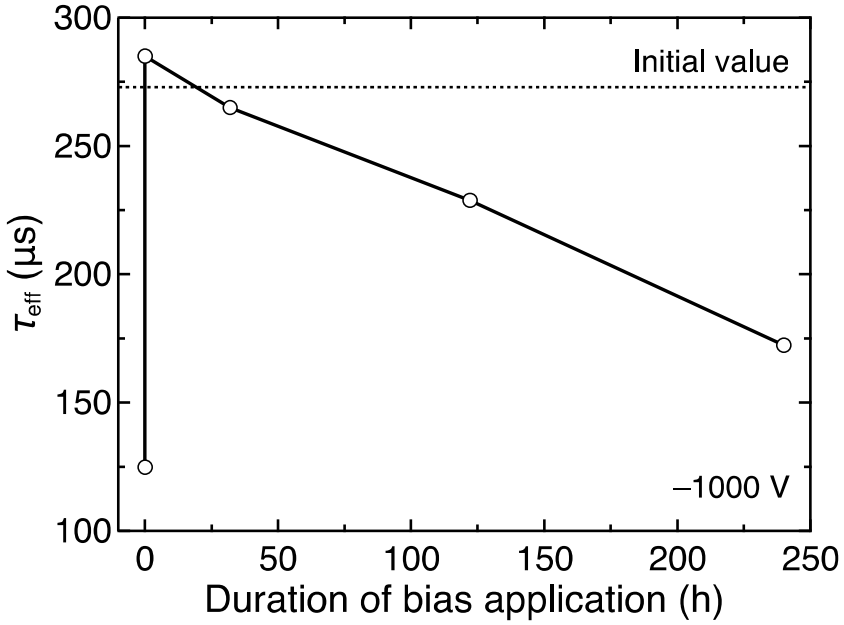
300
250
200
150
100
τ_{eff} (μs)
Initial value
–1000 V
0
50
100
150
200
250
Duration of bias application (h)

Fig. 5.