Degradation behavior of crystalline silicon solar cells in a cell-level potential-induced degradation test

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Abstract

The degradation behavior of crystalline silicon (c-Si) solar cells in a cell-level potential-induced degradation (PID) test and the effect of the test conditions are reported. The PID tests were performed in a vacuum chamber by applying a voltage of 1000 V from a temperature-controlled aluminum chuck underneath an unlaminated sample stack to the top copper electrode placed on the stack. The stack was composed of soda-lime glass, an ethylene vinyl-acetate copolymer sheet, and a conventional p-type c-Si solar cell. The investigated solar cell exhibited a large degradation of the fill factor and slight degradation of the open-circuit voltage. These degradations were mainly caused by a reduction in the parallel resistance, which is the same degradation behavior as that reported previously. This indicates that the cell-level PID test well reproduces the typical degradation behavior. However, the leakage current in the unlaminated sample stack at a relatively low temperature exhibited a different temperature dependence from that in a laminated sample stack. The difference in the temperature dependence was caused by temperature-dependent contact resistances within the unlaminated sample stacks. This indicates that there is a difference between the temperature dependences in cell-level and module-level PID tests. This difference in the temperature dependence was reduced by the use of a heavier top electrode. These findings may assist in choosing the proper test conditions for this kind of cell-level PID test. A cell-level PID test for an n-type front-emitter c-Si solar cell was also performed. A typical degradation behavior, characterized by reductions in the open-circuit voltage and the short-circuit current, was observed, which implies that this test can be widely applied to PID phenomena occurring in many kinds of solar cells.

Keywords: Potential-induced degradation; Reliability test; Crystalline silicon solar cell; Leakage current

1. Introduction

Potential-induced degradation (PID) has been identified as one of the most important reliability issues of photovoltaic (PV) modules deployed in large-scale PV systems (Luo et al., 2017). Relatively high electric-potential differences can exist between the flame and cells in PV modules deployed in such systems, which may lead to significant performance losses. This kind of degradation is called PID, and has been reported to occur in various types of PV modules, such as conventional p-type crystalline silicon (c-Si) (Hacke et al., 2010; Pingel et al., 2010; Berghold et al., 2010), front-emitter n-type c-Si (Hara et al., 2015, 2017; Yamaguchi et al., 2016a; Bae et al., 2017), rear-emitter n-type c-Si (Yamaguchi et al., 2016b, 2016c), n-type back-contact c-Si (Swanson et al., 2005; Naumann et al., 2014a), amorphous Si (a-Si) thin-film (Osterwald et al., 2003, Masuda et al., 2017), c-Si/a-Si heterojunction (Yamaguchi et al., 2017), cadmium telluride thin-film (Hacke et al. 2015, 2016a), and copper indium gallium selenide thin-film (Fjällström et al., 2013; Hacke et al. 2015; Yamaguchi et al., 2015) PV modules, and PV modules with different types of cells are known to degrade with different degradation mechanisms.

To investigate individual PID phenomena, several kinds of PID tests have been used (Luo et al., 2017). In particular, module-level PID tests have been considered basic methods to investigate the PID phenomena. These module-level PID tests have been successfully used to elucidate the influence of environmental factors, the effect of module components, kinetics of PID, and so forth. In such tests, it is, however, difficult to isolate the degraded solar cells and subject them to analyses, such as electron microscopy, because the module components strongly adhere to the cells. This has been a barrier to determining the root cause of PID.

To overcome the difficulty, a cell-level PID test was developed in the Fraunhofer Center for Silicon Photovoltaics (Lausch et al., 2014) and has been successfully used to elucidate the root cause of PID. In this test, module-like layer stacks without lamination are used, which significantly reduces the effort to prepare samples, which enables a quick testing of the PID susceptibility of module components and cells. However, of most importance is the ease with which PID-affected bare cells can be obtained after PID tests, which enables investigation of the root cause in more detail. By using this test, the understanding of PID phenomena occurring in p-type c-Si PV cells has been improved (Naumann et al., 2013, 2014b, 2016). Despite the importance of the cell-level PID test, to date, the degradation behavior and the effects of the test conditions have not been discussed in detail. A comparison between the cell-level and module-level PID tests has not yet been made. These findings may help us select the proper test conditions for this kind of PID test.

In this study, we first investigated whether a typical degradation behavior can be reproduced in the cell-level PID test. We also clarified the effects of the test conditions, such as temperature and pressure applied to samples, on the degradation rate and the leakage current. On the basis of the obtained results, we will discuss the difference between the cell-level and module-level PID tests. In the cell-level PID test, the degradation rate was confirmed to positively correlate

with temperature, which is similar to that observed in module-level PID tests; however, we observed that the dependence of the leakage current on temperature in the cell-level PID test was different from that in module-level PID tests. This modification is proposed to arise from the temperature dependence of interface contact resistances within the unlaminated sample stacks. The applied pressure, which is a specific parameter in the cell-level PID test, was found to reduce the difference in the temperature dependence.

2. Experimental procedure

Module-like stacks composed of 0.7-mm^2-thick flat soda-lime glass, a 0.4-mm-thick uncured ethylene vinyl-acetate copolymer (EVA) sheet, and a PID-prone p-type c-Si solar cell were prepared. The stacks were placed on a temperature-controlled aluminum (Al) chuck in a test chamber, with the cell side down, and a 0.05-, 0.10-, or 0.15-kg-weight copper block was placed on the glass. The copper blocks, the glass, and the EVA sheets had an area of 19.8 × 19.8 mm^2, whereas the solar cells had an area of 20 × 20 mm^2. This meant that there was no current flow through the edge surfaces of the solar cells. The copper block served as both the top electrode and a weight to reduce the contact resistance within the unlaminated sample stacks. The pressure applied to the sample stacks was changed by exchanging the copper block for another copper block with a different weight, where the pressures applied from the 0.05-, 0.10-, and 0.15-kg-weight copper blocks were 1.2, 2.5, and 3.7 kPa, respectively. The chamber was pumped with a diaphragm pump during the PID tests, which assisted in achieving good contacts between the components by eliminating air bubbles lying at the interfaces between the components. PID tests were performed by applying a voltage of 1000 V to the copper block with respect to the Al chuck maintained at 65 and 75 °C, using a PID Insulation Tester (KIKUSUI, TOS7210S) with an ammeter to detect the leakage currents flowing vertically within the samples during the voltage application. The voltage condition was the negative bias condition in the typical module-level PID tests. Leakage current densities were calculated by dividing the measured leakage currents by an area of 19.8 × 19.8 mm^2, which corresponded to those of the copper blocks, the glass, and the EVA sheets. Note that the front and rear electrodes of the solar cells were shorted in most of module-level PID tests whereas they were not shorted in this cell-level PID test. The diode of the investigated solar cells was therefore reverse-biased during the course of the PID tests. However, this was not a problem because the resistance of the encapsulation materials was considerably larger than that of the diode in the reverse-bias condition. We also used EVA sheets, which were cured in advance at 135 °C for 20 min in an electric furnace, to investigate the effects of the use of cured EVA sheets on the degradation rate.

After each PID test, the glass and the EVA sheet were carefully removed from the surface of the solar cell. To estimate the degradation, dark and one-sun-illuminated current density–voltage (J–V) and external quantum efficiency (EQE) measurements were taken on bare solar cells before and after the PID tests. These measurements were performed at 25 °C. Leakage currents were

collected at elevated temperatures with a wider range from 55 to 85 °C under different test conditions to obtain the Arrhenius plots.

We also performed a PID test of a laminated stack composed of soda-lime glass, the EVA sheet, and the p-type solar cell in the same chamber by applying a voltage of 1000 V to the 0.05-kg-weight copper block placed on the cover glass with respect to the underlying Al chuck maintained at a temperature ranging from 55 to 85 °C. Additionally, the front and rear electrodes of the investigated solar cell were not shorted in this test. During the PID tests, the leakage current was determined. These data were compared with those from the cell-level PID tests. The sample stack had no rear EVA sheet or backsheet and was prepared using the same module encapsulation materials as those used in the cell-level PID tests. The module-lamination process was the same as that used in a previous study (Yamaguchi et al., 2016b). Because the sample stack experienced a standard module-lamination process, this test was considered as a kind of module-level PID test. We can therefore determine the differences between cell-level and module-level PID tests by comparing the results of this test with those of the cell-level PID tests.

We also performed the cell-level PID test in which an n-type front-emitter c-Si solar cell was stressed under a voltage of 1000 V, a pressure of 1.2 kPa, and a temperature of 65 °C, to further investigate whether the cell-level PID test can reproduce the typical degradation behavior.

3. Results and discussion

3.1. Degradation behavior of a PID-prone p-type c-Si solar cell

To investigate whether our PID test setup can reproduce the typical degradation behavior, we show the cell-level PID test result of the PID-prone p-type c-Si solar cell. Fig. 1 shows the one-sun-illuminated and dark *J–V* data before and after the cell-level PID test at a voltage of 1000 V and a pressure of 1.2 kPa at 65 °C. The fill factor (FF) and the open-circuit voltage (V_{oc}) decreased with increasing the PID-stress duration (Fig. 1a). From Fig. 1b, the decrease in the FF was mainly caused by a reduction in the parallel resistance. All the investigated samples with p-type c-Si solar cells showed a typical shunting behavior after the PID tests. This result demonstrates that this kind of cell-level PID test can, without lamination, reproduce the typical PID shunting behavior that has been frequently observed in both module-level PID tests and systems in operation.

3.2. Effects of temperature and applied pressure on the progression of PID

Fig. 2 shows the effect of temperature on the progression of the PID of the p-type c-Si solar cells in the cell-level PID test, where a voltage of 1000 V and a pressure of 1.2 kPa were applied. Obviously, the high temperature also accelerated the degradation rate in the cell-level PID tests. This temperature effect partially arose from a temperature-activated ion drift within the sample stack. This may be quite a natural result; however, we observed a different temperature dependence from that in the module-level PID tests owing to the unlaminated sample stack in this test, which will be discussed in Sect. 3.3. It should be noted that the setting

temperature was actually limited to be relatively low in our cell-level PID test owing to undesirable adhesion. In our PID test, undesirable lamination occurred at a temperature of >80 °C. A special treatment of the EVA sheets is known to be needed to avoid such adhesion (Lausch et al., 2014).

Fig. 3 shows the dependence of the applied pressure on the progression of degradation in the PID tests where a voltage of 1000 V was applied at 65 °C. The degradation rate appeared to increase with increasing applied pressure. As shown in Fig. 4, the leakage current density slightly increased with increasing the applied pressure. This result suggests that an increase in the applied pressure reduces the interface contact resistances between the glass and the EVA sheet and between the EVA and the solar cell. Interstices can be distributed along both interfaces because of the surface roughness of the EVA sheet and the textured surface of the solar cell. These interstices behave as large interface resistances, which hinder the current flow through the interfaces. In this cell-level PID test, the applied pressure induces an elastic deformation of the EVA sheet and, as a result, reduces the interstices, which leads to a reduction in the interface contact resistances.

3.3 Temperature- and pressure-dependent leakage current analysis

To investigate the effects of temperature and pressure in more detail, leakage currents flowing vertically within the samples were measured under different temperature and pressure conditions. These leakage currents are known to mainly originate from the drift of mobile ions such as sodium ions (Luo et al., 2017). Arrhenius plots of leakage currents density under each pressure condition are shown in Fig. 5. For comparison, also shown are the results of the PID test using a cured EVA sheet and of module-level PID test where the laminated sample stack was used. When the cured EVA sheet was used, the degradation rate was reduced (not shown here). This is consistent with the results presented in a previous study (Jonai et al, 2015).

For the laminated sample stack, the logarithm of the leakage current densities exhibited a linear dependence of the inverse temperature with an activation energy (E_a) of 0.66 eV (c.f. the solid line shown in Fig. 5). This E_a is similar to that obtained from a module-level PID test with a relatively low humidity (Hacke et al., 2016b), indicating that the leakage current in our laminated sample obeys the same kinetics observed in PV modules.

For the cell-level PID tests, at a high temperature ($1000/T < 2.9\ K^{-1}$), log leakage current densities in the cell-level tests exhibited a linear inverse-temperature dependence similar to that in the module-level PID test (c.f. the upper broken straight line in Fig. 5); however, at a low temperature ($1000/T > 2.9\ K^{-1}$), leakage current densities showed negative deviations from the straight line. The degree of these deviations tended to be larger when a lower pressure was applied to the sample stack. This difference between the laminated and unlaminated PID test samples originated from the temperature dependence of the interface contact resistances between the glass and the EVA and between the EVA and the cell. This modification does not arise from the use of the uncured EVA, because a similar modified temperature dependence can be observed even when pre-cured EVA is used. The reduced leakage currents are caused by an increase in

the volume resistance of the cured EVA (Jonai et al., 2015). At a low temperature, there are many interstices present along the interfaces. EVA sheets are, however, highly fluid and deformable in accordance with the surface morphology of the adjacent layers at a high temperature, reducing the interface contact resistances. When the temperature is sufficiently high, the interstices will probably almost completely disappear, and eventually the interface contact resistances lose their temperature dependence. Leakage currents in the unlaminated sample stacks therefore obeyed the same kinetics as those in module-level PID tests at a high temperature.

The applied pressure seemed to reduce the interface resistances and to enhance the leakage current. This can be confirmed from the fact that the deviations from the straight line were smaller when the applied pressure became larger. A sufficiently high, applied pressure is therefore required to reduce the effect of interface contact resistances at a low temperature. Hence, a high applied pressure plays an important role in filling the gap between the module-level and cell-level PID tests.

On the basis of the above results, the hardness of the polymer sheets is expected to also influence the result of the PID tests, because it effects the interface contact resistances and thus the leakage current. This is because it is difficult to reduce the interstices when the encapsulant is hard. This suggests that when we use relatively hard encapsulants, their PID resistance may be overestimated owing to the high interface contact resistances. To correctly estimate the PID resistance of such encapsulants, sufficiently high temperature and applied pressure must be used. This kind of PID test may be a simple means to estimate the PID susceptibility of module components although the conditions should be carefully chosen so as not to overestimate the PID resistance of such encapsulants.

3.4 Degradation behavior of an n-type c-Si solar cell

To further verify whether this kind of cell-level PID test can reproduce the typical degradation behavior, we performed a degradation test of an n-type front-emitter c-Si solar cell. Fig. 6 shows the *J–V* characteristics and the EQE spectra of the initial cell and the cells after the degradation tests where a voltage of 1000 V and a pressure of 1.2 kPa were applied at 65 °C for 1, 6, and 12 h. Fig. 7 shows the progression behavior of $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, and $P_{max}/P_{max,0}$ of the cell during the PID test, where the subscript 0 indicates the initial values and P_{max} is the maximum output power.

Fig. 6a shows the degradation characterized by reductions in V_{oc} and J_{sc}. This was caused by an enhancement of the surface recombination of minority carriers since the EQE was significantly reduced in the short wavelength region of 300–800 nm. This degradation behavior is the same as the module-level PID test results reported in a previous study (Hara et al., 2015). This degradation has been reported to arise from an increase in the density of fixed positive charges in the front passivation layers (Bae et al., 2017) (so-called the “surface polarization effect”). It has also been reported that the PID in n-type front-emitter c-Si PV modules saturates within a relatively short duration (Yamaguchi et al., 2016a). In

our cell-level PID test, the rapid saturation can be observed within 3 h, as shown in Fig. 7, which is consistent with a previous result (Yamaguchi et al., 2016a). These results indicate that the cell-level PID test can be widely applied to various kinds of solar cells. On the basis of our results, the cell-level PID test can well reproduce PIDs of the shunting type and the polarization type.

4. Conclusions

We have investigated whether typical degradation behavior reported for p-type c-Si PV modules can be reproduced by the cell-level PID test. The investigated solar cell exhibited degradation of the FF and the V_{oc}, which was mainly caused by a reduction in the parallel resistance. This degradation behavior was the same as that observed in module-level PID tests, indicating that the cell-level PID test well reproduces the typical degradation behavior. This feature is of great importance for investigating the root cause of PID phenomena.

However, a difference was observed in the temperature dependences of the cell- and module-level PID tests. The temperature dependence of the leakage current in the cell-level PID test is modified at a relatively low temperature, by the temperature-dependent interface contact resistance. This difference between cell- and module-level PID tests can be partially overcome by applying a high pressure. The effect of the interface contact resistance is expected to be greater when harder polymer sheets are used. This suggests that in this test, we may overestimate the PID resistance of such hard encapsulants, and we should carefully choose the test condition to correctly determine the PID susceptibility of encapsulants.

We also performed the cell-level PID test of an n-type front-emitter c-Si solar cell. A typical degradation behavior, characterized by reductions in V_{oc} and J_{sc}, was observed, which implies that the test can be widely applied to PID phenomena occurring in various kinds of solar cells.

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Figure Captions

Fig. 1. Degradation behavior of the PID-prone p-type c-Si solar cell in the cell-level PID test. (a) One-sun-illuminated and (b) dark *J–V* data of the cell before and after the PID tests where a voltage of 1000 V and a pressure of 1.2 kPa were applied at a setting temperature of 65 °C.

Fig. 2. Effect of temperature on the progression of the PID of p-type c-Si solar cell in the cell-level PID test. The voltage and the pressure were set to 1000 V and 1.2 kPa, respectively.

Fig. 3. Effect of applied pressure on the progression of the PID of a p-type c-Si solar cell in the cell-level PID test. The voltage and the temperature were set to 1000 V and 65 °C, respectively.

Fig. 4. Dependence of the applied pressure on the leakage current density. The voltage and the temperature were set to 1000 V and 65 °C, respectively.

Fig. 5. Arrhenius plots for leakage currents during the cell-level PID tests where different pressures of 1.2, 2.5, and 3.7 kPa were applied. The voltage was set to 1000 V. For comparison, also included are results of the PID test using the unlaminated sample stack with the cured EVA sheet and of the test using the laminated sample stack. The solid line was drawn by fitting the data obtained from the laminated sample stack to the Arrhenius equation, and the E_a was determined to be 0.66 eV. The upper and lower broken lines were obtained by shifting the fitted line toward the positive and negative directions, respectively.

Fig. 6. (a) One-sun-illuminated *J–V* characteristics and (b) the EQEs of the initial cell and cells after the cell-level PID tests in which a voltage of 1000 V and a pressure of 1.2 kPa were applied at 65 °C for 1, 6, and 12 h.

Fig. 7. Progression behavior of $J_{sc}/J_{sc,0}$, $V_{oc}/V_{oc,0}$, and $P_{max}/P_{max,0}$ of the n-type front-emitter c-Si solar cell during the PID test where a voltage of 1000 V and a pressure of 1.2 kPa were applied at 65 °C.

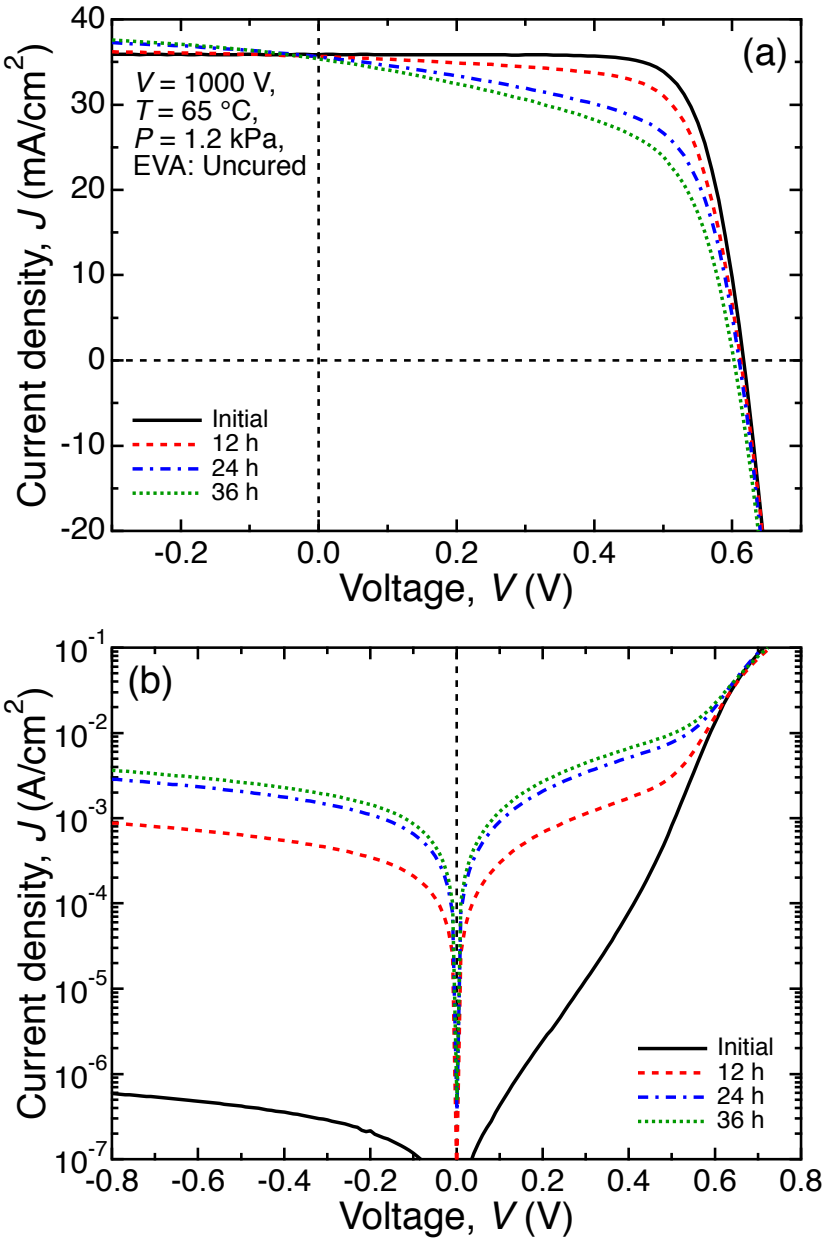
(a)
V = 1000 V,
T = 65 °C,
P = 1.2 kPa,
EVA: Uncured
Initial
12 h
24 h
36 h
Current density, J (mA/cm2)
Voltage, V (V)
(b)
Initial
12 h
24 h
36 h
Current density, J (A/cm2)
Voltage, V (V)

Fig. 1

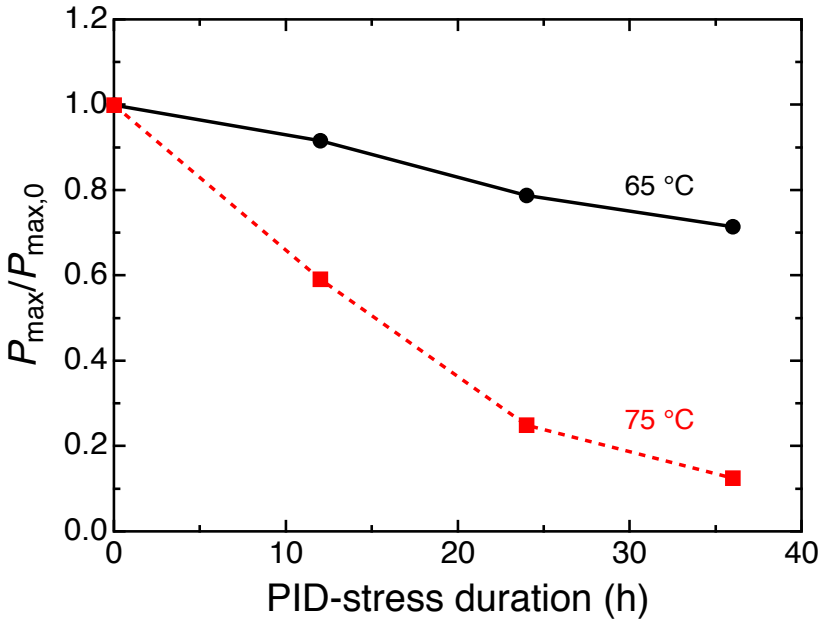
1.2
1.0
0.8
0.6
0.4
0.2
0.0
$P_{max}/P_{max,0}$
65 °C
75 °C
0
10
20
30
40
PID-stress duration (h)

Fig. 2

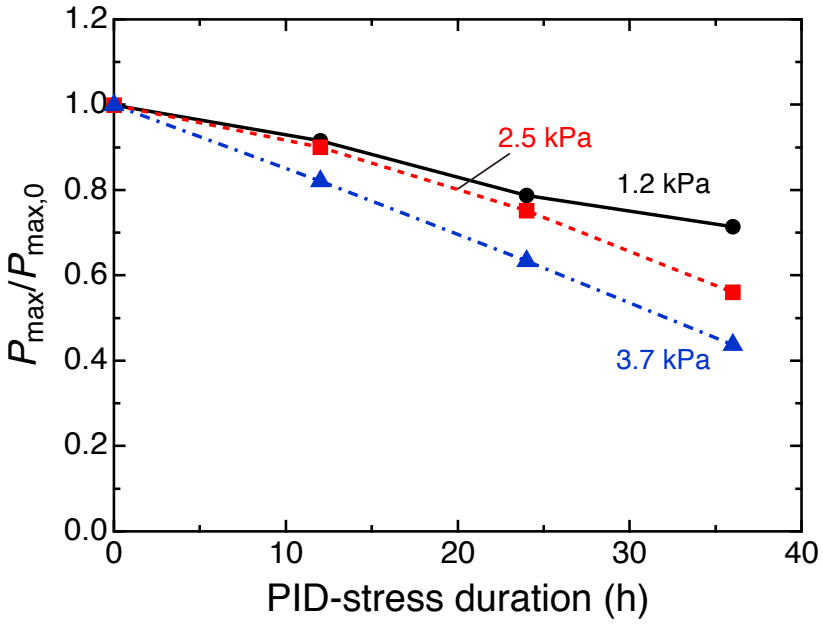
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0
10
20
30
40
$P_{max}/P_{max,0}$
PID-stress duration (h)
2.5 kPa
1.2 kPa
3.7 kPa

Fig. 3

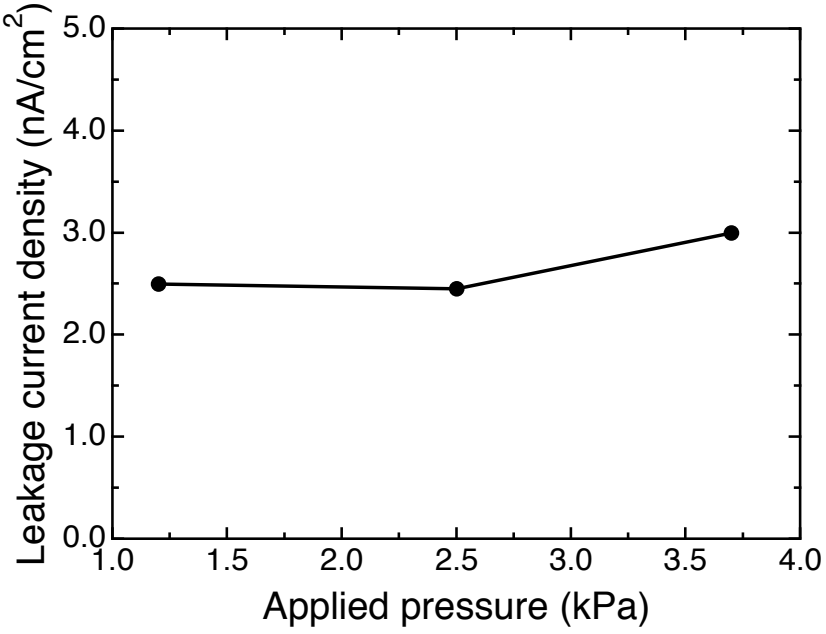
Leakage current density (nA/cm^2)
5.0
4.0
3.0
2.0
1.0
0.0
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Applied pressure (kPa)

Fig. 4

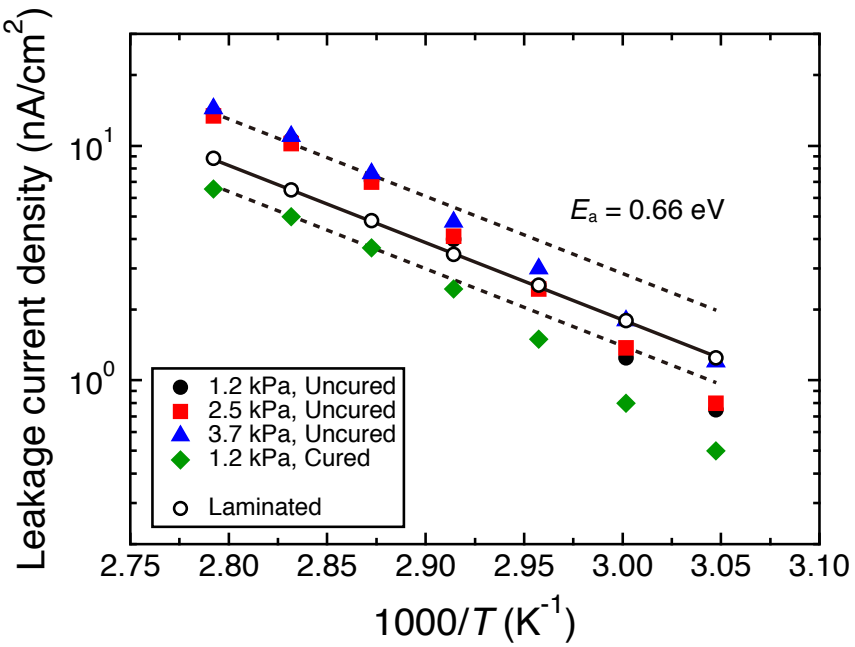
Leakage current density (nA/cm^2)
10^1
10^0
E_a = 0.66 eV
1.2 kPa, Uncured
2.5 kPa, Uncured
3.7 kPa, Uncured
1.2 kPa, Cured
Laminated
2.75
2.80
2.85
2.90
2.95
3.00
3.05
3.10
1000/T (K^{-1})

Fig. 5

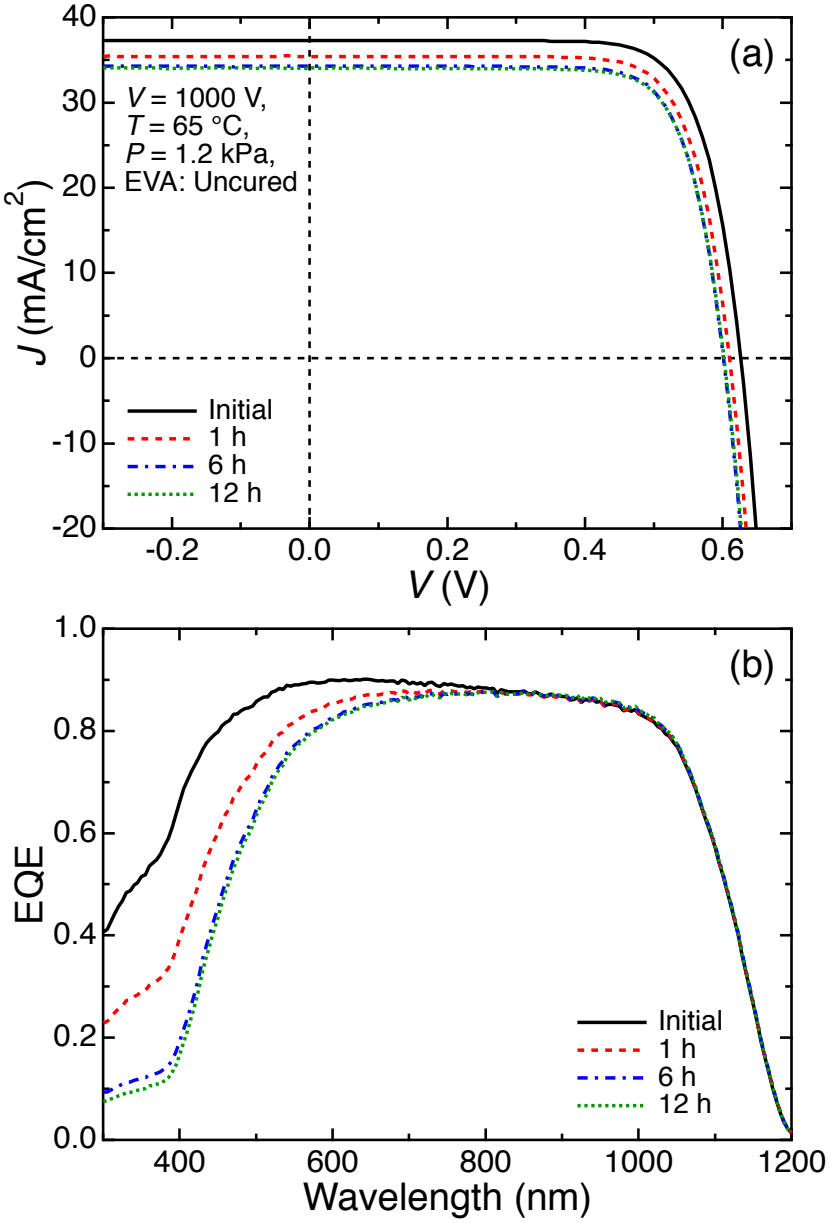
(a)
V = 1000 V,
T = 65 °C,
P = 1.2 kPa,
EVA: Uncured
Initial
1 h
6 h
12 h
J (mA/cm2)
V (V)
(b)
EQE
Wavelength (nm)

Fig. 6

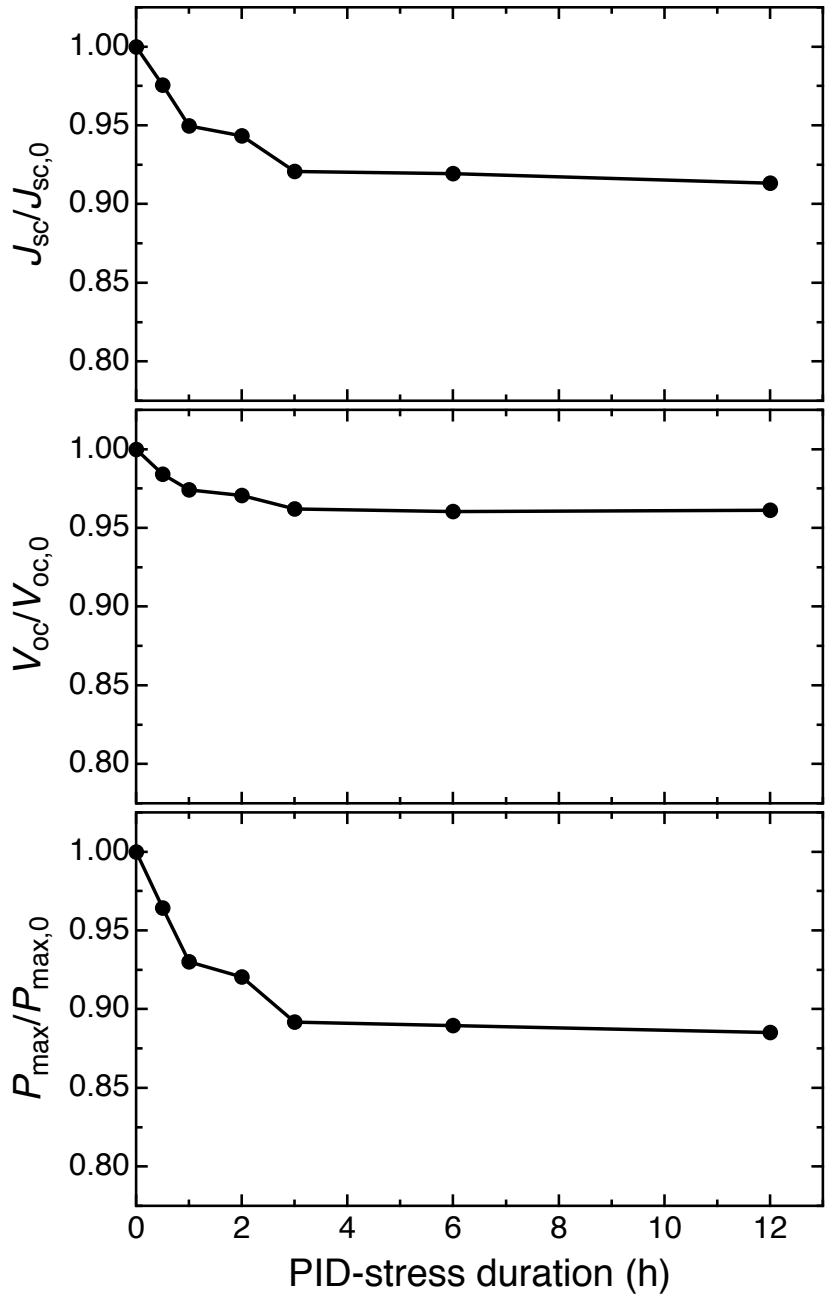
1.00
0.95
0.90
0.85
0.80
$J_{sc}/J_{sc,0}$
$V_{oc}/V_{oc,0}$
$P_{max}/P_{max,0}$
0
2
4
6
8
10
12
PID-stress duration (h)

Fig. 7