Accelerating the Image Retrieval using FPGAs

Etsuko TAKAMICHI (110072)

School of Information Science,
Japan Advanced Institute of Science and Technology

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The main contribution of this paper is to propose an FPGA-based instance-specific solution for an image retrieve problem. Given a gray-scale template image T and a database with a number of images $I_1, I_2, \ldots$, our system lists all images that contain a subimage similar to T.

An FPGA (Field Programmable Gate Array) is a programmable VLSI in which a hardware designed by users can be embedded instantly. Typical FPGAs consist of an array of programmable logic blocks, memory blocks, and programmable interconnect between them.

Our basic idea for accelerating computations using the FPGAs is inspired by the notion of "partial computation". Let $f(x, y)$ be a function that we have to evaluate to solve a problem. Sometimes, a function $f(x, y)$ is repeatedly evaluated only for a fixed x. If this is the case, the computation of $f(x, y)$ can be simplified by evaluating an instance-specific function f_x such that $f_x(y) = f(x, y)$. For instance, imagine a problem such that an algorithm to solve it evaluates $f(x, y) = x^3 + x^2y + y$ repeatedly. If $f(x, y)$ is evaluated only for $x = 2$, then we can simplify the formula such that $f_2(y) = 8 + 5y$. Actually, it is known that the multiplication of two integers can be done efficiently if one of the integers is fixed. The optimization of function f_x for a given particular x is called partial computation.

Usually, partial computation has been used for optimizing a function f_x in the context of software. Our novel idea is to built a hardware that is optimized to compute $f_x(y)$ for a fixed x and various y's.

Suppose that an image database containing a number of gray-scale images $\{I_1, I_2, \ldots\}$ and a template image T are given. We assume that T is small, say, 32×32 or 64×64 while each I_i is large, say, 1024×1024 or larger. We are interested in the task of listing all images in the database that contains a similar subimage to T. This task has many applications in the areas such as object recognition and vehicle tracking. The main contribution of this paper is to present an FPGA-based instance-specific hardware solution for this task. More precisely, let $D(T, I_i)$ denote a function that returns a value indicating the difference between T and I_i such that the value of $D(T, I_i)$ is small if I_i has similar subimage to T. Our idea is to embed a hardware that computes $D_T(I_i)$ $(= D(T, I_i))$ in a PCI-connected FPGA. We have developed a system that computes $D_T(I_1), D_T(I_2), \ldots$

using FPGA. Given a template image T, our hardware generator automatically creates a Verilog HDL source program which is designed for computing $D_T(I)$. More precisely, the generator is written in C-language, which generates a Verilog HDL source program for a gray-scale template image T in a few seconds. The source program is complied using a design tool provided by the FPGA vendor. The created hardware is embedded in the PCI-connected FPGA. The host PC sends images $I_1, I_2, \ldots$ stored in an image database to the PCI-connected FPGA. The FPGA computes the values $D_T(I_i)$ in turn, and returns each of them to the host PC. The host PC lists the images whose $D_T(I_i)$ is no larger than the threshold value.

We evaluate the performance of our image matching hardware using a PCI-connected Xilinx FPGA and a timing analyzer. The generated hardware attains a speedup factor of up to 3000 over traditional software approaches.

As an application of our circuit, we have developed a system that locates subimages in a database of images.