Floorplan Synthesis with Rearrangement of Hierarchical Structure

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The chip layout design in a VLSI(Very Large Scale Integrated circuit) design process is a task which determines the position of each cell in a two-dimentional plane and routes of interconnections between cells. Due to the increase of the number of components integrated into a single chip, hierarchical approach is now indispensable for designing layout.

In such approach, a hierarchical structure is usually given as a consequence of top down design from the system level to the logic (circuit) level, or it is generated by some partitioner. However, a hierarchical structure, which is convenient for system level design to logic level design or is generated only based on topological information, is not always a good one for layout.

The challenge tackled in this paper is to find a hierarchical structure suitable for layout and its floorplan. The method proposed in this paper is the incorporation of modifications of hierarchical structure into Force-Directed floorplanning.The aim of this approach is to use floorplan information of a current partition for improving partition.

Specifically, the problem is formulated as follows. A set of cells, its initial partition and net-list which represents the connection relation between cells are given as an input instance. The output of the problem is a partition of a set of cells which fulfills a given upper bound for the number of blocks

and an area limitation for each block and the position of each block so that the sum of estimated wire length becomes minimum. The estimation of wire length between two blocks is evaluated by the square of Euclidean distance multiplied by a weight which reflects connectivity between two blocks. Although this estimation may not be equivalent to the total wire length, it is often employed, since 1) it is continuous and differentiable on the variables, and 2) its minimization will suppress the occurance of a net with extremely long length.

On the Force-Directed method, for minimizing the sum of the square of wire length, a net between two blocks is considered as a piece of spring, and the position of each block is determined from equilibrium of the resillience of springs. The correctness of this opproach is derived from the fact that the value of square of wire length is equal to the value of the resillience of spring. However, this placement is ideal only on the mass system, thus it does not consider the overlap between blocks. For removing the overlap, repulsion between overlapping blocks is introduced, whose value is proportional to the area of overlapping, and moving and/or reshaping of block guided by the repulsion are employed.

The rearrangement of hierarchical structure uses the information of the precedence placement. In this paper, the rearrangement consists of merging two blocks into a single block and dividing a block int two blocks. On merger of two blocks, pairs of blocks, where the distance between them is less than a given the fixed value, are nominated as candidates for merging. The merger pair of blocks is selected from those candidates by evaluating connectivity and the distance between blocks. On division of a block, the division block is selected by evaluating the value of forces by nets. Two new blocks are obtained by 1) cells in the selected block are placed to their ideal positions by the Force-Directed method on the mass system, 2) evaluating the number of nets cut by cutline with the various direction, and 3) bi-partitioning a set of cells by the cutline which cuts the minimum number of nets. In this paper, the block obtained by the merger is not selected as the division block and the blocks by the division are not selected as the merger blocks for several times, for the prohibitation that the same blocks are selected repeatedly as merger and division.

To solve the problem, the following two methods are proposed. One

is "Modification and Local refinement (ML)" method and the other is "Modification and Retry (MR)" method. ML decides the positions of the new blocks obtained by merging or dividing as the position of original block and removes overlaps by moving and reshaping blocks. On the other hand, MR restarts the placement on the mass system after the rearrangement of hierarchical structure.

To ensure the efficiency, the above methods are implemented. For benchmark data, the proposed method achieves 9.9–21.0 % improvement compared with a conventional topological partitioning followed by Force-derected floorplanning.

In the future works, the improvement of the selection algorithm of the merger/division blocks and its implementation are needed. Furthermore, for the consideration of the performance driven layout, that is, the minimization of the signal propagation delay and the power comsumption, etc., more suitable merger and division method are required.