A Logic Circuit Design Method to balance delays considering Placement and Wiring for Wave-Pipelining

Yoshinori Miyamae (110117)

School of Information Science,
Japan Advanced Institute of Science and Technology

February 14, 2003

Keywords: Wave-Pipelining, Delay Balancing, Delay Difference, Placement/Routing.

1 Introduction

This paper proposes a logic circuit design method to reduce the delay difference among signal paths for the Wave-Pipeling architecture. The Wave-Pipelining architecture is one that improves the operating frequency of LSI circuits beyond switching speed of devices which depend on Scaling of the device.

The technology of the LSI Circuit including microprocessor has been progressing in accordance with Moore's Law. The performance improvement has been accomplished in particular, by scaling. Meanwhile conventional technologys is being limited by many physically factors. It is necessary to create a novel circuit design method that breaks physical limitation of devices and wiring.

2 Wave Pipelining Architecture

In conventional synchronous pipelined circuits, the clock period of the circuit is restricted with the maximum propagation delay of them. On the other hand, in wave pipelined circuits, the clock period is allowed to

the difference between the maximum and minimum propagation delay[2]. Compared with the conventional synchronous pipelined circuit, the wave pipelined circuit has the advantage that makes the operating frequency of the circuit much higher.

3 MOSFET Model and a Delay Evaluation Method

In this chapter, the simple MOSFET model ,logic device model, and the evaluation method of a circuit delay is described. The delay difference is classified into three constituents according to what causes the difference:1)the characteristic difference of characteristics between nMOS and pMOS, 2)the environment variation of operating, and 3)The variety of input patterns to logic components.

Device parameters of MOSFET is decided from the simple transition model and some physical laws. The parameters are especially restricted to important values to construct the simple MOSFET and layer model.

The delay evaluation model is expressed with the logic component delay model and wire delay model. The logic component model consists of a on-resistance, diffusion capacitance and input capacitance. The wire delay model consists of wire resistances and wire capacitances, using Distributed RC Delay Model[3]. The constructed delay model does not simulate the signal wave form propagating the wire but evaluates the time that the output voltage amounts to a certain value.

In conclusion, the delay difference caused by a whole circuit is distinguished from the following characteristics:

1. the delay difference in a path caused by:
   (a) the variation of input patterns at every element
   (b) the variation of operating environments
2. The delay difference among paths caused by:
   (a) the variation of the number and kind of elements, and the wire length of a path

In this paper, the factor 1-(a) and 2-(a) is targeted in delay balancing.

4 Potentials of Wave Pipelining on CMOS

In this chapter, potentials of wave- pipelining on CMOS are discussed. In the beginning, Nowka's study about potentials in a long-channel MOSFET model is discussed[5][4]. Two parameters $\mathcal{A}$ and $\mathcal{B}$ are introduced to show effects of the delay difference according to factors. The parameter $\mathcal{A}$ is to evaluate the degree of the delay difference caused by the variation of each path length, and the parameter $\mathcal{B}$ is introduced to evaluate the degree caused by the variation of operating environment.

To discuss the potential of a deep sub-micron device, the ideal circuit of which each path is balanced in wave pipeline is shown. Then, the simple parameter $\mathcal{B}'$ is defined as the minimum to the maximum on-resistance ratio. In the ideal circuit, the parameter $\mathcal{B}$ is equal to $\mathcal{B}'$. $\mathcal{B}$ is 1 when stabiligation of the variation of operating environment is considered.

Last, $\mathcal{B}'$ is calculated from parameters that is used in actual production[1], shows that wave-pipelined circuit can be operated at the latency of about 40% to the maximum propagation delay.

5 A Delay Balancing Method focusing on the Delay Difference in an Element

The delay balancing method focusing on the delay difference in an element has four strategies on inverter insertion

1. α insert: to reduce the direct load of an element.
2. β insert: to rise the speed of an element.
3. γ insert: to hold the delay balance among paths.
4. δ insert: to take adjustment logically.

The method has also other strategies: Decomposition Strategy to operate flexible buffer insertions, Resizing Strategy to control an element speed, Exchanging Strategy to minimize the size of the inserted inverter, and Re-Connecting Strategy to minimize the delay difference produced by the variation of the on-resistance and diffusion capacitance among pins.

In the 1-bit-full-adder, the wave-pipelined 4bit-ALU that applied the method can operate on the frequency about three times higher than the conventional-pipelined one under an ideal device.

6 A Delay Balancing Method considering placement and wiring problem

The delay balancing design between the netlist level independent of technology and the placement and wiring design level is introduced as the method considering placement and wiring problem.

First, the method operates the placement virtually at the netlist level. The method puts a pair of inverters so that any path in the circuit passes through elements only the same number. Elements have the level respectively, and the element of the same level is placed on the same axis. After that, the method operates the placement virtually so that the element of the same stage may have the wiring of the same length mutually. Concurrntly, the load partition strategy is applied.

Second, the method operates the Alpha/Beta insertion when the technology mapping by creating the unit that consists of the targeted element and Alpha/Beta buffer in the same cell, called Block. The size of the Alpha buffer is the smallest inverter in the library, and the Beta buffer is variable according to the length of the wire which each element has.

The wave-pipelined 4bit-ALU that applied the method can operate on the frequency 2.39 times higher than the conventional-pipelined one.

7 A Delay Balancing Method for arbitrary circuit

The method is applied to the 32-bit ALU and the 16-bit Multiplier to check the effect of the constructed method to a large circuit. In both the 32-bit ALU, unbalanced with respect to the number of the stage of each path, and the 16-bit ALU, balanced roughly with respect to it, each circuits that applied the method can operate on the frequency about twice higher than the conventional-pipelined circuit.

8 Conclusion

Whether the original circuit is balanced or unbalanced with respect to the number of the stage of each path, the delay balancing method in this paper can accomplish the compression of the delay difference according to the length variation of each path enough to judge that the balance of operating environment should be considered to get more performance. In addition, this method can design the delay balanced circuit from the architectural design level to the placement and wiring design level without the feedback of the design flow.

References

[1] The MOSIS service, http://www.mosis.org/.

[2] W.P. Burleson, M. Ciesielski, F. Klass, and W. Liu. Wave-pipelining: A tutorial and research survey. *IEEE Transactions on VLSI Systems, Vol.6, No.3, Sep.'98, pp. 464-470.*, 1998.

[3] J.Rubinstein, P.Penfield Jr, and M.A.Horowitz. Signal delay in RC tree networks. *IEEE Trans. Computer-Aided Design Integrated Circuits Syst*, Vol. CAD-2, pp. 202–211, July 1983.

[4] Kevin J. Nowka. High-performance CMOS system design using wave pipelining. Technical Report CSL-TR-96-693, 1996.

[5] Kevin J. Nowka and Michael J. Flynn. Environmental limits on the performance of CMOS wave-pipelined circuits. Technical Report CSL-TR-94-600, 1994.