Reaearch on Clock Distribution of a Wave-Pipeling Processor

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1 Introduction

The ultimate target of this research is improvement in a performance of a processor. A more highly efficient processor is aim. Frequency of operation is an important parameter as a performance index of a processor. A pipeline is an important technique because of improvement in frequency of operation. This research clarifies the method of clock distribution about the circuit which uses the wave pipeline. When spreading a clock signal from the same clock sauce, a delay buffer is inserted between a certain stages and next stages, and clock timing is adjusted to it. The quantity to adjust is made to meet at the minimum delay time between a pipeline's stages. Since change of the time out of which an operation result comes size-comes to come so that a stage increases, it is necessary to allot by the clock so that a wave pipeline may operate well.

In this research, it proposes applying to an Placement/Routing stage from clock distribution circuit composition to a wave pipeline, and performing distribution optimization.

2 A Wave Pipeline's Principle of Operation

In the usual pipeline, a clock enters and comes out of each stage at this time, it receives that a certain clock cycle serves as the maximum delay. In the case of a wave pipeline, a clock cycle is considered as determination with the difference of the maximum delay and the minimum delay. To the synchronous formula circuit from the former which can be shortened, a clock cycle can perform overthrow of a clock limit and can be called architecture with a possibility of making it operating at high speed.

3 The Character and the Evaluation Method of MOSFET

The fundamental character of MOSFET was described at first. Moreover, the used analysis method is a thing as the foundation for it being notionally exact although simplified, and solving most problems of an accumulation system.

In carrying out the simulation of the circuit, a setup and formula of MOSFET and a parameter were shown, and evaluation of delay was considered in the evaluation method. It calculates and asks for delay of MOSFET based on a factor physical from the first. Change of conditions of operation and professional wrestling, then the cause of skew were clarified. The cause of delay is analyzed from the characteristic of MOS. There is mainly a cause of two and they are gate delay and wiring delay. Although wiring delay is not changed, since degree of movement μ, the gate width W, and the gate length L change, gate delay is changed by process change. Moreover, since temperature and voltage change with change of conditions of operation, delay is changed.

In developing the argument on the possibility of the wave pipeline on CMOS, about the design, model construction was carried out and the characteristic was evaluated for the buffer of delay through the easy simulation by HSpice.

4 Consideration about Placement/Routing

Development of the semiconductor process which enables more detailed processing is carrying out the biggest contribution to the improvement in a performance of a microprocessor. also making wiring detailed, although frequency of operation will improve by proportionality reduction, if detailed-ization of an integrated circuit progresses area in a fixed case, wiring delay will increases.

About aluminum wiring, the easy model was built and the characteristic was evaluated through the simulation by HSpice.

The RC circuit · track was analyzed and RC concentration constant was analyzed for the purpose of considering how approximating in easy RC concentration constant circuit. When the terminus especially of the receiving end was carried out by capacity nature load, the formula of the response characteristic was considered about 1 step of RC circuit. Moreover, the formula which asked for delay evaluation of a limited length RC track was examined.

Therefore, as for wiring, the process evaluated delay to change. The cause of skew of wiring was considered. When wiring was short, even if there was skew of 10 %, change of wiring delay showed clearly that there are very few portions which affect the whole to 10 % skew of MOSFET.

The proposal and evaluation of a wave pipeline processor of the clock distribution technique It proposed performing distribution optimization, being based and applying a wave pipeline's principle of operation, MOSFET, and Placement/Routing to an Placement/Routing stage from clock distribution circuit composition to a wave pipeline. The clock distribution system for inserting a delay buffer between a certain stages and next stages, adjusting clock timing to it, and giving exact timing to it, when spreading a clock signal from the same clock source having been established . The method of clock distribution was clarified about the circuit which uses the wave pipeline.

A concrete wave pipeline processor Placement/Routing and skew containing a processor on the whole, clock distribution were designed and evaluation and examination were performed.

It is Examination of the Clock Distribution Technique to Atrbitrary Wave

Pipelines' Circuit.

Since the stage of a wave pipeline processor increases, change of the time out of which an operation result come size-comes to come. In the here, including skew, clock distribution of a wave pipeline processor were considered with analysis, and the solution method was proposed.

5 Conclusion

It will be secured by the clock distribution technique proposed by this research that a wave pipeline operates well. It is the foundations of development how a cycle time is reduced as a factor of a performance. Shortening of a cycle time is made in pipeline technology, circuit technology, etc. by improvement in usage operation frequency. the number of theoretical stages of a former pipeline stage was reduced, and the number of stages was increased in a deep pipeline, 1 clock 1 command achievement cannot be carried out, but efficiency falls The usual pipeline determines the limit of a clock frequency in maximum delay time between stages. Since all stages need to operate to the same timing, they become difficult in clock distribution. The high-speed CPU architecture was enabled to insert a delay element and to realize distribution of a clock by a wave pipeline's view, also including skew and Placement/Routing.

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