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Description	

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Effects of passivation configuration and emitter surface doping concentration on polarization-type potential-induced degradation in n-type crystalline-silicon photovoltaic modules

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Abstract

System voltages can cause significant degradation in photovoltaic modules. Polarization-type potential-induced degradation (PID) is accompanied by decreases in the short-circuit current density and the open-circuit voltage. The system voltage causes a polarization and surface charge accumulation, increasing the interface recombination. The surface passivation and the emitter doping concentration and gradient are considered to have large impacts. However, a systematic study on these effects has not yet been performed. In this paper, the effects of the front surface structure of n-type passivated emitter and rear totally diffused cell modules were investigated by accelerated PID tests. Standard cells with thin silicon dioxide/80 nm silicon nitride (SiN_x) antireflection/passivation layers, refractive index (RI) of 2.0, exhibited typical polarization-type PID. Cells with increased RI = 2.4 for the bottom 20 nm SiN_x showed no degradation at all. This may be caused by reduced charge accumulation in the SiN_x layer near the interface due to the higher electrical conductivity of the Si-rich bottom layer. Secondly, cells with both a highly distorted interface, due to nitrogen insertion in the silicon surface, and an emitter with a high surface doping concentration have excellent resistance to PID. Cells with either the highly distorted interface or the higher emitter-surface doping concentration show no to minor improved resistance to PID. These findings improve the understanding

of the effects of the front surface structure of cells on the polarization-type PID and may contribute to the implementation of these measures to reduce PID.

Keywords: Polarization-type potential-induced degradation; Photovoltaic module; n-type crystalline-silicon solar cell; Passivated emitter and rear totally diffused cell; Reliability; Acceleration test

1. Introduction

Crystalline-silicon (c-Si) photovoltaic (PV) cells fabricated on n-type c-Si wafers, so-called n-type c-Si PV cells, have attracted attention because of their potential to obtain higher power-conversion efficiencies than those of p-type ones. These n-type c-Si PV cells have high-quality n-type base materials, where the minority-carrier lifetimes are generally long because of the small impurity capture cross-sections for minority carriers [1]; this leads to higher cell efficiencies than those of p-type ones [2]. In addition, they are known not to suffer much from light-induced degradation, that is caused by the formation of metastable boron–oxygen complexes [3, 4], as frequently observed in conventional p-type c-Si PV cells. Consequently, n-type c-Si PV cells display superior long-term photostability over p-type ones and may therefore be suitable for use in large-scale PV systems.

However, to utilize these cells in large-scale PV systems, it is very important to understand the behaviors and mechanisms of their potential-induced degradation (PID) [5–10]. PID is triggered by potential differences between grounded frames and the active circuit of cells in modules. One of the features is that large degradation appears in a relatively short time, such as several months, in the field. The PID is therefore considered one of the most important reliability issues of large-scale PV systems.

In particular, polarization-type PID is known to be the fastest degradation mode out of the PID modes. It has been observed in several types of c-Si cells including n-type passivated emitter and rear totally diffused (PERT) cells [11–19], n-type interdigitated back-contact cells with front surface field [20, 21] or with front floating emitters [22], in p-type passivated emitter and rear cells [18, 23] and p-type conventional c-Si cells [24]. The polarization-type PID is known to be characterized by reductions in the short-circuit current density J_{sc} and the open-circuit voltage V_{oc}. The PID has been reported to start within the first seconds in an accelerated PID test in which a bias of −1000 V is applied at 85°C [12, 13]. Additionally, it occurs even when the applied voltage in the PID test is very low, for example −50 V [11]. This means that this kind of PID can occur in small-scale PV systems with relatively low system voltages.

As for the mechanism, it has been proposed that the polarization-type PID is caused by positive (or negative) charge accumulation in the front SiN_x layers of solar cells [20]. The accumulated charges attract minority carriers and enhance interface recombination via interface defects, leading to reductions in the J_{sc} and the V_{oc} [20]. Positive ions such as Na^+ ions [17] and charged K centers in SiN_x [12, 13] have been proposed so far as charge sources causing polarization type PID. On the basis of the above mechanisms, the surface passivation configuration and the emitter doping concentration and gradient are considered to have large impacts. There have been some reports discussing the effect of the surface passivation configuration [15, 18, 24, 25]. Janssen and coworkers [25] have reported that a SiN_x antireflection/passivation stack with a bottom layer with a high refractive index (RI) effectively reduces polarization-type PID. However, a systematic study has not yet been performed on the effects of the surface passivation configuration and the emitter doping.

Here, we report and discuss the effects of the surface passivation configuration and the surface doping concentration profile on polarization-type PID in modules with n-PERT cells. We prepared five different kinds of cells with different

passivation configurations and emitter-surface doping concentrations. We performed accelerated PID tests on the cells. After comparing the results, we discuss their effects on the polarization-type PID. n-PERT cells have been reported to show sodium-related degradation which occurs with different mechanisms from polarization-type PID [14, 26]. However, the sodium-related degradation is not addressed in this paper.

2. Experimental procedures

2.1. Solar cell and module

We prepared five different kinds of bifacial front-emitter n-PERT cells summarized in Table I. The basic structure of the front-side of the cells is schematically shown in Fig. 1. Note that all the cells had the same, 80-nm single-layered SiN_x, rear surface passivation structures. The solar cells are made of pseudo square wafers with sizes of 156 × 156 mm^2. All the SiN_x layers were deposited by plasma-enhanced chemical vapor deposition (PECVD). It is noted that all the cells have thin ~1.5 nm thick SiO_x layers between the Si and the SiN_x layer. The SiO_x thin layers were formed by the nitric acid oxidation of Si (NAOS) technique [27]. We fabricated solar cells with a standard SiN_x layer and a standard emitter. The standard SiN_x layer is an 80 nm thick SiN_x layer with an RI of 2.0 and the standard emitter is a boron-doped front emitter with a boron-depleted surface region. These standard solar cells were always used as references in this study. Solar cells with a different dielectric layer and/or a different emitter were also prepared.

To investigate the influence of the passivation configurations on polarization-type PID, we fabricated two different SiN_x layers next to the standard SiN_x layer. One is a passivation stack composed of 60 nm thick SiN_x top layer with an RI of 2.0 and 20 nm thick SiN_x bottom layer with an RI of 2.4 (Fig. 2). (The bottom layer will also be referred to as the "high-RI interlayer" in this paper.) The other is a SiN_x layer with a plasma-deposition-damaged (distorted) interface originating from the nitridation in the PECVD process. The nitridation is additional plasma treatment prior to the actual SiN_x deposition. (The details of the nitridation step are given in Refs. 28 and 29.) It is known that atomic-scale Si-rich thin layers are formed in the immediate vicinity of the distorted interface [28, 29].

As for the emitter, we prepared a surface-etched emitter to compare with the standard emitter. The surface-etched emitter is made by etching away the boron-depleted region. This results in a surface doping concentration that is expected to be higher than that of the standard emitter.

The full-size cells with dimensions of 156 × 156 mm^2 were cleaved into small cell pieces with dimensions of 20 × 20 mm^2 and standard interconnector ribbons were soldered onto the busbars on both sides of the cells. After soldering, we prepared stacks composed of conventional cover glass/ethylene–vinyl acetate copolymer (EVA) sheet/cell/EVA sheet/typical white backsheet. Mini-modules were prepared by laminating the stacks in a module laminator. The lamination process consisted of a degassing step for 5 minutes and an adhesion step for 15 minutes. The stacks were placed on a stage maintained at 135°C during both steps.

2.2. PID test and characterization

Accelerated PID tests on the fabricated PV modules were performed by applying a bias of −1000 V to shorted interconnector ribbons with respect to a grounded aluminum plate placed on the cover glass via an electrically conductive rubber sheet in a chamber maintained at 85°C. All the PID tests were conducted in the dark. Polarization-type PID in n-PERT cells is known not to be largely influenced by illumination [18]. The humidity in the chamber during the PID test was not controlled; however, the relative humidity in a similar setup was very low (<2%) [30]. Thus, the influence of moisture ingress was disregarded in this study.

To evaluate cell degradation, current density–voltage (J–V) measurements in the dark and under one-sun illumination, without spectral mismatch correction, were performed before and after the PID tests. External quantum efficiency (EQE) measurements were also performed before and after the PID tests. All the measurements were conducted at 25°C.

3. Results

It has been reported that polarization-type PID is affected by the layers near the front surface such as the presence of a thin SiO_2 layer or the composition of the SiN_x stack [15, 24, 25]. In this study, we investigated the front surface passivation stack and the emitter surface doping concentration in the n-type c-Si PV cell modules to understand their effects on the polarization-type PID in c-Si PV modules.

Table I also summarizes the solar cells' initial performances. This information is important for developing measures to prevent the polarization-type PID. In this experiment, the standard cell has the lowest efficiency of 18.5%. On the other hand, the other cells have higher efficiencies of 19.6–20.0%. Applying these non-standard passivation configurations and emitter does not at least reduce the solar cells' performances.

3.1. Effect of high-RI interlayer

Fig. 3 shows the normalized maximum output power, $P_{max}/P_{max,0}$, of PV modules fabricated from the standard n-type c-Si cells and cells with the SiN_x layer with the high-RI interlayer, where P_{max} is the maximum output power and $P_{max,0}$ is the initial P_{max}. The standard cell modules showed the typical degradation behavior characterized by reductions in J_{sc} and V_{oc}. After the PID test for 180 s, the normalized J_{sc} and V_{oc} were approximately 0.943 and 0.958, respectively. Similarly as in the previous work [12, 13], these reductions were accompanied by a decrease in the EQE in the short wavelength region (not shown here). On the other hand, the PV modules fabricated from cells with the high-RI interlayer showed no significant changes in $P_{max}/P_{max,0}$. The stable performance could result from the increase in the conductivity caused by the change in chemical composition of the high-RI SiN_x interlayer as discussed in the Discussion, section 4.1.

3.2. Effect of emitter surface doping concentration

Fig. 4a shows $P_{max}/P_{max,0}$ of PV modules fabricated from cells with the standard emitter and with the surface-etched emitter. Shown in Fig. 4b are the active dopant profiles of the standard and surface-etched emitters acquired from electrochemical

capacitance–voltage (ECV) measurements. The standard emitter has a boron depletion region at the interface; on the other hand, the surface-etched emitter has a higher surface doping concentration since its boron depletion region has been removed. Both cells exhibited the typical polarization-type PID behavior. The cells with the surface-etched emitter, however, were degrading more slowly than the standard cells. Moreover, after the saturation of the degradation, the degree of degradation of the cells with the surface-etched emitter is somewhat smaller than that of cells with the standard emitter.

3.3. Effect of distorted interface

Fig. 5 shows $P_{max}/P_{max,0}$ of PV modules fabricated from the standard cells, cells with a distorted interface, and cells with both a distorted interface and with the surface-etched emitter. The effect of cells with only the modified emitter process is shown in Section 3.2 and Figure 4. It is known that atomic-scale Si-rich thin layers are formed in the immediate vicinity of the distorted interface [28, 29], which may cause a higher electric conductivity in the immediate vicinity of the interface. From Fig. 5, applying the SiN_x with distorted interface has no effect on the progression of the PID. This indicates that introducing the distorted interface alone does not effectively reduce the PID effect. However, by applying both the SiN_x with distorted interface and the surface-etched emitter, which has a high surface doping concentration, the degradation can be effectively reduced.

4. Discussion

4.1. Effect of high-RI interlayer

The polarization-type PID is known to be caused by charge accumulation in the front SiN_x passivation layers. On the basis of this, the properties of the front SiN_x passivation layers are very important. In this section, we will discuss the effect of the use of high-RI SiN_x interlayers. The concept of the high-RI SiN_x interlayers has already been presented in Ref. [25]. Here, further discussion based on carrier transport between the emitters and the interlayers is provided.

As shown in Fig. 3, the modules fabricated from cells with the passivation stack including the high-RI SiN_x interlayer, see Fig. 2, showed almost no degradation due to the applied potential difference. This means that the high-RI SiN_x interlayer effectively prevents polarization-type PID. The polarization-type PID is known to be due to charge accumulation in the front SiN_x layers in the vicinity of the c-Si interface [11–13, 20]. Although the chemical composition is not determined here, the RI is widely used as an indicator of the chemical composition. High-RI SiN_x layers are Si-rich and have a higher conductivity than those of near-stoichiometric SiN_x layers. Thus, the high-RI SiN_x interlayer will result in a high (surface) conductivity, and the interlayer enables carrier transport between itself and the c-Si. This effectively reduces charge accumulation and therefore reduces or even prevents the PID effect.

The properties of the passivation layers inserted between the interlayer and the c-Si emitter will also be very important when the above PID suppression effect is used as a measure to prevent the polarization-type PID. For example, front-emitter n-type c-Si PV cells have thin passivation layers, such as SiO_x or AlO_x, underneath

the SiN_x antireflection/passivation layers. The SiO_x passivation layers have been reported to play an important role in maintaining accumulated charges in the SiN_x layers [12, 13, 15, 24]. If such layers are sufficiently thick and dense to suppress carrier transport between the SiN_x and the c-Si, the PID suppression effect by the use of a high-RI interlayer may disappear. We confirmed that the PID suppression effect did not occur in front-emitter n-type c-Si PV cells with relatively thick thermally grown oxide layers even when high-RI SiN_x layers were used. Fig. 6 shows $P_{max}/P_{max,0}$ of PV modules fabricated from n-type front-emitter c-Si cells with SiN_x antireflection/passivation layers with RIs of 2.03, 2.20, and 2.34 before and after PID tests where a negative bias of −1000 V was applied. (Note that in this experiment, single-layered SiN_x films deposited on SiO_2 were used.) All the cells had thermally grown ~10 nm SiO_2 layers between the SiN_x layers and the emitters. All the modules show almost the same degradation behaviors regardless of the RI of the SiN_x layers, and no prevention effects are observed, unlike in the case of sufficiently thin SiO_2 prepared by the NAOS process. This implies that the use of thick and dense SiO_2 layers invalidates the PID prevention effect of high RI SiN_x layers. This may be because the thick and dense SiO_2 layers effectively reduce charge carrier transport between the emitters and the SiN_x films. This result indicates that the high-RI interlayers should be applied together with sufficiently thin SiO_x layers (or other layers) which enable carrier transport via tunneling. Additionally, such layers should also have a good passivation quality for the initial performance. The thin SiO_x layers fabricated by the NAOS technique [27] can satisfy these requirements and are a promising material for high performance and highly reliable PV modules. An additional systematic study has to be performed for better understanding of the effects of the thickness and the fabrication method of SiO_2.

One of the advantages of the use of the SiN_x stack is that the initial cell performance is retained. It was possible that the use of the Si-rich SiN_x interlayer leads to a J_{sc} reduction due to an enhancement in parasitic absorption. However, as shown in Table I, such an unfavorable effect was confirmed not to occur. The reason is not clear at present, and, however, it might be caused by an improved antireflection property of the stacked SiN_x layers. Additionally, the SiN_x stack can be readily realized only by changing the gas flow ratio during the PECVD process. This is also another great advantage of this measure. These indicate a high industrial feasibility of the preventive measure.

4.2. Effect of emitter surface doping concentration

On the basis of the proposed mechanism, also the properties of the emitter-surface region are important, for instance the surface doping concentration and the surface recombination velocity. Here we discuss the effect of the emitter-surface doping concentration on the polarization-type PID.

In Fig. 4, it is shown that having a surface-etched emitter, with higher surface doping concentration, decreases the rate and degree of degradation compared to an emitter with a boron depletion region but higher concentration deeper below the surface. The observation in Fig. 4 may be related to the influence of the charge accumulation and associated electric field on the surface band bending. The SiN_x

passivation layers of both cells are the same, leading to the same strength of electric fields originating from the accumulated charges in the SiN_x passivation layers. Given that the electric field strength is the same, the higher the emitter surface doping concentration, the smaller the degree of the surface band bending due to the electric field. Therefore, cells with an emitter with a high surface doping concentration will exhibit less surface band bending and are thus considered to be more resistant to polarization-type PID. Note that the emitter profile is important as well, in particular for emitters with depletion region.

This result also implies that solar cells involving so-called selective emitters will be sensitive to polarization-type PID. This is because such kind of cells have low emitter surface doping concentrations and a decreasing concentration with increasing depth. These cells are thus considered to be sensitive to electric field caused by accumulated charges in the SiN_x layers. Therefore, measures to reduce the polarization-type PID are even more important in selective-emitter cells. One candidate is the use of high-RI SiN_x interlayers.

Etching of the boron depletion region might be a measure to reduce the polarization-type PID. However, as shown in Fig. 4a, the effect is relatively small. To effectively reduce the PID effect, either another measure should be combined with the surface-etched emitter, or emitters with even higher concentrations should be used. The combination with the distorted interface may be a candidate (cf. the next section).

4.3. Effect of distorted interface

SiN_x layers with distorted interfaces, due to nitridation after the NAOS step, are known to have atomic-scale Si-rich layers in the immediate vicinity of the interface, leading to a high electric conductivity near the interface. It is therefore expected that there is an effect similar to that of the use of high-RI interlayers. To investigate the effect of the distorted interfaces, we performed PID tests of modules fabricated from cells with single RI = 2.0 SiN_x layers with highly distorted interfaces.

As shown in Fig. 5, modules with cells with distorted interfaces showed almost the same trend with the modules with standard cells. This indicates that the distorted interface alone does not have an effect on polarization-type PID. The effect of applying the surface-etched emitter alone was displayed in Fig. 4 and discussed in Section 4.2, and also in this case, a very large effect to reduce PID was not observed. However, when both the distorted interface and the emitter with a high surface doping concentration were applied, the polarization-type PID was effectively reduced (cf. “Distorted interface + Surface-etched emitter” in Fig. 5) to near zero. These results indicate that the individual effects of the distorted interface and the emitter with a high surface doping concentration are small, but a large effect can be obtained by combining both. This might result from combination of high electrical conductivity in atomic-scale Si-rich thin layers at the interface and applied-electric-field insensitivity caused by a high surface doping concentration of the emitter. However, additional work is required to understand the effect of the distorted interface.

4.4. Potential measures to prevent polarization-type PID

From the practical point of view, it is very important to develop measures to prevent polarization-type PID that are industrially applicable. The most effective measure in this study may be the use of the high-RI interlayer. As shown in Fig. 3, the cells with the interlayer showed no degradation. In addition, this method is considered to be cost-effective because high-RI interlayers can be realized by slightly changing the ratio of source gases in the PECVD process. On the other hand, the measure cannot work effectively when a thick, dense passivation layer, such as thermally grown SiO_2, is applied underneath the interlayer. This is because such SiO_2 layers behave as barrier layers for electron transport between the interlayer and the c-Si emitter. Sufficiently thin SiO_2 layers must therefore be used, like SiO_2 layers fabricated by the NAOS technique [27] that realizes very thin SiO_2 passivation layers with excellent passivation qualities.

As discussed in Section 4.3, by applying both the distorted interface and the emitter with a high surface doping concentration and continuous decreasing concentration below the surface, the polarization-type PID can be reduced effectively. It can therefore be a preventive measure. For this measure, an additional process is needed to realize the high surface doping concentration. The etching of the surface depletion layer, however, not only improves PID resistance but also leads to a higher initial performance. The surface depletion layer is accompanied by a high minority carrier concentration and results in a low minority carrier lifetime. Therefore, the removal of the surface depletion layer leads to a higher V_{oc}. Actually, the standard cell has an efficiency of 18.5% whereas the cell with the surface-etched emitter has a higher efficiency at 19.8%. The PID-delay effect of the high emitter-surface doping concentration is expected to remain even with a thick, dense passivation layer underneath the SiN_x layer. However, it is unclear whether the effect of the SiN_x layer with the distorted interface remains or is annulled when such a thick SiO_2 layer is used. We will have to investigate the application range of the distorted interface in more detail.

5. Conclusions

In this study, we have investigated the effects of the passivation layer configurations and of the emitter surface doping concentration on the polarization-type PID of modules with front-emitter n-PERT cells. The standard cells have boron-doped front emitters passivated by stacked layers composed of 80 nm top SiN_x layers with an RI of 2.0 and a thin SiO_2 bottom layer prepared by the NAOS technique. The modules with standard cells show polarization-type PID which is characterized by rapid reductions in J_{sc} and V_{oc}.

Modules fabricated from cells with a stacked SiN_x layer composed of a 60 nm SiN_x top layer with an RI of 2.0 and a 20 nm SiN_x bottom interlayer with an RI of 2.4 did not exhibit polarization-type PID. The RI of 2.4 interlayer has a high conductivity, which enables carrier transport between itself and the c-Si emitter. This reduces accumulated charges in the interlayer, and therefore reduces the polarization-type PID. Additionally, it was also implied that the high-RI interlayers should be applied together with sufficiently thin SiO_x layers which enable carrier transport via tunneling.

The cells with the distorted interfaces underneath the SiN_x passivation layer

showed a very similar degradation behavior as PID-prone cells. The distorted interface alone therefore seemed not to improve the PID resistance. Furthermore, we found that cells with a high emitter surface doping concentration and continuous decreasing concentration below the surface have a moderate resistance to polarization-type PID. The improvement of PID resistance is because the increased majority carriers reduce band bending caused by the electric field created by accumulated charges in the front SiN_x layers. Although both measures individually lead to, at best, a small reduction in PID, the PID was fully prevented by combining the distorted interface with the emitter with a high surface doping concentration.

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Figure captions

Fig. 1. Schematic diagram of the basic structure near the front surface of cells used in this study.

Fig. 2. Surface passivation configurations of (a) the standard cell and of (b) the cell with the high-RI interlayer.

Fig. 3. $P_{max}/P_{max,0}$ of modules fabricated from cells with the single-layered 80-nm-thick SiN_x with an RI of 2.0 and with the double-layered SiN_x composed of the 60-nm-thick SiN_x top layer with an RI of 2.0 and the 20-nm-thick SiN_x interlayer with an RI of 2.4, as a function of PID-stress duration. The data points show the mean values for the three modules, and the error bar corresponds to the standard deviation of the mean. The solid and broken lines are guides to the eye.

Fig. 4. (a) $P_{max}/P_{max,0}$ of modules fabricated from the cell with the standard emitter and from the cell with surface-etched emitter as a function of PID-stress duration, both with the single-layered 80-nm-thick SiN_x with an RI of 2.0. The data points show the mean values for the three modules, and the error bar corresponds to the standard deviation of the mean. The solid and broken lines are guides to the eye. (b) ECV active dopant profiles of the cells.

Fig. 5. $P_{max}/P_{max,0}$ of modules fabricated from the standard cell, cell with the SiN_x with the distorted interface, and the cell both with SiN_x with the distorted interface and the surface-etched emitter. All the cells have the single-layered 80-nm-thick SiN_x with an RI of 2.0. The data points show the mean values for the three modules, and the error bar corresponds to the standard deviation of the mean. The solid, broken, and chain lines are guides to the eye.

Fig. 6. $P_{max}/P_{max,0}$ of modules fabricated from the n-type front-emitter c-Si cells with the single-layered SiN_x films with RIs of 2.03, 2.20, and 2.34 before and after PID tests. All the cells have thermally grown ~10 nm SiO_2 layers between the SiN_x layers and the emitters. The solid, broken, and chain lines are guides to the eye.

Table I. Structure and properties of solar cells used in this study. All the solar cells have a thin SiO_2 layer between the emitter and the SiN_x by the NAOS process step. Note that all the data were obtained from the full-area cells before cutting.

Emitter	Additional nitridation	SiN_x	J_{sc} (mA/cm^2)	V_{oc} (mV)	Fill Factor	Efficiency (%)
Std.[*1]	No	Std.[*2]	37.1	630	77.9	18.5
Std.[*1]	No	RI = 2.0/2.4	37.7	647	79.8	19.8
Surface-etched	No	Std.[*2]	38.1	646	79.0	19.8
Std.[*1]	Yes	Std.[*2]	38.1	643	78.8	19.6
Surface-etched	Yes	Std.[*2]	38.2	650	79.0	20.0

[*1] Std. emitter: Emitter with surface depleted layer

[*2] Std. SiN_x: 80-nm single layered SiN_x

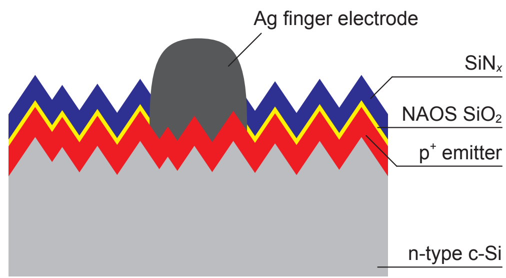

Fig. 1

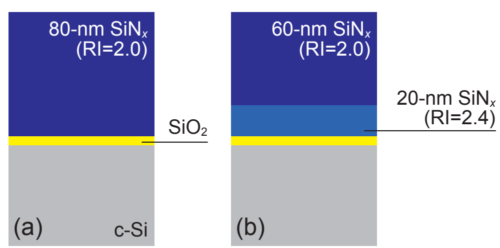

Fig. 2

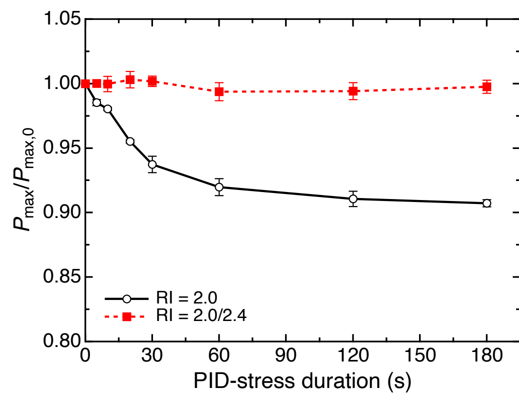

Fig. 3

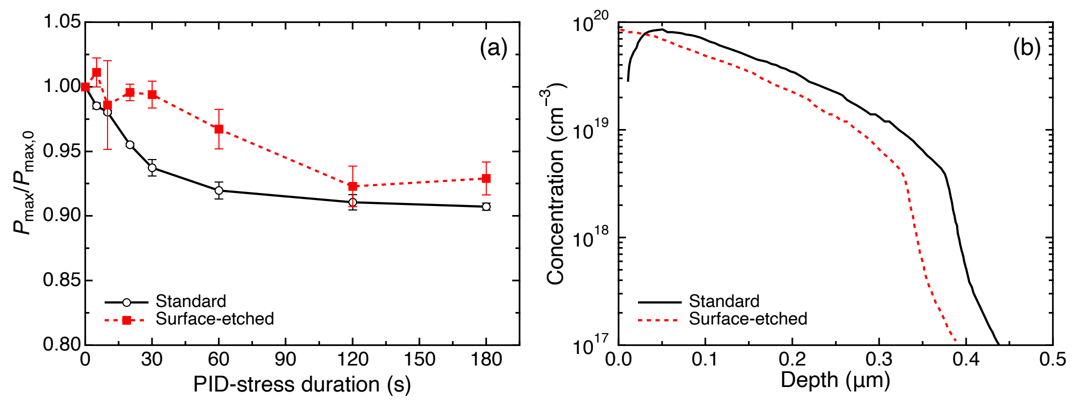

Fig. 4

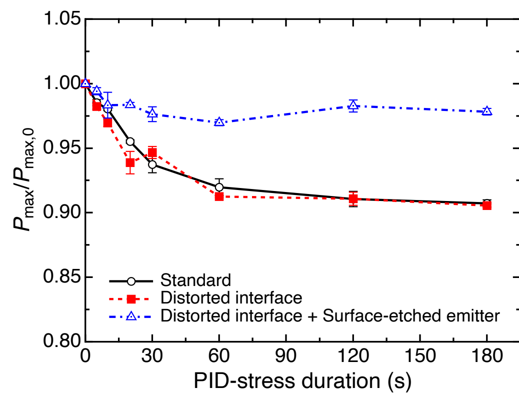

Fig. 5

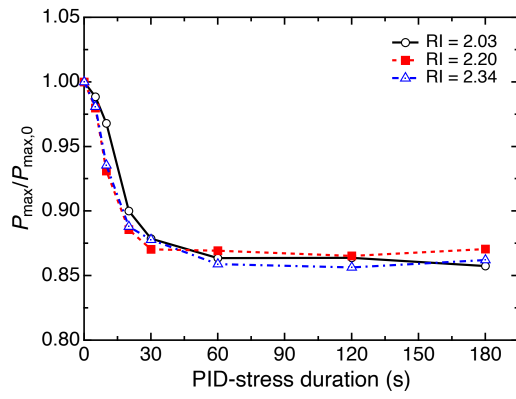

Fig. 6