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Description	

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Delay of the potential-induced degradation of n-type crystalline silicon photovoltaic modules by the prior application of reverse bias

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We investigated the influence of the pre-application of reverse bias on the potential-induced degradation (PID) of n-type front-emitter (n-FE) crystalline Si (c-Si) photovoltaic modules. Applying a prior positive reverse bias to n-FE cells delays charge-accumulation-type PID (PID-1), decreases in short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}). The prior positive bias accumulation may accumulate negative charges in the SiN_x, which leads to an increase in a duration for the positive charge accumulation by the PID test applying a negative bias. We also found that sufficiently long prior positive bias application results in the delay of PID-2, a fill factor (FF) reduction by the incursion of Na ions into the depletion region of the p–n junction of n-FE cells.

Keywords: n-type front-emitter crystalline silicon solar cell, potential-induced degradation, Photovoltaic module

1. Introduction

In recent years, global warming and energy resource depletion issues have become increasingly serious. It is thus necessary to use energy sources such as solar power to replace fossil fuels. Photovoltaic (PV) power generation is one of the simple and effective ways to use solar energy, and the installation of PV modules is ongoing at present all over the world. The long-term reliability of the PV modules is particularly important for their stable operation.

Potential-induced degradation (PID), output losses in PV modules caused by a potential difference between cells and a grounded frame,[1–3] is one of the most serious issues of the long-term reliability of PV modules, particularly in large-scale PV power plants. The PID of PV modules with cells using a p-type c-Si base has been investigated in detail.[1–9] It occurs when the cells are put in a negative potential and is caused by a decrease in shunt resistance and resulting reduction in fill factor (FF). The shunting occurs by stacking faults decorated with Na penetrating the front n^+ emitters.[8,9] n-type c-Si solar cells, in general, have better performance than the p-type cells and better stability against light-induced degradation, and they are thus expected to increase the market share in the near future. In order to guarantee the long-term reliability of n-type c-Si PV modules, it is essential to investigate their degradation. There are, however, relatively smaller number of studies on the PID of n-type c-Si PV mocules.[10–21]

We have previously reported that the PID of n-type front-emitter (n-FE) c-Si PV modules occurs in three stages under negative bias.[22] The first-stage PID (PID-1) of n-FE c-Si PV modules is caused by positive charge accumulation in the anti-reflection silicon nitride (SiN_x).[13] Si dangling bonds back-bonded to three N atoms (K centers) lose electrons by an electric field, resulting in positive fixed charges remained in SiN_x.[20] The PID-1 is characterized by reductions in J_{sc} and V_{oc} and occurs within a few minutes in our indoor PID test. The second-stage PID (PID-2) and the third-stage PID (PID-3) are caused by Na introduction into the cells.[22] PID-2 is characterized by a reduction in FF alone, which occurs after a few hours in the indoor test. PID-2 is caused by Na incursion into the depletion region of the p–n junction of n-FE cells. Na creates a large number of defect levels in the depletion region and a recombination current is increased. PID-3 is characterized by decreases in V_{oc} and FF after a few days in the indoor test, which results from the formation of Na-based domes destroying the surface SiN_x and p^+–n junction.[23]

The PID of c-Si PV modules can be affected by the prior reverse bias application. The PID of conventional p-type c-Si PV modules under negative bias stress is delayed by the

prior positive bias application.[24] Similar phenomena may be observed in the n-FE c-Si PV modules, which can be measures for the mitigation or delay of their PID in the field. In this study, we investigated the effects of prior reverse bias application on the multi-stage PID of n-FE c-Si PV modules.

2. Experimental methods

We used commercial 156×156 mm^2 n-FE c-Si PV cells which have anti-reflection and passivation films consisting of SiN_x and Si dioxide (SiO_2) films. The cells were cut to pieces with a size of 20×20 mm^2 for the fabrication of one-cell mini modules. The lamination process for the module fabrication was conducted using a module laminator (LM-50X50-S, NPC) with the following two steps: heating at 150 °C in vacuum for 5 min for degassing and heating at 150 °C under atmospheric pressure for adhesion. The fabricated n-FE c-Si PV modules consisted of 45×45 mm^2 conventional tempered cover glass/ethylene-vinyl acetate copolymer (EVA)/cell/EVA/backsheet. The backsheet consisted of polyvinyl fluoride (PVF)/polyethylene terephthalate (PET)/PVF.

The PID test was conducted in the dark at 85 °C under no intentional humidity stress (<2%RH). A bias voltage of −1 kV was applied between the cells and the grounded Al plate fully covering the cover glass of the PV modules.[25] The reverse bias application was performed in the same environmental setup by applying a voltage of +1 kV to the n-FE cell prior to the PID test. The bias voltages were applied by using an insulation tester (TOS7210S, KIKUSUI).

We evaluated the performance of the n-FE c-Si PV modules by measuring current-density–voltage (*J–V*) characteristics under 1-sun light illumination and external quantum efficiency (EQE) spectra at 25 °C using a measurement system (CEP-25, Bunkoukeiki).

3. Results and discussion

3.1 Effect of short-duration prior reverse bias application

Figure 1 shows the *J–V* characteristics of n-FE c-Si PV modules with and without prior reverse bias application for 3 min before and after the PID test for 5 min. One can see reductions in J_{sc} and V_{oc} for the modules after the PID test, which are typical behavior of PID-1, acceleration of carrier recombination on the p^+ emitter surface induced by positive charges accumulated in SiN_x.[13–14, 20] Note that the reductions in J_{sc} and V_{oc} are smaller in the modules receiving positive bias application prior to the PID test.

Figure 2 shows the J_{sc}, V_{oc}, FF, and P_{max}, normalized by their initial values, of n-FE c-Si

PV modules with and without prior reverse bias application as a function of PID-stress duration. The PID stress causes the simultaneous J_{sc} and V_{oc} reductions both in the modules with and without prior reverse bias application, while no FF reduction occurs in this PID-stress duration range. These are clear indications of PID-1.[14,20)] We can see that PID-1 is delayed in the modules receiving the prior reverse bias application, and longer reverse bias application tends to result in more delay of PID-1. The delay of J_{sc} by prior positive bias application is seen more clearly in the EQE spectra of the modules, as shown in Fig. 3. The modules receiving 5-min PID stress have smaller EQE in the short wavelength region than that the reference module without PID stress. The smaller EQE in the short wavelength region is due to more recombination on the p^+ emitter surface induced by positive charges accumulated in SiN_x.[14,21)] We can also see that longer reverse bias application tends to have larger EQE in the short wavelength region, indicating the delay of PID-1 by the prior positive bias application.

The mechanism of the delay of PID-1 by the prior reverse bias application is schematically explained in Fig. 4. We have previously proposed that the origin of the charges in SiN_x is K centers.[14,20,26)] K centers are Si dangling bonds back-bonded to three N atoms in SiN_x and can be negatively-charged (K^-), neutral (K^0), and positively-charged (K^+) by extracting or adding electrons.[27–29)] By the PID stress, i.e. negative bias application to the n-FE cell, electrons are extracted from the K centers in SiN_x, resulting in the formation of K^+ centers. The K^+ centers attract minority carriers, electrons, in the p^+ emitter and induce more active surface recombination, leading to simultaneous reductions in J_{sc} and V_{oc}. When the positive bias is applied prior to the PID stress, electrons are introduced into the SiN_x and are captured at the K centers, resulting in the formation of K^- centers. By the successive negative bias application to the cell, these K^- centers lose electrons and become K^+ centers in the end. However, more electrons have to be extracted from the SiN_x received prior positive bias application to transform all the K centers to be K^+ centers, compared to the case of SiN_x without positive bias application. This can explain the delay of the PID-1 of n-FE c-Si PV modules by the application of prior positive bias. We have previously reported that the PID-1 of n-FE c-Si PV modules can be recovered by the post positive bias application.[20)] This supports the possibility of electron supply to the SiN_x and resulting formation of K^- centers by the positive bias application.

3.2 Effect of long-duration prior reverse bias application

Figures 5 shows the J_{sc}, V_{oc}, FF, and P_{max} of n-FE c-Si PV modules with and without 20-h prior reverse bias application as a function of PID-stress duration. After the PID tests, the J_{sc} and the V_{oc} of the modules without reverse bias application start to decrease within 10 s and are saturated within approximately 180 s. As in the case of the short-duration prior reverse bias application, reductions in J_{sc} and V_{oc} are effectively delayed by the prior positive bias application. Note that the saturated J_{sc} and V_{oc} values are identical independent of the presence or absence of the prior reverse bias application. This is reasonable since the saturation of PID-1 corresponds to the situation in which all the K centers are converted to K^+ centers, and sufficiently long PID stress eventually extract all the electrons from the K^- and K^0 centers even if the cells receive prior positive bias application. This indicates that the prior positive bias application cannot be measures for the complete suppression of PID-1. Another important point is that the delay of PID-1 is a few minutes, which is much smaller than the duration for the reverse bias application (20 h). This can also be explained by the K center model. All the K centers may be fully converted to K^- centers if the positive bias application is long to some extent, and further long positive bias application do not increase K^- centers any more.

By further long PID stress, FF starts to decrease within 3 h and is then saturated within ~70 h for the modules without prior positive bias application. This represents a common characteristic of PID-2, where Na infiltrates the depletion region of the p^+–n junction, leading to an elevated recombination current. In the modules with prior 20-h positive bias application, the reduction in FF is delayed and mitigated. This clearly demonstrates that the prior positive bias application for n-FE c-Si PV modules is effective for the delay of PID-2 as well as for the delay of PID-1. Note that FF of the modules without prior positive bias application inversely increases after the PID stress for >20 h. Similar phenomenon can also be seen in our previous study.[22] This may be an indication of the onset of PID-3, the formation of Na-based domes.[23] We speculate that Na ions in the depletion region of the p^+–n junction are drawn out to the surface Na domes through the stacking faults and FF temporarily increases.

Figure 6 shows the schematic explanation of the delay of PID-2 by the prior positive bias application. We have recently reported that Na ions existing near the cell surface in EVA encapsulant invade into the cell and induce PID-2 under an electric field created by a negative bias, as shown in Fig. 6(a).[30] Prior positive bias application may drift the Na ions away from the cell surface, and the number of Na ions in the vicinity of the cell is reduced, as shown in Fig. 6(b). In the successive PID test, i.e., negative bias application, more duration

is required for the drift of Na ions to reach the cell surface, and PID-2 can be delayed.

Finally, we discuss the practical use of the reverse bias application. It is known that the post reverse bias application is effective for the recovery of PID-1 and PID-2.[20,22] However, the reverse bias application to the modules after the installation in the field are quite troublesome. On the contrary, the application of positive reverse bias just after the fabrication of n-FE c-Si PV modules may be more realistic. Although the complete suppression of PID-1 and PID-2 of n-FE c-Si PV modules cannot be realized by the prior reverse bias application, it will certainly delay the two types of PIDs and thus increase their total power generation amounts.

4. Conclusions

In this study, we investigated the delay effect of the short and long-duration prior reverse bias application for the PID of n-FE c-Si PV modules. We demonstrated that the prior reverse bias application leads to the delay of PID-1, charge accumulation in SiN_x, and PID-2, Na incursion into the depletion region of the p^+–n junction. The delay of PID-1 can be well explained by the prior formation of K^- centers and resulting increase in the duration for their conversion to K^+ centers. PID-2 may be delayed by drifting away of Na ions existing near the cell surface in EVA encapsulant. The reverse bias application can be used for the delay of PIDs in the commercial n-FE c-Si PV modules and contributes to an increase in their total power generation amount.

Acknowledgments

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Figure Captions

Fig. 1. *J–V* characteristics of n-FE c-Si PV modules with and without prior reverse bias application for 3 min before and after the PID test for 5 min.

Fig. 2. J_{sc}, V_{oc}, FF, and P_{max} of n-FE PV modules normalized by their initial values as a function of PID-stress duration. Each data point shows the mean value for two modules, and each error bar corresponds to the standard deviation of the mean.

Fig. 3. EQE spectra of n-FE c-Si PV modules with and without prior reverse bias application before and after the PID test for 5 min.

Fig. 4. Schematics of the delay of PID-1 by prior positive reverse bias application.

Fig. 5. J_{sc}, V_{oc}, FF and P_{max} of n-FE c-Si PV modules with and without prior reverse bias application for 20 h as a function of PID-stress duration.

Fig. 6. Schematics of the delay of PID-2 by prior positive reverse bias application: (a) PID-2 under negative bias and (b) Na drift by the positive bias application.

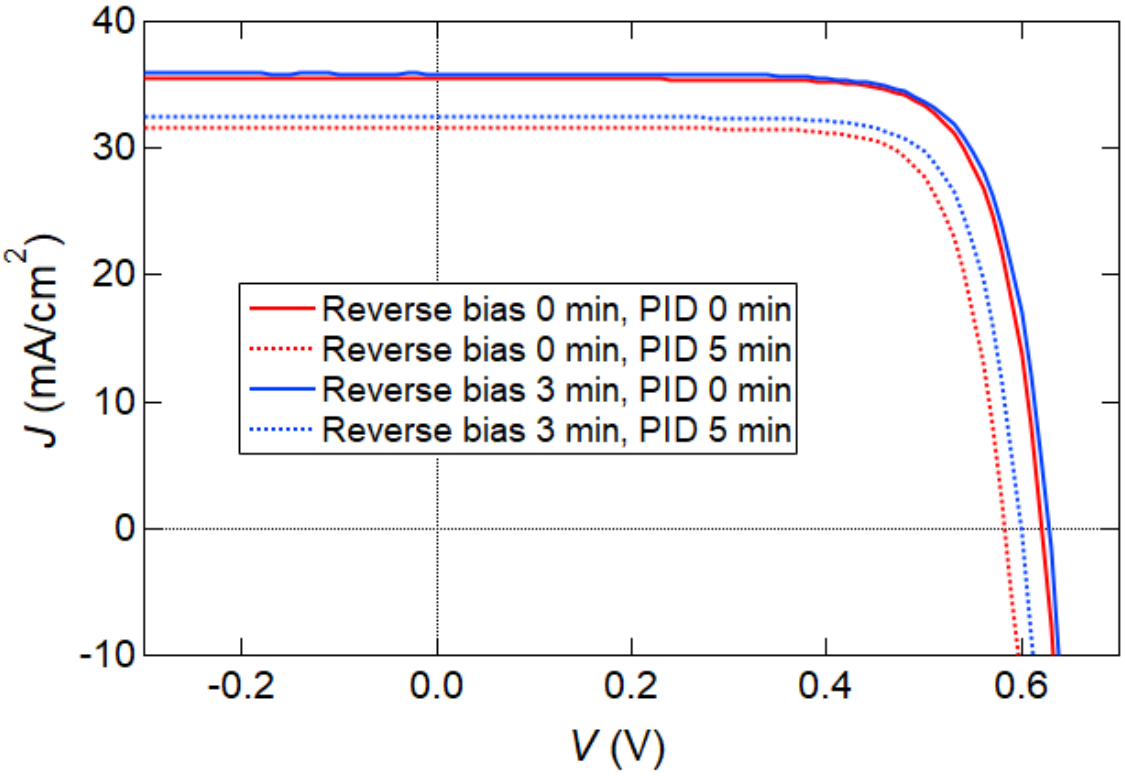
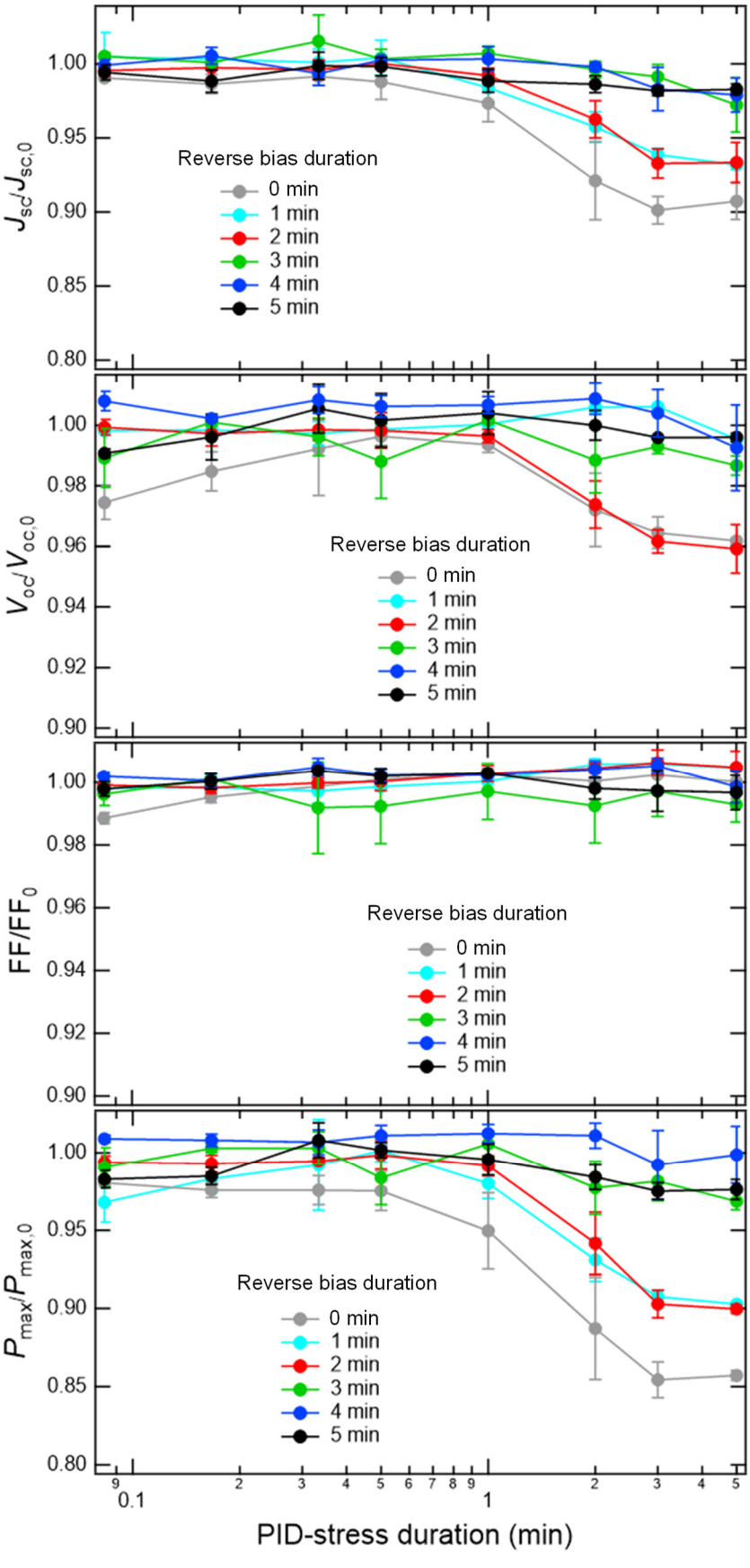

40
30
20
10
0
-10
-0.2
0.0
0.2
0.4
0.6
J (mA/cm2)
V (V)
Reverse bias 0 min, PID 0 min
Reverse bias 0 min, PID 5 min
Reverse bias 3 min, PID 0 min
Reverse bias 3 min, PID 5 min

Fig. 1.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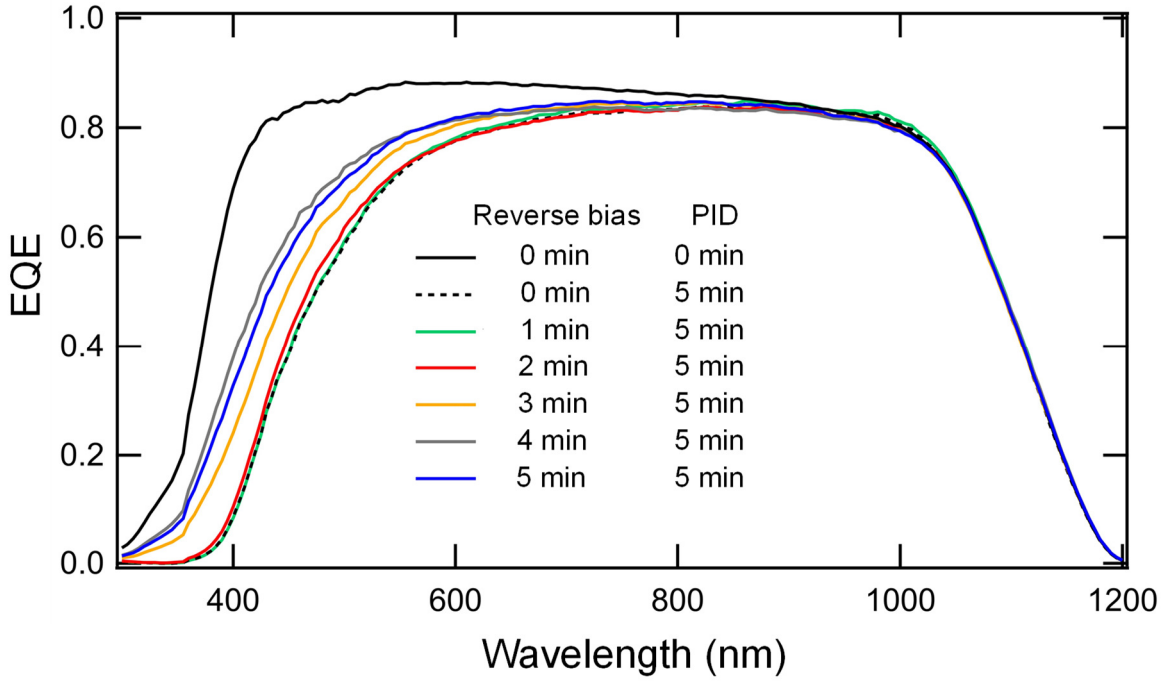
$V_{oc}/V_{oc,0}$
FF/FF$_0$
$P_{max}/P_{max,0}$
Reverse bias duration
0 min
1 min
2 min
3 min
4 min
5 min
PID-stress duration (min)

Fig. 2.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0.8
0.6
0.4
0.2
0.0
EQE
400
600
800
1000
1200
Wavelength (nm)
Reverse bias
PID
0 min
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5 min
5 min

Fig. 3.

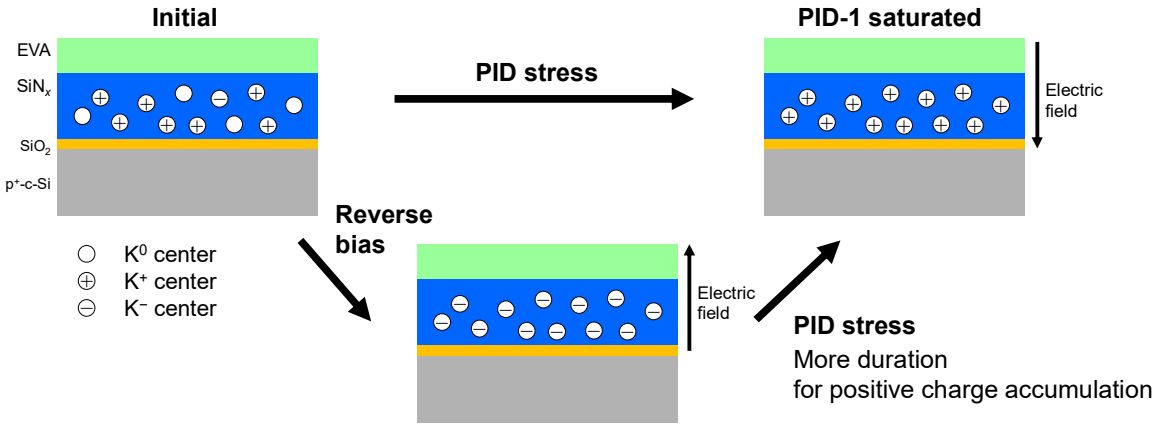
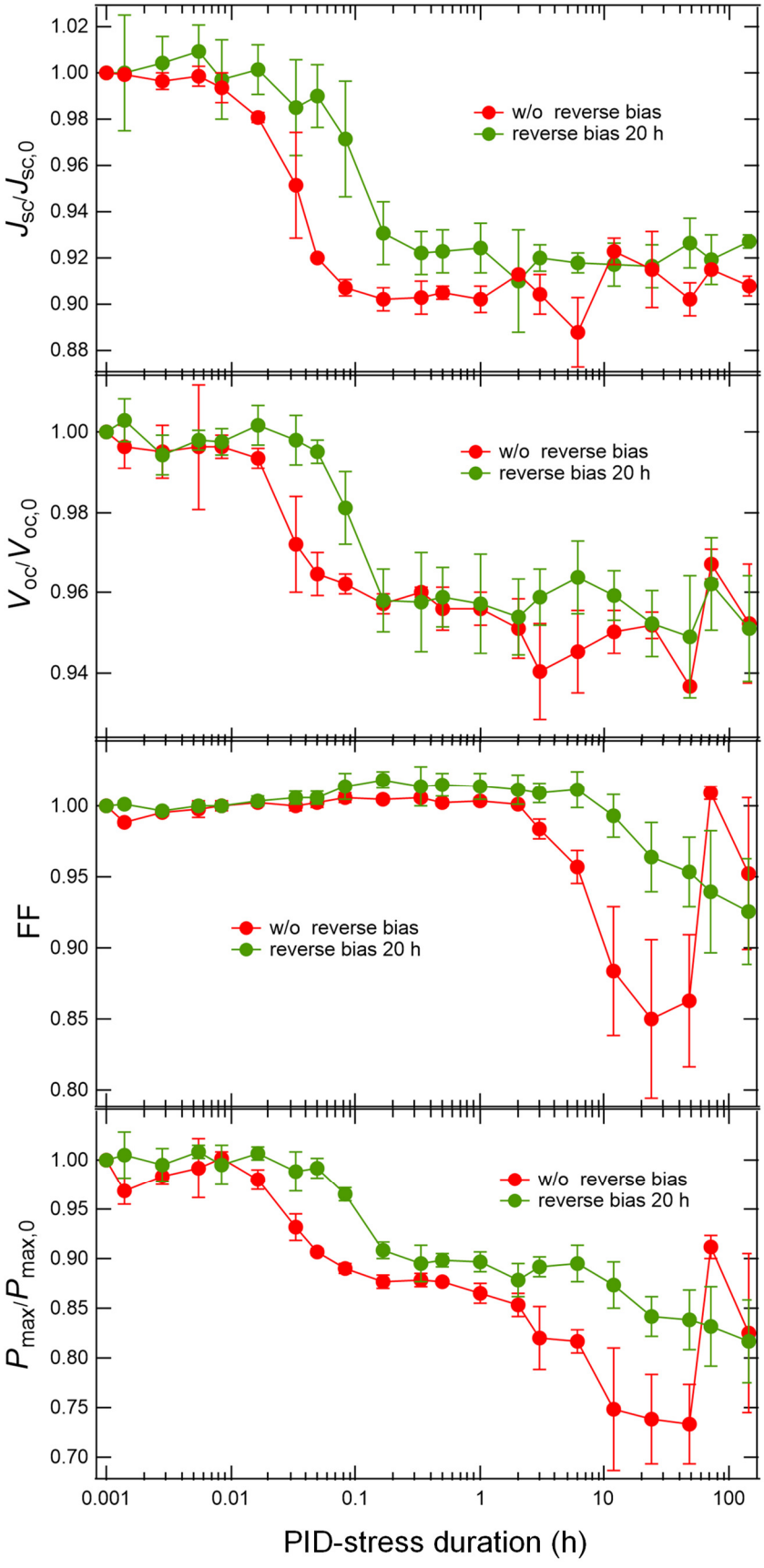

Initial
EVA
SiNx
SiO2
p+-c-Si
K0 center
K+ center
K− center
PID stress
PID-1 saturated
Electric field
Reverse bias
Electric field
PID stress
More duration
for positive charge accumulation

Fig. 4.


$J_{sc}/J_{sc,0}$
$V_{oc}/V_{oc,0}$
FF
$P_{max}/P_{max,0}$
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reverse bias 20 h
PID-stress duration (h)
0.001
0.01
0.1
1
10
100

Fig. 5.

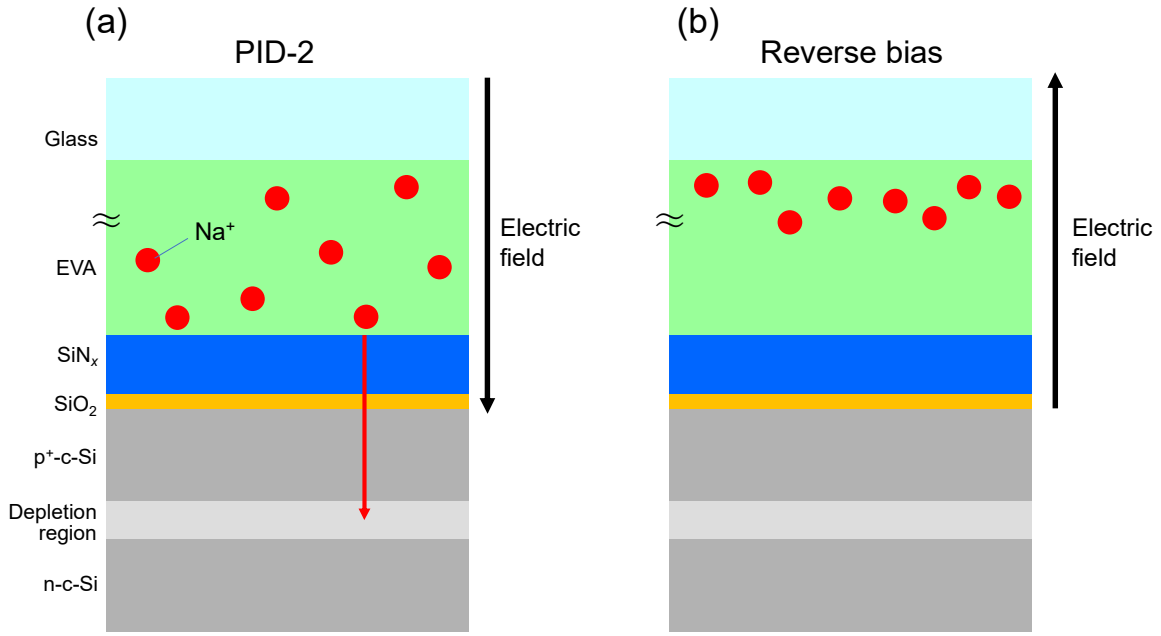
(a)
PID-2
Glass
EVA
Na+
SiNx
SiO2
p+-c-Si
Depletion region
n-c-Si
Electric field
(b)
Reverse bias
Electric field

Fig. 6.