Research on power consumption reduction that uses data compression

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February 9, 2006

Keywords: Cache memory, Power consumption, Data compression.

1 Introduction

Recently, power dissipation of microprocessor has increased. The power dissipation influences a battery drive type mobile device and the lekage current cannot be disregarded by making of process rule minute. So, static power comsuption has increased. On the one hand, software is a large-scale and complexity, so, speed-up and the energy-saving of processor are requested. The processor and main memory are speed-up, but the speed difference between processor and main memory increases every year. To cover the speed difference between the processoe and the main memory, the cache memory has been increased. The cache memory has the majority of the area of the processor, and it is reported that power consumption reaches 50% of the processor.Recently the power consumption reduction technique of the cache memory is researched.

In this paper, the cache memory that greatly occupies the power consumption of the processor is paid to attention. we propose the cache memory architecture that achieves low power consupmtion. Power consumption is reduced by doing data compression and the voltage control.

2 Power consuption reduction method of processor

The attention of the power consumption of the processor is growing. The processor that adopts the power consumption reduction technology appears in the last few years. It introduces the technology adopted with a business processor. Moreover, the research on the power consumption reduction in the cache memory that has the majority of the processor has been increased. Here, the research of the power consumption reduction in cash concerning this research is described.

3 Power consuption reduction method

The L1 data cache, the instruction cache and L2 cache memory are assumed to be on a chip. We propose a memory hierarchy consisting of uncompressed L1 instruction, data caches, main memory and compressed L2 unified cache. Compression does every the cache block, if the cache block stored in the L2 cahce memory is compressed into 1/2 or less by compressor, the cache block is stored in the compressed block. And the voltage of the cache memory is controlled by the unit of 1/2 of the cache block where the compression data was stored, and the power consumption of the cache memory os reduced. When cache block is stored form L2 cache memory to L1 cache meomry and main memory, if the cache block is compressed, the data is decompressed by decompressor, and if the data is uncompressed, another path is passed for the overhead reduction.

4 Compression and Decompression

Compression algorithm uses FPC(Frequent Pattern Compression). Data is compressed every the cache block. Each cache line is divide into 32-bit words(e.g., 16 words for a 64-byte line). Each 32-bit word is encoded based on the decided pattern. There are 8 kinds of compression patterns. Each pattern is shown as information in 3-bits. Each 32-bit word is encode as a 3-bits information plus data in 32-bit word.

When the compression data is decompression, 3-bits infomation is used.

5 Power reduction method

Gated-Vdd is used for the voltage control of cache memory, the coltage control of cache block is the unit of 1/2 of the cache block. Gated-Vdd is arole of the swith that controls the voltage of the cache block. The power consumption of the cache memory os decreased by switching Gated-Vdd. Compression bit is in L2 cache memory tag. Compression bit is the compression of the cache block.

Setup Time is generated for the voltage control of cache block.Setup Time might influence the execution cycle and . Write buffer is used to decrease the influence of Setup Time.

6 estimation

The propsal method is evaluated by the simulation. We assumed that the number of entries of Write buffer is 16, 32, 64, Setup time is 500, 1000, 5000, 10000, and 50000. The execution time and L2 leakage energy is measred by the simulation. The reduction rate of the compressibility and the power consumption of the L2 cache almost became the same as a result of the simulation. When Setup Time becomes 10000 cycle or more when Write buffer is 16 entries, a big influence is exerted on the performance and power consumption. The influence of Setup Time was able to be decreased by making it to 32 and 64 entry.

7 Summary

In this thesis, it proposed the technique for doing the energy-saving of the cache memory by paying attention to the cache memory that had the majority of the processor, and using data compression and the electric power control. Write buffer was able to reduce power consumption equal with the compressibility of cash with 32entry by using the proposal method because of the minimum.