High throuput Wave Pipelined DSP

Kouhei Uyama (410018)

School of Information Science,
Japan Advanced Institute of Science and Technology

February 14, 2006

Keywords: Wave pipeline, Systolic array, MAC, Wiring delay.

1 Introduction

Recently, application areas of DSP (Digital Signal Processor) have been growing. Signal processing in multimedia devices requires high throughput and demands the next generation DSP. The DSP is featured in product-sum operation executed by a multiplier and an accumulator.

Commercial DSPs have adopted synchronous pipeline architecture. However, the ratio of wiring delay in propagation delay of LSIs is increasing in today's fine fabrication process technology. As a result, synchronous pipeline architecture can not exploit effect of device scaling and cannot achieve performance improvement.

Signal processing use product-sum operations. The objective of this paper is to propose a design methodology of high throughput MAC (a multiplier and an accumulator).

The systolic array and the wave pipelined architecture are applied for this purpose [1]. Precise delay evaluation including wiring delay is conducted by circuit simulator, HSpice.

2 Wave pipelined architecture

The clock cycle time of the wave pipelined architecture is decided by difference between the maximum and the minimum delay time. The clock cycle time is shortened by balancing delay variation. The delay balancing method prolongs the minimum delay time by inserting delay-buffers in the

minimum delay pass.

There are, however, difficulties to design perfect delay balanced circuits. Therefore, precise delay analysis and a new delay balancing approach are necessary.

3 Composition of MAC

It is desiable that the mothod to adopt the wave pipeline architecture is easy. The MAC is composed with simple circuits, array of full adders. It is easy to accomplish balancing delayes of a full adder.

This chapter proposes a novel MAC architcture configured with systolic array [2]. The delay of carry propagation impedes multiple bit addition and increase latency of obtaining a calculation result.

Pipelined operation of ripple carry adders configured with systolic array hides delayies of carry propagation. Input data are shifted in the partail product generator through shift registers, the products are moved into ripple carry adders configured with systolic array.

This configuration achieves high throughput, but the additional area for the shift registers is required.

4 Delay simulation by HSpice

In this chapter, the delay simulation of an FA (full adder) and a DFF (D type flip-flop) for a latches of sytolic array is conducted.

Precise delay time analysis for FA and operation timing analysis for DFF are examined. The delay balance is done by inserting delay-buffers. The distributed constant wiring model is simulated a RC lumped-constant circuit.

The outline of this chapter is shown in the following.

1)MOSFET design of 90n process rule [3]

2)Design of FA with delay balance and latch (DFF)

3)Layout of FA and latch (DFF) [4]

4)Decision of wiring model

5)Delay simulation including wiring delay

5 Conclusion

The FA of the wave pipeline architecture can be operated by clock fre-

quency 5GHz. This is 2.4 times faster than synchronous pipeline architecture. The systolic array MAC is all composed by the FA. The FA is a unit of the processing element. Therefore, the MAC can't be operated faster than the FA. The accumulator of MAC has feedback. It is necessary to match the timing of the latch in the back and forth to use the multiphase clock. Timing is matched by using Delay. Proposed MAC operates by clock frequency 5GHz.

References

[1] Hibino Yasusi. Multithread type super-pipeline processor architecture. H10∼12.Science research cost result report B210480058,2002.

[2] JOHN McCANNY.Systolic Array Processors.PRENTICE HALL,1989.

[3] BSIM3 Homepage,http://www-device.eecs.berkeley.edu/∼bsim3/.

[4] Neil H.E.Weste and Kamran Eshraghian. Principles of CMOS VLSI Design.MARUZEN,1988.