Doctoral Dissertation

Vertical spintronic device application of MnAs/InAs/MnAs double heterostructure on GaAs (111) B by molecular beam epitaxy (MBE)

Md Tauhidul Islam

Supervisor: Masashi Akabori

Graduate School of Advanced Science and Technology

Japan Advanced Institute of Science and Technology

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Abstract

Spintronics, or spin transport electronics, represents a rapidly evolving field that utilizes the intrinsic spin of electrons, alongside their charge, to develop innovative technologies for data storage, sensing, and computation. Semiconductor spintronics combines the benefits of semiconductors, such as bandgap tunability and carrier modulation, with spin-dependent phenomena, enabling novel devices with enhanced functionality. A key concept in spintronics is the spin field-effect transistor (spin-FET), which uses a gate voltage to modulate spin-polarized currents, offering the potential for low-power, high-speed computing. Spin valves, on the other hand, rely on the relative alignment of magnetizations in ferromagnetic layers to control resistance, forming the foundation of many spintronic devices.

This work explores the growth, characterization, and application of MnAs/InAs/MnAs double heterostructures in vertical spin valve (VSV) devices, combining ferromagnetic MnAs layers with a thick low-temperature-grown InAs (LT-InAs) channel. These heterostructures, grown using molecular beam epitaxy (MBE) on GaAs (111) B substrates, represent a significant step forward in hybrid semiconductor/ferromagnetic spintronic systems. The use of LT-InAs offers advantages in growth combination with MnAs at same temperature but presents challenges in defect management and interface quality.

The growth of LT-InAs was optimized by varying parameters such as the V/III beam equivalent pressure ratio and growth temperature. Optimized growth conditions yielded samples with minimal surface roughness, high carrier concentration, and n-type conduction, as confirmed by Hall measurements. Structural characterization using X-ray diffraction (XRD) revealed lattice expansion in LT-InAs, attributed to strain relaxation mechanisms. Atomic force microscopy (AFM) and scanning electron microscopy (SEM)

showed defect-minimized, uniform surfaces, critical for achieving good-quality interfaces with MnAs layers.

The MnAs/InAs/MnAs heterostructures demonstrated well-defined interfaces, as verified by cross-sectional SEM and energy dispersive X-ray spectroscopy (EDS). Magnetization measurements revealed distinct coercive fields for the top and bottom MnAs layers, enabling spin-dependent transport in the double heterostructure. Vertical spin valve devices were fabricated using advanced lithography and etching techniques, achieving precise device geometries for current-perpendicular-to-plane (CPP) measurements. Spin valve measurements were performed using AC lock-in method and showed clear resistance changes corresponding to the parallel and antiparallel alignment of the MnAs layers. We achieved a highest of ~1.2% spin injection efficiency at 240 K measurement temperature.

This work marks the first successful demonstration of a vertical spin valve device using MnAs/thick-InAs/MnAs heterostructures, paving the way for further advancements in semiconductor spintronics. The findings highlight the challenges of impedance mismatch and interface quality but also emphasize the potential of this hybrid material system for efficient spin transport and injection. Future directions include improving LT-InAs growth using advanced techniques like migration-enhanced epitaxy (MEE), reducing impedance mismatch through conductive alloys, and exploring novel device architectures such as gate-all-around spin field-effect transistors (spin-FETs). These advancements will contribute to the realization of high-performance spintronic devices for next-generation technologies.

Keywords: Semiconductor spintronics, vertical spin valve, MnAs/InAs/MnAs double heterostructure, molecular beam epitaxy, low-temperature InAs.

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Contents

List of figures

List of tables

Chapter 1: Introduction

1.1 Spintronics

Spintronics, also known as spin transport electronics, introduces a transformative approach by utilizing both the charge and spin of electrons in devices. Unlike traditional electronic devices such as transistors and integrated circuits, which depend solely on the flow of charge carriers (electrons or holes) and disregard electron spin, spintronic devices exploit the variation in transport between “spin-up” and “spin-down” electrons. The concept of spintronics gained momentum after the 1988 discovery of giant magnetoresistance (GMR), paving the way for numerous technological advancements and creating a wealth of career opportunities for engineers and scientists. Today, GMR-based sensors have become integral to hard drives, robotics, electric vehicles, magnetic random-access memory (MRAM), industrial motors, magnetic sensing, and navigation technologies [1-4].

1.1.1 Overview

Conventional information processing and communication devices achieve functionality by controlling the flow of electric charges through integrated circuits, typically constructed from nonmagnetic semiconductor materials. In these semiconductors, electron spin – a fundamental property of electrons representing intrinsic angular momentum – is disregarded, with devices focusing exclusively on charge transport. As a result, the information encoded in the electron’s spin state goes unused, limiting these circuits to binary charge manipulation.

Spintronic devices, however, capitalize on the spin of electrons, introducing a new

dimension for encoding and manipulating information. By utilizing the spin degree of freedom, spintronic devices can simultaneously generate and control charge currents and interconvert electrical and magnetic signals within the same device. This expanded functionality provides a versatile platform capable of seamlessly integrating processing, storage, sensing, and logic on a single chip. Such integration could redefine conventional circuit design by enabling devices that not only store information but also process it directly, significantly enhancing the efficiency and multifunctionality of electronic systems.

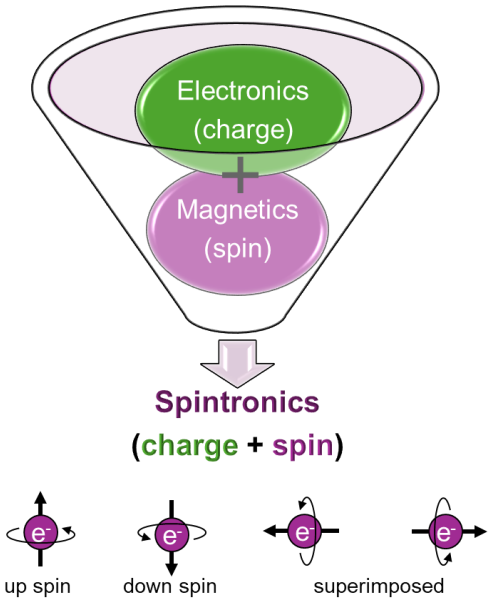

Figure 1.1 Spintronics combines electron charge and spin for advanced functionality.

Furthermore, spintronics offers substantial benefits for overcoming limitations in traditional semiconductor-based electronics. The inherent properties of spintronic materials allow for increased scalability, reduced power consumption, and improved data processing speeds. As device dimensions continue to shrink and energy efficiency becomes paramount, the advantages of spintronic technology are increasingly relevant, making it a powerful complement and potential alternative to conventional semiconductor

devices. The seamless integration of magnetic and electronic properties within a unified platform is expected to drive innovation in future computing, enabling faster, more compact, and energy-efficient circuits.[5]

In the electronics industry, Moore's law predicts a doubling of transistor density on chips annually, but further miniaturization is limited by stability issues and hard disc constraints. Spintronics, a field focusing on the spin rather than the charge of carriers, offers a path forward with devices like spin FETs, spin LEDs, and spin photodiodes, which promise high speed, non-volatility, high density, and low power consumption. Key breakthroughs include the discovery of giant magnetoresistance (GMR), tunnel magnetoresistance (TMR), and the spin transistor proposed by Datta and Das [6]. However, efficient spin injection into semiconductors remains a major challenge.

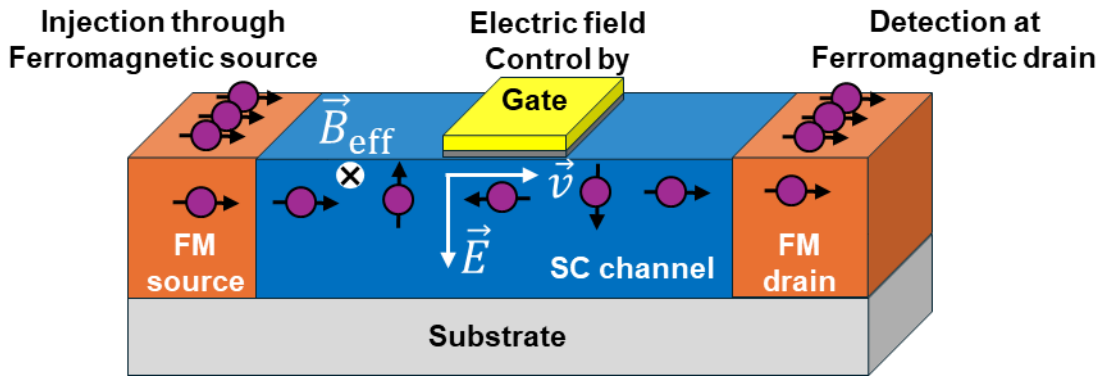

Figure 1.2 Simple illustration of Datta-Das type spin-FET. Here $\vec{B}_{\text{eff}}$, $\vec{E}$, and $\vec{v}$ are effective magnetic field felt by the carriers, electric field and velocity of carriers respectively.

The electron's spin represents a fundamental form of angular momentum that exists independently from the angular momentum associated with its orbital movement. The projection of the electron's spin along an arbitrary axis is quantified as 1/2 $\hbar$, indicating

that the electron behaves as a fermion in accordance with the spin-statistics theorem. Similar to orbital angular momentum, spin possesses a corresponding magnetic moment, with its magnitude represented as,

$$\mu = \frac{\sqrt{3}}{2}\frac{q}{m_e}\hbar \quad (1a)$$

The collective behavior of electron spins in a solid can significantly influence the material's magnetic and electronic characteristics, such as imparting a permanent magnetic moment, as observed in ferromagnetic materials.

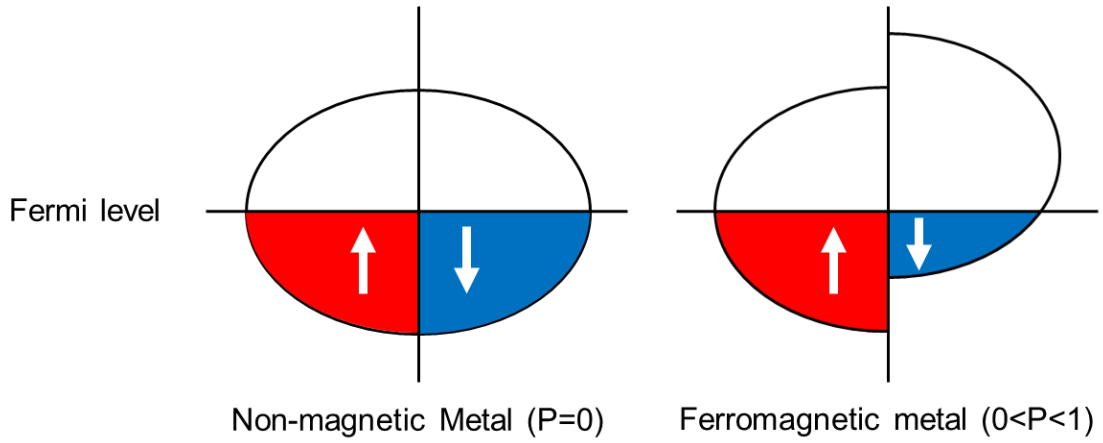

Figure 1.3 Simplified band structure diagram of non-magnetic and ferromagnetic metal. For non-magnetic metal, the conduction bands are the same for spin-up and spin-down electrons. Hence the current passing through has no spin polarization at zero field, i.e. $P = 0$. In ferromagnetic materials the spin-up and spin-down are split due to Coulomb interaction, hence depending on the material the current emerging from it will have some degree spin polarized, i.e. $0 < P < 1$.

In several materials, electron spins are evenly distributed between up and down states, yielding transport properties that are independent of spin. For spintronic devices, however, it's essential to create or manipulate a spin-polarized population of electrons, which results in an imbalance between spin-up and spin-down electrons. The polarization of any

spin-dependent property P can be defined as,

$$P = \frac{D_\uparrow - D_\downarrow}{D_\uparrow + D_\downarrow} \quad (1b)$$

Here, D is the spin density, then $D_\uparrow$ and $D_\downarrow$ represent the number of spin-up and spin-down carriers per unit volume, respectively. Spin polarization can be established by introducing an energy difference between spin-up and spin-down states. This can be achieved through several methods: applying a strong magnetic field (Zeeman effect), utilizing the exchange energy in ferromagnetic materials, or pushing the system into a non-equilibrium state. The timespan over which this non-equilibrium spin population is maintained is referred to as the spin lifetime, τ.

While metal-based spintronics has seen significant advancements, semiconductors provide unique benefits, such as gate-controlled modulation of spin currents and compatibility with optical techniques, making them ideal for versatile applications [7]. Unlike metals, semiconductors allow for efficient gate control of spin states, longer spin relaxation times, and enhanced spin coherence over extended distances, which are crucial for robust spintronic functionality [8]. Additionally, semiconductor spintronics can use established semiconductor fabrication processes, allowing for easier integration with existing electronic and optoelectronic platforms, which is challenging in metal-based systems [6, 9]. In Section 1.1.2, we examine how semiconductor spintronics combines the magnetic functionality of traditional spintronics with the adaptability of semiconductors, enabling a new class of devices that are more efficient, multifunctional, and scalable for future technologies [10].

1.1.2 Semiconductor spintronics

Spintronics utilizing semiconductors offers the significant benefit of merging the capabilities of magnetic materials, such as current control by spin manipulation and nonvolatility, with the functionalities of semiconductors, including gate-controlled current and optical coupling. Datta and Das [6] introduced the concept of a spin-effect transistor (spin FET) that utilizes spin transport in lateral semiconductor channels, connecting spin-polarized sources and drains, with spin transmission regulated by a field-effect gate (Figure 1.2). Spin precession can be controlled via spin-orbit coupling. The three components essential for a spin transistor are (1) an extended relaxation period of a semiconductor, (2) gate voltage modulation of the spin-orbit coupling, and (3) elevated spin injection coefficients. Optical tests have demonstrated that the electron spins in semiconductors exhibit prolonged relaxation times. Gate voltage has been reported to modulate the spin-orbit splitting at the Fermi level for both electrons and holes across various semiconductors.

The fundamental challenge in spin injection arises from the conductivity mismatch between a ferromagnetic metal emitter and a semiconductor. Research indicates that the spin injection coefficient in a diffusive regime, denoted as γ, is defined as

$$\gamma \propto \frac{\sigma_N}{\sigma_F} \quad (1c)$$

where σ_N and σ_F are the conductivities of a normal (N) and FM contacts, then

$$\frac{\sigma_N}{\sigma_F} \gg 1 \quad (1d)$$

when N is a paramagnetic metal, and

$$\frac{\sigma_N}{\sigma_F} \ll 1 \quad (1e)$$

when N is a semiconductor [11]. This distinction clarifies why spin injection from a

ferromagnetic source into a paramagnetic metal is highly efficient; however, performing the same injection into a semiconductor encounters significant challenges. The difference arises due to mismatched electronic properties and spin lifetimes, which make efficient spin transfer into semiconductors more complex.

1.2 Materials for semiconductor spintronics

In spintronic devices, the choice of ferromagnetic (FM) materials and semiconductors is crucial for achieving efficient spin injection, transport, and detection. Ferromagnetic metals such as cobalt (Co), iron (Fe), and nickel (Ni), and their alloys, are commonly used for their high spin polarization at the Fermi level, which enables the injection of spin-polarized electrons into adjacent non-magnetic layers [7]. Additionally, half-metallic ferromagnets, like chromium dioxide (CrO_2) and certain perovskite oxides (e.g., $La_{0.7}Sr_{0.3}MnO_3$), exhibit nearly 100% spin polarization [12]. These materials are particularly advantageous for spintronic applications as they provide a high degree of spin polarization, which is essential for maximizing the efficiency of spin injection and enhancing the overall signal [13].

On the semiconductor side, materials such as gallium arsenide (GaAs), indium arsenide (InAs), and silicon (Si) are commonly employed as spin channels [14]. These semiconductors are selected based on factors like their spin diffusion length, spin lifetime, and the presence of spin-orbit coupling, which are critical for sustaining spin coherence over longer transport distances. GaAs, for instance, has a relatively long spin lifetime, making it suitable for sustaining spin polarization over considerable distances [15]. InAs, on the other hand, exhibits strong spin-orbit coupling, which not only preserves spin coherence but also allows for electrical control of spin precession, a valuable feature for

spin manipulation in devices such as the spin field-effect transistor (spin-FET) [6].

The interface between ferromagnets and semiconductors plays a pivotal role in determining the efficiency of spin injection and detection. Direct metal-semiconductor interfaces can suffer from conductivity mismatch, which can limit spin injection efficiency. To overcome this, tunneling barriers, such as thin oxide layers (e.g., MgO or Al_2O_3), are often introduced between the FM and semiconductor layers. These barriers create conditions for spin-conserved tunneling, which improves the injection efficiency by aligning the density of states and facilitating spin-selective electron transport [16].

For spin detection, semiconductors coupled with ferromagnetic contacts enable spin accumulation at the FM/semiconductor interface, which can be detected through techniques like magnetoresistance (MR) measurements. By monitoring changes in resistance as the relative magnetization of FM contacts is altered by an external magnetic field, spin accumulation in the semiconductor can be observed [17]. This technique, integral to spin valve structures, allows for the readout of spin information, which is crucial for developing spin-based memory and logic devices.

1.3 Spin orbit coupling

Spin-Orbit Interaction (SOI) is a quantum mechanical phenomenon arising from the coupling between an electron's spin and its orbital motion around the nucleus. As the electron moves through the electric field created by the positively charged nucleus primarily due to the Coulomb interaction it perceives, in its rest frame, an effective magnetic field. This field, in turn, interacts with the electron's intrinsic magnetic moment (its spin), creating the SOI. This interaction plays a crucial role in determining the electronic, magnetic, and optical properties of materials, as it links the electron's motion

to its spin orientation, leading to effects such as spin splitting and band structure modifications that are fundamental to spintronics and quantum computing applications.

1.3.1 Spin orbit coupling mechanism

The spin-orbit Hamiltonian is expressed as a function of the momentum operator (P) as follows [19]:

$$H_{SO} = \frac{e\hbar}{4m^2c^2}(\nabla \mathrm{V} \times \mathrm{P}) \cdot \sigma = \frac{-e\hbar}{4m^2c^2}(\mathrm{E} \times \mathrm{P}) \cdot \sigma \quad (1\mathrm{f})$$

Where:

- e is the charge of the electron.
- $\hbar$ is the reduced Planck's constant.
- m is the electron mass.
- c is the speed of light.
- $\nabla \mathrm{V}$ represents the gradient of the electric potential V
- P is the electron's momentum operator.
- σ represents the Pauli matrices corresponding to the electron's spin.

The spin-orbit interaction may occur in solids as a result of (i) an internal potential gradient and/or (ii) an externally applied electric field. Both Dresselhaus and Rashba spin-orbit interactions are identified as contributing factors to spin splitting in the absence of a magnetic field. Dresselhaus spin-orbit interaction (SOI) is prevalent in wide bandgap semiconductors, whereas Rashba SOI is more prominent in narrow bandgap semiconductors [18]. Additionally, the Rashba spin-orbit interaction can be adjusted through the application of bias.

1.3.2 Rashba SOC

The Rashba Spin-Orbit Interaction (SOI) is a quantum phenomenon that occurs in systems lacking structural inversion symmetry, often due to band bending at surfaces or interfaces. This asymmetry creates an internal electric field that couples an electron's spin to its momentum, described by the Rashba Hamiltonian [19]

$$H_R = \alpha(\sigma_x k_y - \sigma_y k_x) \quad (1g)$$

describes this interaction, where α represents the Rashba SOI strength and k_x and k_y are components of the electron's wavevector (momentum) in the x and y directions. Applying an external electric field further enhances this coupling, leading to an induced Rashba parameter α_{ind}, which allows precise control of spin states via the electric field. In the presence of both electric and magnetic fields, the Hamiltonian adjusts to [20]

$$H_R(F,B) = \alpha_{ind} k_i(B) eF \quad (1h)$$

$$\text{where, } k_i(B) = \sqrt{\frac{2eB}{\hbar}}$$

depends on the magnetic field. Rashba SOI is significant in spintronics, enabling spin manipulation via electric fields, which is advantageous for low-power spintronic devices, spin-based transistors, and quantum computing.

In a ferromagnet/semiconductor/ferromagnet (FM/SC/FM) spin valve, Rashba spin-orbit interaction (SOI) can be utilized to enhance spin manipulation within the semiconductor (SC) layer. The Rashba SOI, induced by structural inversion asymmetry (e.g., an applied electric field across the SC), creates an effective magnetic field that couples with electron spins. This interaction enables gate-controlled spin precession as electrons pass through the SC layer, allowing the alignment or misalignment of spins with the magnetization of the FM layers. By tuning the Rashba SOI strength, one can control spin transport properties in the SC channel, which enhances spin injection, modulation, and detection

in the spin valve, ultimately improving device performance and enabling dynamic control of spin currents in FM/SC/FM structures [21-23].

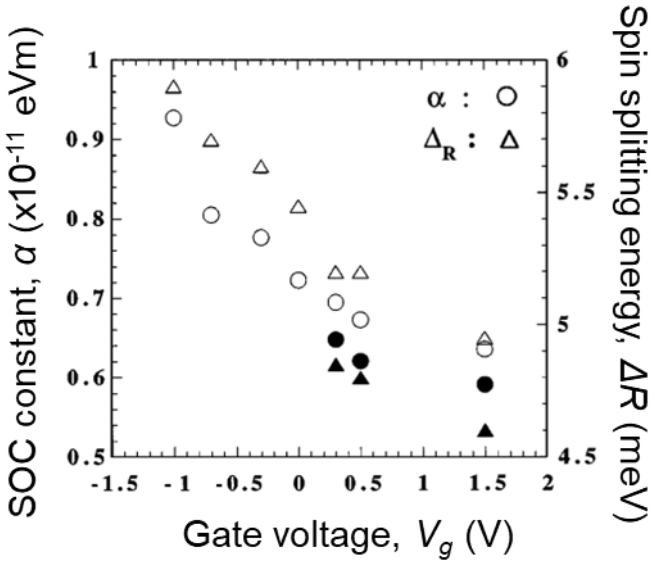

Figure 1.4 SOC constant (α) can be modulated by gate voltage modulation [23].

1.4 Spin valve

The giant magnetoresistance (GMR) effect can be observed in a trilayer junction, shown on Fig. 1.5, where a non-magnetic (NM) spacer layer is positioned between two ferromagnetic (FM) electrodes. The junction's resistance varies based on the alignment of the FM electrode magnetizations, switching between high and low values. This trilayer structure acts as a spin valve, allowing electrical current to be turned on or off by an external magnetic field that controls the FM alignment.

There are three main types of spin valves, defined by the spacer material and its thickness:

1. Metal Spacer: A metal spacer typically exhibits a low magnetoresistance (MR) relative to the junction's volume resistance [24]. To enhance MR, superlattice structures can increase the number of interfaces while maintaining consistent thickness and volume

resistance [25-28]. For thin metal spacers, usually less than a few nanometers, MR arises from indirect exchange coupling between magnetic layers [29,30].

2. Thick Semiconductor Spacer: With a thick semiconductor spacer, the FM layers are magnetically decoupled, and transport through the spacer becomes diffusive. Here, MR depends on spin injection, which is challenging to achieve with metal/semiconductor contacts. Tunneling through a barrier between the FM and semiconductor enables more efficient spin injection [31-34].

3. Thin Insulator Spacer: For a thin insulating spacer, transport relies on spin-conserved tunneling between electrodes, with MR influenced by the alignment of spin polarization in the tunneling process.

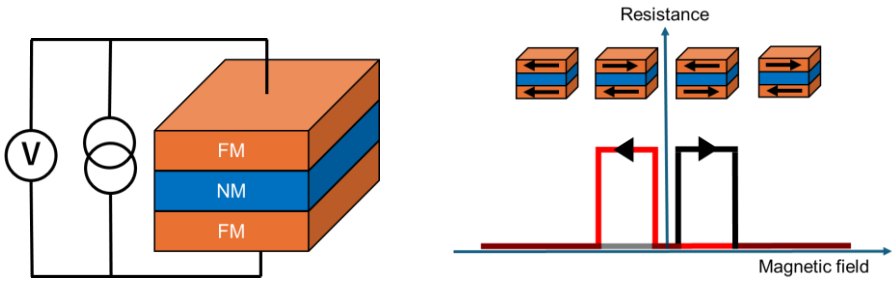

Figure 1.5 Schematic of spin valve operation.

1.4.1 Lateral and vertical spin valve

The resistance of a spin valve junction varies between two distinct states, depending on whether the magnetizations of the ferromagnetic (FM) metal layers are aligned parallel or antiparallel to each other. This alignment determines the ease with which spin-polarized electrons traverse the device, directly impacting the observed resistance. Spin valve devices are broadly categorized into two structural configurations: (i) Lateral Spin Valve (LSV) and (ii) Vertical Spin Valve (VSV), each with unique design and operational

characteristics.

In the lateral spin valve (LSV) configuration, FM electrodes are deposited on the surface of a non-magnetic (NM) layer, allowing the spin-polarized current to flow laterally, parallel to the plane of the device. This setup, referred to as a current-in-plane (CIP) geometry, maintains the spin current along the same horizontal plane as the FM and NM layers, resulting in a compact, planar design (Fig. 1.6). CIP geometry is advantageous for applications that benefit from low-resistance paths and efficient spin current propagation along the lateral interface, often favored in all-metal spintronic devices [35].

In contrast, the vertical spin valve (VSV) configuration places the NM layer between two FM electrodes in a stacked, layered arrangement. Here, the spin-polarized current flows perpendicularly through the NM spacer, creating a current-perpendicular-to-plane (CPP) geometry (Fig. 1.5). This CPP setup enables direct interaction between the FM electrodes through the spacer, often resulting in enhanced magnetoresistance due to the reduced spin diffusion length required for current traversal. The vertical alignment is particularly suitable for high-density, multilayered structures where vertical current flow and efficient spin injection across the interfaces are critical for device performance [36,37].

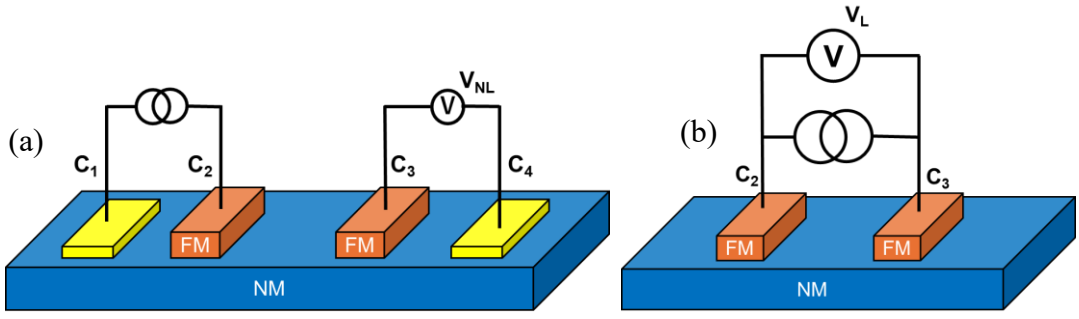

Figure 1.6 (a) Non-local and (b) Local measurement configuration of a lateral spin valve.

1.4.2 Spin signal measurement

In lateral spin valves (LSVs) configured in a current-in-plane (CIP) geometry, the spin valve signal can be measured using either local or non-local measurement techniques, each providing insight into different aspects of spin transport. In both cases, the resistance either non-local (R_{NL}) or local (R_L) is measured as a function of an applied in-plane magnetic field.

The non-local measurement setup, illustrated in Fig. 1.3 (a), involves four electrodes: C_2 and C_3, which are ferromagnetic (FM) electrodes, and C_1 and C_4, which ideally are non-magnetic metals. In this configuration, an injection current is applied between electrodes C_1 and C_2, while the voltage is detected across C_3 and C_4, forming a non-local circuit. Here, C_2 functions as the spin injector, and C_3 as the spin detector, taking advantage of the spin-dependent density of states (DOS) in FM materials at the Fermi level [38, 39].

As spins are injected from C_2, they diffuse on both sides of the injector, creating a spin accumulation that spreads through the device. To measure pure spin current without interference from charge current, the voltage is detected non-locally across C_3 and C_4, which remain isolated from the charge flow path. This non-local measurement technique effectively decouples spin current from charge current, allowing for an accurate assessment of the spin signal. By dividing the measured voltage across C_3 and C_4 by the injection current, the non-local resistance is obtained. The non-local spin signal, ΔR_{NL}, can be calculated by [40]:

$$\Delta \mathrm{R_{NL}} = \frac{V_{NL}^{P} - V_{NL}^{AP}}{I} = \frac{P^2 \lambda_s}{2W\sigma} e^{-L/\lambda_s} \quad (1i)$$

where V_{NL}^{P} and V_{NL}^{AP} are non-local voltages measured across C_3 and C_4 for parallel and antiparallel magnetization states, I is the injection current, P is spin injection/detection efficiency, λ_S is spin diffusion length, W is width of non-magnetic strip, σ is conductivity and L is separation between central FM electrodes.

The local measurement technique involves measuring the two-terminal resistance across the two ferromagnetic electrodes. In this process, a spin-polarized current is injected from one ferromagnetic metal, travels through the non-magnetic layer, and is detected by the other ferromagnetic film. Figure 1.3 (b) illustrates the local measurement setup, showing that current is applied between C_2 (FM) and C_3 (FM), while voltage is measured across the same electrodes. The identification of spin valve signals in a local configuration presents considerable challenges, primarily due to the influence of charge current, which generates a substantial background signal. The non-local measurement technique offers advantages compared to the local technique due to the absence of charge current between the injector and detector [41].

The spin valve signal in vertical magnetic junctions, utilizing CPP geometry, can be measured by assessing the magnetoresistance ratio (MR) as a function of the magnetic field. The schematic illustrating spin transport measurement for vertical structures is presented in Fig. 2b. In this setup, an in-plane magnetic field (B) is varied to obtain both parallel and antiparallel magnetization states. Magnetoresistance (MR) is low when the magnetizations of the two ferromagnetic electrodes, FM_1 and FM_2, are oriented in a parallel configuration, and high when they are oriented antiparallel. The MR is assessed utilizing the relationship [42]

$$MR = \frac{R_{AP} - R_P}{R_P} \quad (1j)$$

where R_{AP} is resistance corresponding to antiparallel magnetization configuration and R_P

is resistance for parallel configuration.

1.5 Motivation and organization of the thesis

1.5.1 Overall objective

The primary objective of this work is to achieve high-quality MnAs/InAs/MnAs double heterostructures on GaAs (111) B using low-temperature molecular beam epitaxy (LT-MBE), which is a novel approach towards spin-FET realization. Although there have been research related to MnAs/InAs/MnAs thin trilayer on GaAs (111) B [43], but to the best of our knowledge, no work has been done that specifically investigate MnAs/InAs/MnAs thick double heterostructure on GaAs (111) B for the purpose of vertical spin-FET application. The key challenges in this study center on enhancing the quality of the LT-grown InAs layer and optimizing its interfaces with MnAs, as these factors critically impact the device performance. Our previous investigations with MnAs/InAs-based hybrid structures have shown promising outcomes in in-plane device applications [44]. However, the device design was limited by photolithography constraints, restricting the channel length to no less than 1 μm. While preliminary spin valve signals were observed, they lacked clarity, likely due to substantial impedance mismatch between the ferromagnetic (FM) and semiconductor (SC) layers.

To address this limitation, our approach focuses on reducing the channel length of the spin injection region. Decreasing the channel length is expected to significantly improve spin injection efficiency by increasing the current density and enhancing spin accumulation, which, in turn, boosts spin polarization and shortens the electron diffusion length. Therefore, in this study, we aim to grow MnAs/InAs/MnAs vertical double heterostructures in which the InAs channel is sandwiched between the MnAs source and

drain.

This vertical geometry presents a distinct advantage: it enables precise control over the InAs channel length on the nanometer scale through MBE growth techniques, allowing for significantly shorter channels than those achievable with conventional photolithography. By reducing the channel length to nanoscale dimensions, the vertical structure is anticipated to minimize impedance mismatch and increase the efficiency of spin injection, which are crucial for robust spintronic device performance.

To realize MnAs/InAs/MnAs vertical hybrid structures through MBE, it is essential to adjust the growth temperature. While the typical growth temperature for InAs in MBE is approximately 480°C [45], MnAs growth is conventionally performed at lower temperatures, around 200-300 °C. Thus, our approach involves developing an optimal growth protocol at reduced temperatures to achieve high-quality InAs and well-defined interfaces with MnAs. Ensuring a good surface and interfacial quality is essential for reliable device operation and improved spin transport properties.

Finally, with the improved vertical MnAs/InAs/MnAs structure, we expect to achieve enhanced spin injection efficiency facilitated by the shortened channel length, which we plan to evaluate through local spin valve (LSV) device fabrication and measurement.

1.5.2 Selection of ferromagnetic source/drain (MnAs)

We choose MnAs as the ferromagnetic (FM) source and drain for our spintronic device because it offers a combination of high Curie temperature, substantial spin polarization, and compatibility with III-As semiconductors. The Curie temperature (T_C) of MnAs, like that of other transition metals such as Fe, Co, and Ni, exceeds room temperature, enabling it to retain ferromagnetic behavior in practical operating conditions. This characteristic

makes MnAs particularly suitable for devices that need to operate at or above room temperature, a critical requirement for many spintronic applications.

One of the compelling reasons for selecting MnAs over other ferromagnetic metals is its high degree of spin polarization. MnAs exhibits a clear difference in up-spin and down-spin density of states at the Fermi level, with around 50% spin polarization at this energy level [46, 47]. This property allows MnAs to serve as an efficient spin injector, which is vital for effective spin transport in spintronic devices. Achieving a substantial spin polarization at the Fermi level enhances the device's performance by maximizing the spin-polarized current.

Another key advantage of MnAs over other ferromagnetic transition metals, such as Fe, Co, and Ni, is its compositional compatibility with III-As semiconductors. When transition metals like Fe are deposited on III-As substrates, unintentional reactions at the FM/semiconductor (FM/SC) interface can occur, resulting in the formation of magnetically dead layers (MDLs) that degrade the interfacial spin properties [48]. For instance, in systems like Fe/GaAs or Co/GaAs, interactions between the metal and semiconductor can lead to unwanted atomic mixing, creating a detrimental MDL that hampers spin injection efficiency and stability [49, 50]. This MDL issue is particularly troublesome in spintronic devices, where a clean and well-defined interface is essential for optimal performance.

In contrast, MnAs inherently contains arsenic (As) in its crystal structure, minimizing the likelihood of interfacial mixing with III-As materials. Since MnAs itself is an arsenide, its growth on III-As semiconductors can occur without forming unwanted interfacial compounds, thus avoiding the MDL issue that is often seen with other FM/SC interfaces [51, 52]. This intrinsic compositional compatibility provides a stable interface and

preserves the magnetic and spin properties across the junction, which is critical for reliable spintronic device functionality.

MnAs can be epitaxially grown on GaAs substrates, specifically on GaAs (111) B surfaces, which supports a hexagonal NiAs-type structure with the c-axis aligned perpendicular to the substrate. This orientation results in an almost isotropic magnetic response in the in-plane directions, which is desirable for spintronic applications that require uniform magnetic behavior. When grown on GaAs (001) substrates, MnAs typically forms a mixed phase, combining both hexagonal (ferromagnetic) and orthorhombic (nonmagnetic) regions, leading to lateral magnetic anisotropy that complicates device behavior [53, 54]. The GaAs(111)B orientation, however, enables MnAs to maintain a single-phase hexagonal structure, simplifying the magnetic properties and enhancing control over the epitaxial growth direction, which is beneficial for device integration and performance [55].

Additionally, while Heusler alloys are known for their half-metallic nature, offering theoretically 100% spin polarization, they present significant challenges in achieving this ideal behavior in practice. Issues such as crystalline disorder, atomic displacement, misfit dislocations, and symmetry breaking at the film surface can lead to deviations from half-metallicity and even result in the formation of MDLs [56]. These factors reduce the actual spin polarization in Heusler alloy films, compromising their application as spin injectors in spintronic devices. In contrast, MnAs offers more consistent and reproducible magnetic and spin properties due to its stable epitaxial growth and absence of MDLs, making it a more reliable material choice for device applications.

Thus, MnAs is an advantageous material for spintronic devices. Its high Curie temperature, significant spin polarization, stable interface with III-As semiconductors,

and controlled growth on GaAs(111)B substrates make it an ideal FM source and drain for reliable and efficient spintronic device performance.

1.5.3 Selection of semiconductor channel (InAs)

We select InAs as the semiconductor channel material in our study due to its narrow band gap, unique electronic properties, and compatibility with ferromagnetic (FM) materials like MnAs, making it an ideal candidate for future spin field-effect transistor (spin-FET) applications. InAs, a III-As semiconductor with a zinc-blende crystal structure, possesses a narrow band gap of 0.35 eV at room temperature, along with a naturally occurring surface electron accumulation layer [57]. This accumulation layer, with its triangular potential well, enables high conductivity without the need for intentional doping, making InAs a readily conductive channel material. Furthermore, InAs has a large split-off energy, which correlates with a higher degree of spin-orbit coupling (SOC), a critical requirement for spin-FET operation, where the SOC facilitates the spin precession of carriers within the channel.

The strong SOC in InAs is particularly advantageous for spintronic applications, as it enables efficient spin manipulation within the channel. This characteristic has already positioned InAs as a promising channel material for spin injection and detection experiments with ferromagnetic contacts [58, 59]. However, achieving a high-quality two-dimensional electron gas (2DEG) in epitaxially grown InAs remains essential to optimize its performance as a channel material.

InAs growth on a GaAs (111) B substrate is particularly beneficial for reducing dislocation-related degradation of its physical and electronic properties. On the GaAs (111) B orientation, InAs has three in-plane sliding planes, which promote dislocation

density annihilation and inhibit three-dimensional growth at the interface, improving the material quality by reducing defect density at the interface [60]. The dislocation network on the (111) B plane also contributes to improved electrical properties of the InAs channel compared to growth on GaAs (001), where dislocation-related degradation is more significant. This attribute is essential for high-performance spintronic applications where carrier mobility and low defect density are critical.

While there have been previous attempts to create MnAs/InAs heterostructures with ultra-thin InAs layers (less than 10 nm) on GaAs (111) B [63] and GaAs (100) [61], there is limited exploration into the direct growth of InAs on MnAs layer on GaAs (111) B, particularly in configurations optimized for vertical electrical and spin transport. Additionally, we would like to grow InAs at lower growth temperature than usual. The usual growth temperature of InAs in MBE is ~480 ^{o}C. To obtain the vertical structures, it will be required to apply growth at low temperature (LT) to match the usual growth temperature of MnAs (200-300 ^{o}C). The lower substrate temperature during LT-InAs growth can result in reduced surface mobility of indium adatoms and excess As concentration, leading to the formation of several defects. There has been little research on the structural, electrical, and morphological [62, 63] aspects of LT-InAs. M. Takushima et al. [64] have shown effect of excess As in LT-InAs on InAs substrates and consequent lattice mismatch and electrical properties. Nevertheless, there is still insufficient information on the relationship among growth conditions, lattice deformation, and electrical characteristics and almost no information about using GaAs (111) B as the substrate. In this work, we also tried to dive into these issues.

Therefore, to clearly outline the purpose of this study, **Chapter 1** provides the background and motivation, including the fundamental concepts relevant to this research. **Chapter 2** details the epitaxial growth process of MnAs/InAs/MnAs on GaAs(111)B, examining the structural, morphological, basic electrical, and magnetic properties of the resulting double heterostructures. In **Chapter 3**, we shall discuss the properties of LT-InAs and describe about the possible defects formation due to low growth temperature. **Chapter 4** describes the fabrication of vertical spin valve using the double heterostructure and the local spin valve measurement results. **Chapter 5** summarizes the whole work and discuss about the future prospects.

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Chapter 2: Molecular beam epitaxial (MBE) growths

2.1 Overview of MBE system

Molecular Beam Epitaxy (MBE) is a highly precise technique for thin-film deposition, widely used in the fabrication of high-quality semiconductor materials and heterostructures. Developed in the late 1960s, MBE is distinguished by its ability to control growth at the atomic layer level, making it an essential tool in materials science, particularly for the growth of compound semiconductors [1]. MBE operates in an ultra-high vacuum (UHV) environment, where elemental or molecular beams are directed onto a heated substrate, allowing for epitaxial layer formation through controlled atomic or molecular interactions on the substrate surface [2].

The unique advantage of MBE lies in its ability to achieve monolayer control, facilitated by the ultra-slow deposition rates (typically on the order of one monolayer per second or slower). This controlled deposition enables the growth of complex structures with abrupt interfaces and atomically smooth surfaces, making MBE ideal for applications requiring precise layer composition, such as quantum wells, superlattices, and other low-dimensional structures [3]. The UHV environment minimizes contamination, preserving the purity of the deposited films and enhancing crystalline quality [4].

In MBE, the growth process is often monitored in real-time using techniques like Reflection High-Energy Electron Diffraction (RHEED). RHEED provides immediate feedback on surface crystallography and morphology, enabling adjustments during growth and allowing researchers to maintain control over atomic-scale features.

Additionally, MBE systems can incorporate effusion cells for elemental sources, cracker cells for molecular species, and shutters to modulate beam fluxes, allowing for precise control of stoichiometry and doping levels [5].

Figure 2.1 illustrates the basic configuration of our ultra-high vacuum (UHV) molecular beam epitaxy (MBE) system, which is designed to maintain an extremely low contamination environment essential for high-quality thin-film growth. The system consists of three interconnected chambers: the load lock chamber, the buffer chamber, and the main growth chamber. Each chamber is isolated from the others by gate valves (GV) to ensure a controlled flow of samples and to protect the ultra-high vacuum conditions of the main growth area.

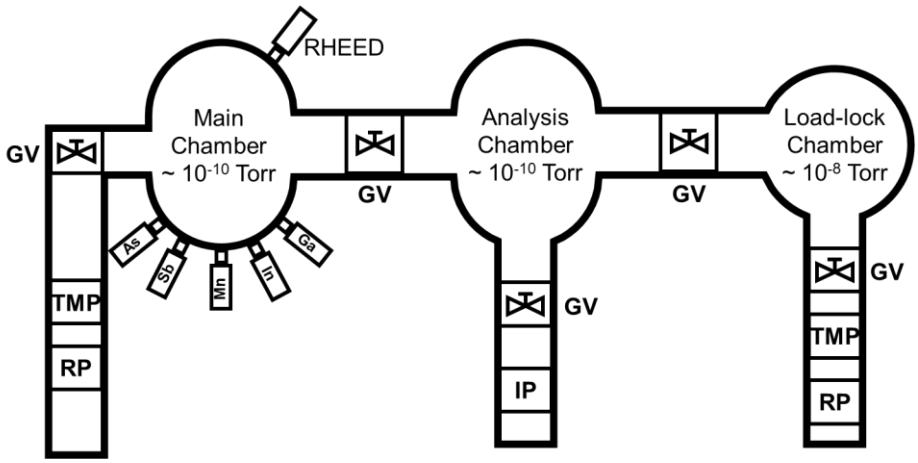

Figure 2.1 Simple illustration of our MBE system.

The load lock chamber is the entry point for samples and allows for initial pumping and outgassing before they proceed into the UHV environment. This chamber enables samples to be loaded and unloaded without compromising the vacuum integrity of the main chamber, minimizing potential contamination from exposure to atmospheric conditions. Once a sample is loaded into the load lock chamber, it undergoes preliminary evacuation to remove residual gases, which is crucial for preserving the high vacuum in

subsequent stages.

Between the load lock and the main growth chamber lies the buffer chamber (analysis chamber), serving as an intermediary zone that further reduces the risk of atmospheric exposure to the primary growth area. The analysis chamber isolates the main chamber from direct exposure to the load lock chamber and allows for additional outgassing if needed. This configuration prevents abrupt pressure changes in the main chamber and ensures that any contaminants introduced in the load lock do not immediately reach the growth environment, thereby safeguarding the UHV conditions required for MBE.

The main growth chamber is the heart of the MBE system, where the actual thin-film growth occurs. This chamber houses the source cells, typically effusion cells, which contain the elemental or molecular sources (in our system: As, Sb, Ga, In and Mn) for the epitaxial growth process. The growth chamber is equipped with an in-situ Reflection High-Energy Electron Diffraction (RHEED) system, allowing for real-time monitoring of the surface structure, growth rate, and layer quality during deposition.

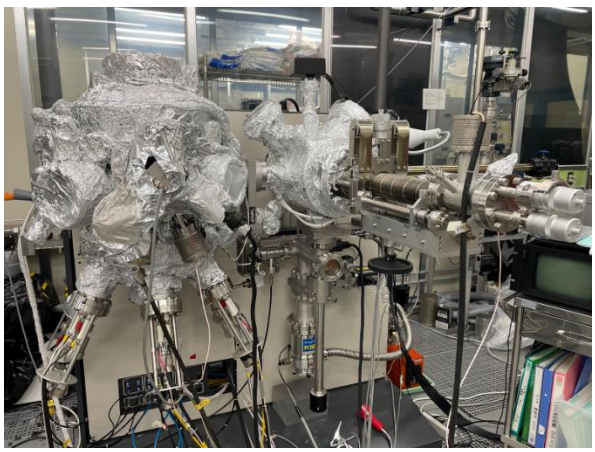

Figure 2.2 EIKO MBE system we used.

Each chamber is continuously evacuated by dedicated pumping systems, typically including rotary pumps (RP), turbo-molecular pumps (TMP) and ion pumps (IP), to

maintain the required vacuum levels. The main growth chamber, in particular, is maintained at ultra-high vacuum levels (10^{-10} to 10^{-11} Torr) to prevent contamination, ensuring that only the intended atoms or molecules interact with the substrate surface. This stringent vacuum control is critical for high-purity epitaxial growth, allowing the fabrication of materials with sharp interfaces and minimal defect density.

2.2 MBE growth

A semi-insulating GaAs (111) B substrate with dimensions of 15 mm × 12 mm was prepared for growth by undergoing a thorough cleaning process. Initially, organic cleaning was performed using acetone, methanol, and deionized water (DIW), followed by inorganic cleaning with Semico Clean 23 from Fruuchi Chemical. After cleaning, the substrate was mounted onto a molybdenum block sample holder using pure indium to secure it, and then loaded into a solid-source MBE system.

The substrate first underwent initial degassing in the load lock chamber to reduce surface contaminants. Following degassing, it was transferred to the analysis chamber, where it was preheated to approximately 370°C under vacuum conditions. This step helped to further desorb any remaining surface impurities. Subsequently, the substrate was moved to the growth chamber, where it was exposed to an arsenic (As) ambient. Thermal cleaning was performed at approximately 580°C for 15 minutes to remove surface oxides and achieve a clean, oxide-free surface, ready for high-quality epitaxial growth.

2.2.1 Low-temperature (LT) InAs

One of the major challenges in achieving a high-quality MnAs/InAs/MnAs double heterostructure was optimizing the growth of low-temperature (LT) InAs (~250 ºC) with sufficient crystalline and interface quality [6-11]. Attaining a high-quality LT-InAs layer is essential, as it forms the central channel layer in the heterostructure, directly impacting the overall device performance. To address this, we conducted a systematic investigation to determine the optimal growth conditions for LT-InAs.

Our approach involved varying multiple parameters, including the substrate temperature during growth and the beam equivalent pressure (BEP) ratio of indium (In) to arsenic (As). By adjusting these parameters, we aimed to control the surface morphology, crystallinity, and stoichiometry of the LT-InAs layer, which are crucial for minimizing defects and achieving a smooth, uniform layer. Each variation in growth temperature and BEP ratio was carefully monitored to understand its effects on the InAs layer properties, allowing us to identify conditions that best support the desired quality for spintronic applications.

The detailed outcomes of these experiments, including the influence of specific growth temperatures and BEP ratios on the structural and electrical properties of LT-InAs, will be discussed in the next chapter. This investigation provides insights into the optimization process and the balance required to achieve good-quality LT-InAs suitable for integration into the double heterostructures.

2.2.2 InAs on MnAs

Informed by our previous successful MnAs growth on GaAs (111) B [12], we optimized growth conditions to produce a high-quality MnAs layer with an As/Mn BEP ratio close

to 234, maintaining an arsenic BEP of ~1.5×10^{-5} Torr. The growth temperature was ~ 250 ^{o}C. This careful balance yielded a MnAs layer with remarkably low surface roughness, as shown in Figure 2.3, indicating a highly uniform and smooth layer conducive to further heterostructure growth. The growth rate achieved was approximately 2.75 nm/min, providing a steady and reproducible basis for the next steps. Confident in the stability of these conditions, we decided to apply them to the initial MnAs layer in our planned double heterostructure.

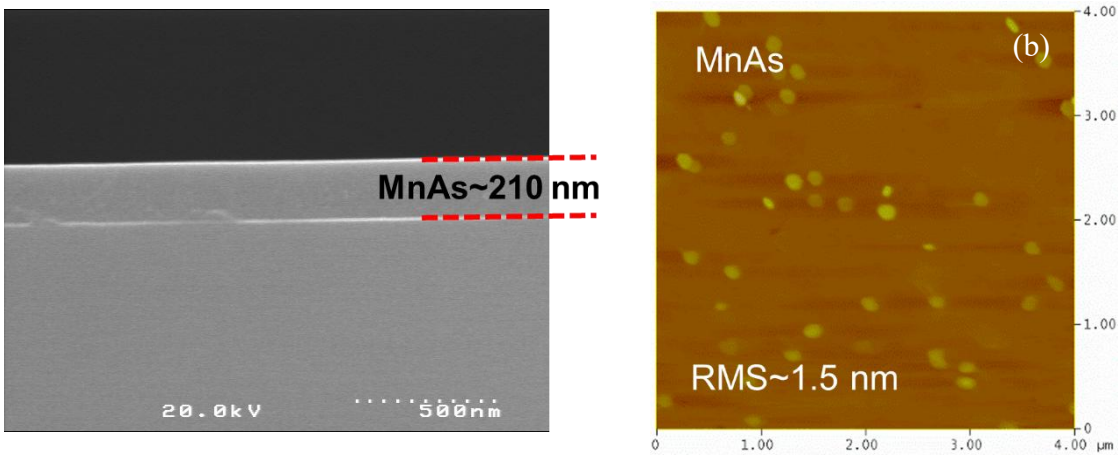

Figure 2.3 (a) SEM cross-section and (b) AFM surface morphology of MnAs on GaAs (111)B

In the next phase, we turned to the deposition of InAs on MnAs as one more step towards the double heterostructure. Recognizing the sensitivity of this structure to growth temperatures, we initially attempted InAs deposition at its standard growth temperature of approximately 480 °C, while maintaining the MnAs layer below it grown at its optimal temperature of around 250 °C.

The resulting sample had a very rough surface (Fig 2.4 b) with root mean square (RMS) of roughness around 77 nm. The rough surface obtained during the deposition of InAs on MnAs under these conditions can be attributed to several factors related to growth

temperature mismatch and material properties. The significant temperature increases from MnAs's optimal growth temperature (~250°C) to InAs's standard growth temperature (~480°C) likely caused thermal strain due to the mismatch in thermal expansion coefficients between the two materials, resulting in lattice distortions and surface roughening.

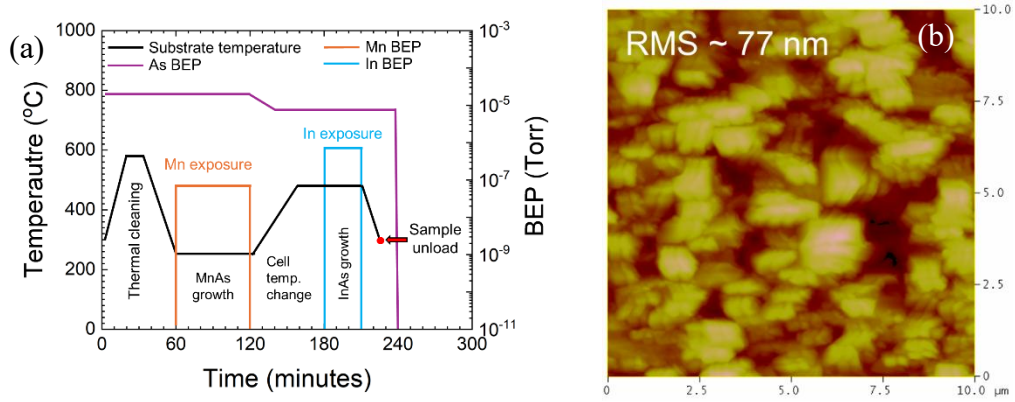

Figure 2.4 (a) MBE growth condition for InAs (HT) on MnAs and (b) AFM of InAs/MnAs surface.

Additionally, MnAs is sensitive to higher temperatures, and exposure to 480°C may have led to surface degradation, reconstruction, or partial desorption, compromising the interface for InAs growth. The temperature disparity may have also disrupted the nucleation process, leading to uneven growth and island formation.

Realizing the challenges associated with the temperature mismatch between MnAs and InAs growth, we adjusted our approach and attempted to grow InAs on MnAs at the same growth temperature as MnAs (~250°C). This adjustment significantly minimized the roughness of the surface, reducing it to approximately 7.5 nm (Figure 2.5).

The improvement in surface quality can be attributed to several factors. First, growing InAs at the same temperature as MnAs eliminated the thermal strain caused by the large temperature difference during the earlier attempts. By maintaining a consistent growth

temperature, we avoided the mismatch in thermal expansion coefficients that previously led to lattice distortions and surface irregularities. Second, the stability of the MnAs surface at its optimal growth temperature was preserved, preventing degradation or reconstruction that could compromise the interface. This stable interface provided a smoother foundation for InAs nucleation and growth.

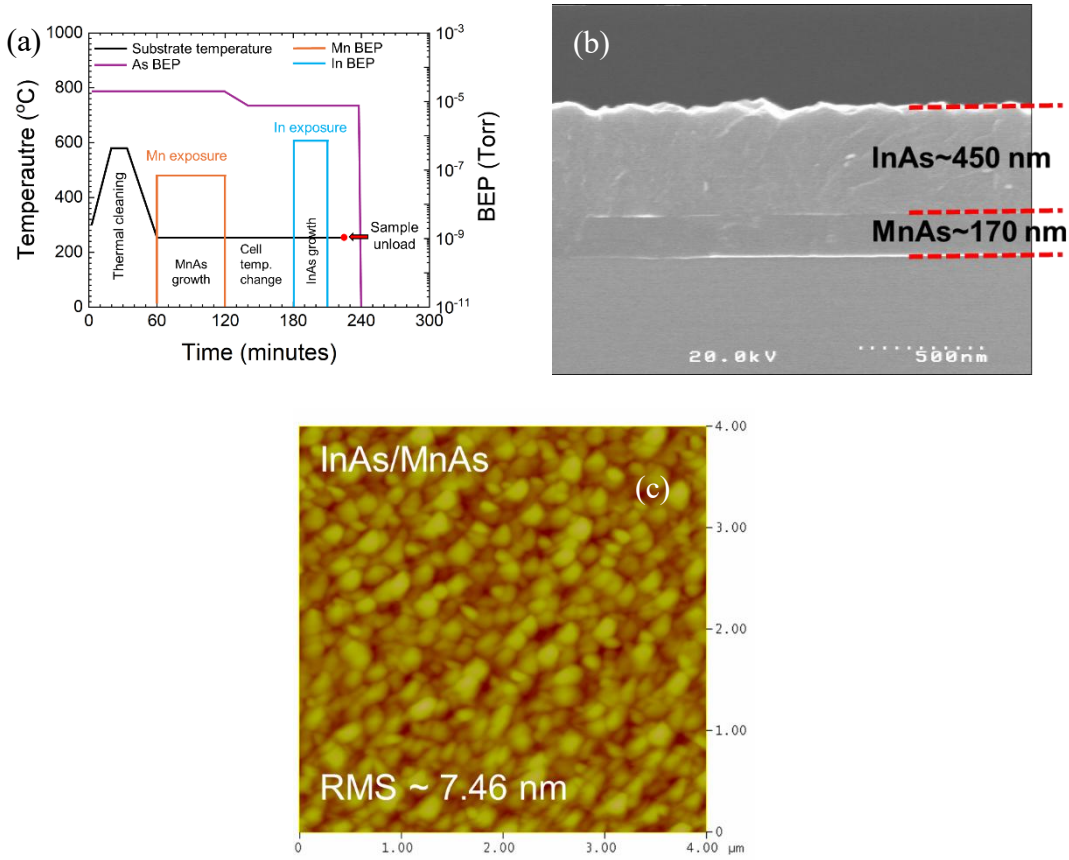

Figure 2.5 (a) Growth conditions, (b) SEM-cross section and (c) surface AFM of InAs (LT) on MnAs.

Thus, we proceed to double heterostructure with LT-InAs as the channel.

2.2.3 MnAs/InAs/MnAs double heterostructure (DH)

To construct the MnAs/InAs/MnAs double heterostructure, we designed the top and bottom MnAs layers with different thicknesses to achieve distinct coercive fields, a

critical requirement for spin valve measurements.

In a spin valve configuration, the ability to independently switch the magnetization of the two ferromagnetic layers is essential to control the relative magnetic alignment (parallel or antiparallel) and thereby modulate the spin-dependent transport properties. By varying the thickness of the MnAs layers, we exploit the thickness dependence of coercive fields: thinner ferromagnetic layers often exhibit higher coercive fields due to the dominance of pinning effects and surface anisotropies, which make it more difficult for magnetic domains to nucleate and move. On the other hand, thicker layers tend to have lower coercive fields because the volume of the material allows for easier domain wall motion and reduced impact of surface pinning. This engineered difference ensures that the magnetization of the two MnAs layers can be switched at different external magnetic field strengths, enabling the desired spin valve operation and reliable measurement of spin-dependent transport phenomena in the heterostructure.

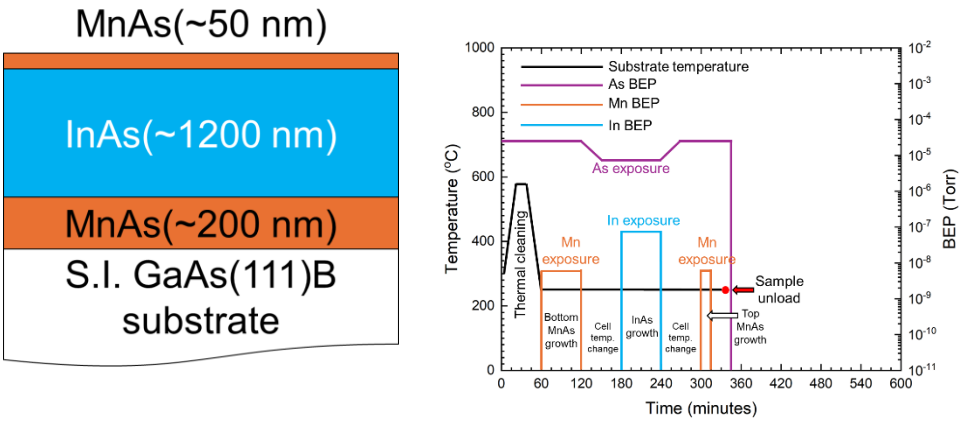

Figure 2.6 Schematic design and planned growth conditions of the double heterostructure.

We have grown several double heterostructure samples, changing the V/III BEP ratio of InAs to find an optimized condition. After the sample preparation and degassing in the analysis chamber, the sample was transferred to the growth chamber under an arsenic

(As) ambient with a beam equivalent pressure (BEP) of approximately 1.6×10^{-5} Torr. Thermal cleaning was conducted at ~580°C for 15 minutes to remove surface oxides and ensure a clean substrate surface. Following the cleaning process, the substrate temperature was reduced to 250°C, and the bottom MnAs layer was grown for 1 hour using an As/Mn BEP ratio of ~245.

The subsequent InAs growth was performed under controlled conditions. The indium (In) BEP was maintained at 7.6×10^{-7} Torr, while the arsenic-to-indium (As/In) BEP ratios were varied across three samples: 2, 10, and 20, corresponding to samples named V/III-2, V/III-10, and V/III-20, respectively. The growth duration for the InAs layer was 1 hour for each sample. Finally, the top MnAs layer was deposited for 15 minutes under the same conditions as the initial MnAs layer, ensuring consistency in growth parameters and quality.

Table 2.1 Growth conditions of DHs

Sample name	Mn BEP (Torr)	As BEP (Torr)	In BEP (Torr)	V/III BEP ratio	Growth temperature (°C)	Top MnAs thickness (nm)	Bottom MnAs thickness (nm)	InAs thickness (μm)
V/III-2	6.5×10^{-8}	1.6×10^{-6}	7.6×10^{-7}	2	~250 °C	~200	~50	1.1
V/III-10		7.6×10^{-6}		10		~180	~46	1.2
V/III-20		1.6×10^{-5}		20		~190	~47	1.23

The growth of the three distinct layers—bottom MnAs, InAs, and top MnAs—was confirmed using scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS). Cross-sectional observations revealed clearly distinguishable layers of MnAs and InAs. Figure 2.7 presents cross-sectional backscattered electron (BSE) images, along with elemental mappings for manganese (Mn) and indium (In), and their corresponding line profiles.

The elemental mappings and line profiles confirmed the formation of a sandwiched

structure, with bottom and top MnAs layers enclosing the InAs layer in all three samples. However, the interfaces between these layers varied in quality. For the V/III-2 sample, the interfaces, both bottom MnAs/InAs and top MnAs/InAs, appeared less uniform compared to the other two samples. This was attributed to the lower quality of the InAs layer grown with an As/In BEP ratio of 2, which exhibited the highest surface roughness among the three variations. In contrast, the V/III-10 and V/III-20 samples displayed improved interface quality, with V/III-10 showing slightly better results overall. These findings align with the characteristics of the individually grown InAs layers, where smoother InAs surfaces directly translated to higher-quality interfaces in the heterostructure.

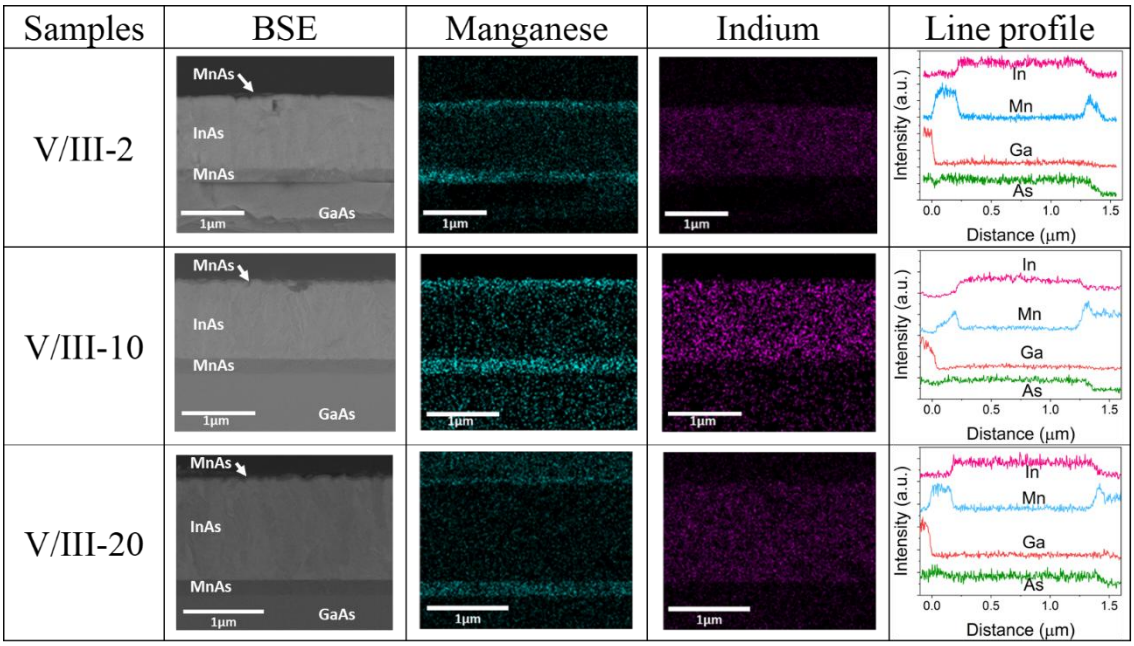

Figure 2.7 SEM-EDS analysis of cross-section of double heterostructures.

The measured thicknesses of the bottom MnAs layers were approximately 200 nm, 180 nm, and 190 nm for the V/III-2, V/III-10, and V/III-20 samples, respectively. Despite slight variations, the growth rates of the bottom MnAs layers—0.055 nm/s, 0.05 nm/s,

and 0.053 nm/s for V/III-2, V/III-10, and V/III-20, respectively—were nearly identical. Minor differences likely resulted from fluctuations in the effusion cell temperature. The top MnAs layers exhibited consistent growth across all samples, with thicknesses of 50 nm, 46 nm, and 47 nm, maintaining a ~1:4 ratio of top-to-bottom MnAs layer thickness corresponding to the growth times.

For the InAs layer, the observed thicknesses were ~1.1 µm (0.305 nm/s), 1.2 µm (0.33 nm/s), and 1.23 µm (0.34 nm/s) for V/III-2, V/III-10, and V/III-20, respectively. These values were consistent with those obtained from single InAs layer growths on GaAs (111)B substrates. The thickness and growth rates reflect the varying As/In BEP ratios and further highlight the impact of growth conditions on surface roughness and interface quality.

The crystal structure and epitaxial growth of the double heterostructure were analyzed using X-ray diffraction (XRD) measurements (rocking curve) (Figure 2.8). The results of the 2θ scan, performed between 20° and 40°, are shown in Fig. 3. Distinct peaks corresponding to InAs(111), GaAs(111), and MnAs(0002) were clearly observed from the low-angle side, confirming the presence of the respective layers.

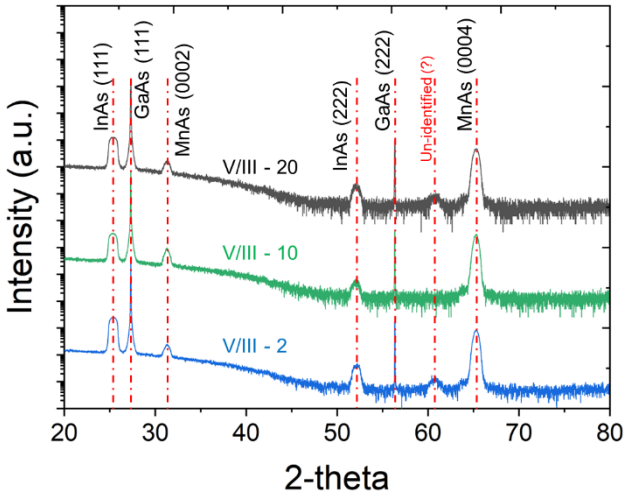

Figure 2.8 XRD measurement of the DHs.

From the XRD analysis, the lattice parameters of cubic InAs and GaAs were determined to be approximately 6.06 Å and 5.65 Å, respectively. For hexagonal MnAs, the c-axis lattice parameter was measured to be ~5.71 Å. These values align closely with their known bulk lattice parameters [13, 14], indicating that the epitaxial layers are strain-relaxed despite the inherent lattice mismatch between the materials. However, residual strain was later identified in the LT-InAs layer, a topic that will be explored in detail in the next chapter.

The V/III-10 sample appeared to be epitaxially grown, with no evidence of interdiffusion at the interfaces. In contrast, the V/III-2 and V/III-20 samples displayed a weak additional peak preceding the MnAs (0002) peak in the XRD scans. The origin of this peak is unclear, but it may indicate the occurrence of interdiffusion or interfacial reactions at the MnAs/InAs and InAs/GaAs interfaces in these samples. Such interactions could have led to the formation of a new compound or phase with distinct lattice parameters, thereby resulting in the observed additional peaks.

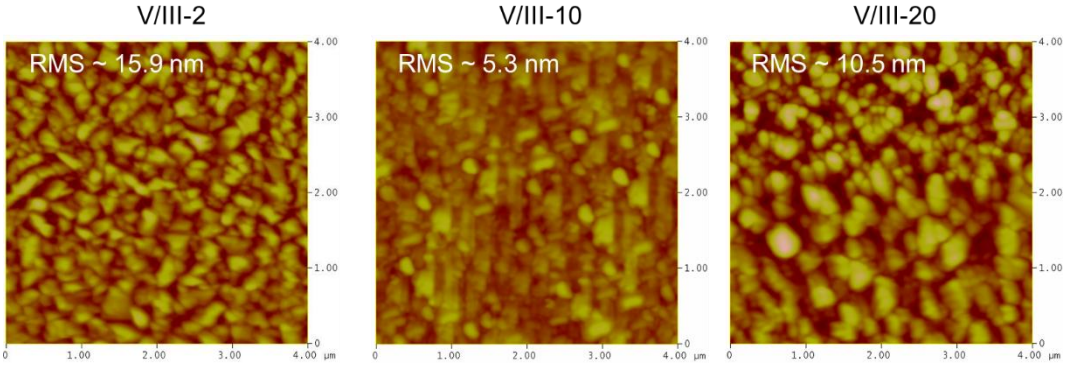

Figure. 2.9 Surface morphology by AFM

The surface morphology of the samples was analyzed using atomic force microscopy (AFM) (Fig. 2.9), and the surface roughness was quantified as root mean square (RMS) values along the [0-11] direction of the GaAs (111) B substrate.

For the double heterostructure samples, the surface roughness was measured to be ~ 16

nm, 5.3 nm, and 10.5 nm for V/III-2, V/III-10, and V/III-20, respectively. These roughness values were dominated by the quality of the low-temperature InAs layer. In comparison, our previous study of the MnAs/InAs/GaAs(111)B structure, where InAs was grown at ~480°C, showed a significantly smoother surface with a roughness of ~0.9 nm. The rougher surfaces observed in the current experiment reflect the influence of the low growth temperature on the InAs layer morphology. Notably, the V/III-10 sample again demonstrated the smoothest surface among the three double heterostructures, reinforcing the conclusion that the V/III ratio of 10 provides superior growth conditions for low-temperature InAs layers.

Magnetization (M) measurements were performed using a superconducting quantum interference device (SQUID) magnetometer to investigate the magnetic characteristics of the double heterostructures at both 4 K and 300 K. For these measurements, a 4 × 4 mm^2 square sample was prepared. Figure 2.10 (a) shows the normalized magnetization as a function of the applied magnetic field (H), measured along the in-plane direction of the hexagonal MnAs at 4 K. In this analysis, the diamagnetic contributions from GaAs and InAs were not subtracted.

The magnetization (M-H) curves for the V/III-10 and V/III-20 samples exhibited two distinct steps, a feature arising from the difference in coercive force (H_C) between the top and bottom MnAs layers. This difference is due to their varying thicknesses and the poorer crystal quality, surface roughness, and interfacial imperfections of the top MnAs layer compared to the bottom layer. The top MnAs layer, with these structural disadvantages, exhibited a larger coercive force. For the V/III-10 sample, the coercive forces for the top and bottom MnAs layers were approximately 800 Oe and 375 Oe, respectively, while for the V/III-20 sample, they were about 695 Oe and 375 Oe. The clear

two-step feature in the M-H curve of the V/III-10 sample more distinctly highlights the effect of thickness differences. Furthermore, the saturation magnetization (M_S) ratio between the top and bottom MnAs layers was approximately 1:4 for both samples, consistent with the expected thickness ratio of these layers in the double heterostructure.

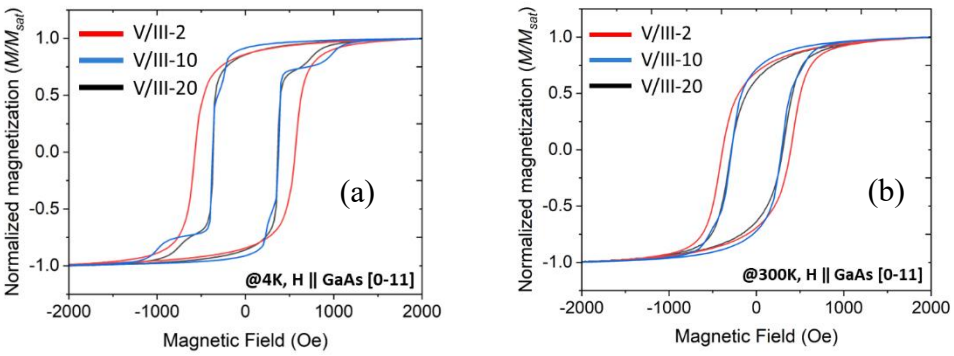

Figure 2.10 Magnetization measurements of DHs at (a) 4 K and (b) 300 K.

In contrast, the V/III-2 sample did not show a distinguishable two-step feature in its M-H curve. This can be attributed to the poor surface and interface quality of both the top and bottom MnAs/InAs interfaces, leading to an indistinguishable difference in coercive force between the two MnAs layers.

Magnetization measurements were also performed at 300 K, as shown in Figure 2.10 (b). At this temperature, all samples demonstrated in-plane easy magnetization, with significantly reduced coercive forces. This behavior is typical of ferromagnetic materials due to the inverse relationship between coercive force and temperature. Consequently, the two-step features observed at 4 K were absent at 300 K. Nevertheless, the persistence of ferromagnetic behavior at room temperature confirms that the magnetic transition temperature (T_C) of MnAs is well above 300 K. This stability underscores the suitability of MnAs layers for applications requiring ferromagnetic properties at elevated temperatures.

Next, we grew the DHs varying the InAs layer thickness as Figure 2.11.

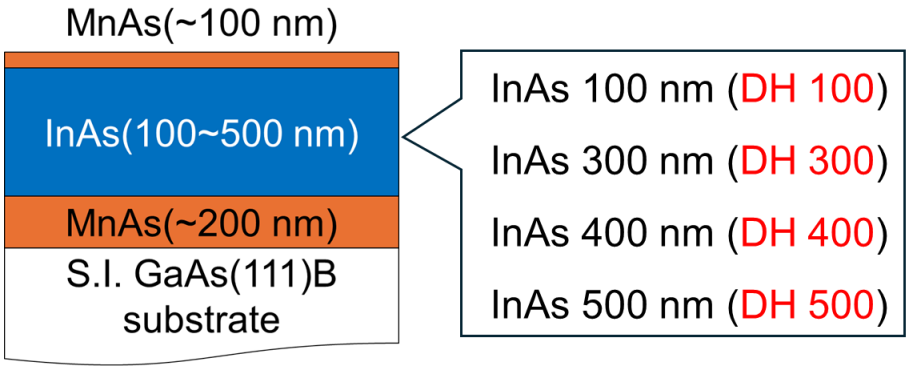

Figure 2.11 Schematic of InAs thickness varying DHs. Thicknesses mentioned are nominal, for proper recognition of the samples.

This time the V/III ratio was kept at ~10 for all the samples. We confirmed the formation of DHs by SEM cross-sectional images showing individual layers and checked the surface roughness in AFM (Figure 2.12).

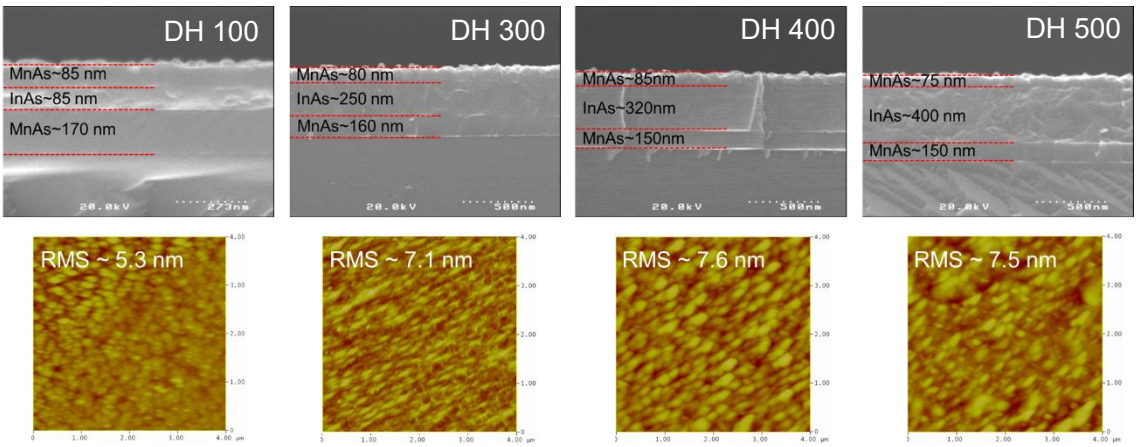

Figure 2.12 SEM cross-section and AFM surface morphology of DHs.

The effect of InAs layer thickness didn't seem to have a significant effect on surface morphology. DH 100 exhibited the smoothest surface with an RMS roughness of 5.3 nm, while DH 300 showed higher roughness at 7.1 nm. The roughness further increased slightly for DH 400 and DH 500, reaching 7.6 nm and 7.5 nm, respectively, indicating

stabilization of surface morphology at larger InAs thicknesses. This suggests that beyond a certain thickness, strain relaxation or improved growth uniformity mitigates further roughness increase. Overall, the surface roughness and structural control highlight the effectiveness of the growth parameters in achieving better-quality DH structures.

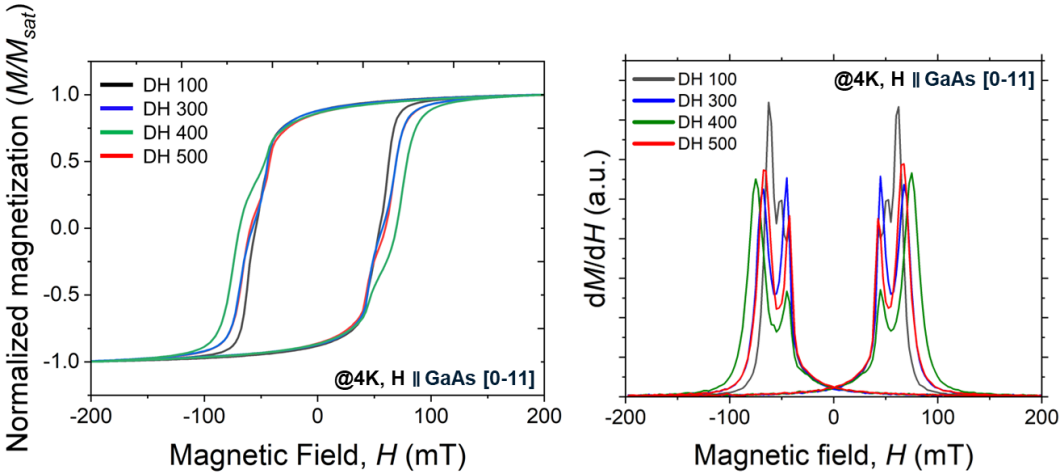

Figure 2.13 Magnetization measurements of the DHs.

The magnetic properties of the InAs double heterostructures (DHs) were measured at 4 K using a SQUID magnetometer with the magnetic field applied parallel to the GaAs [0−11] crystallographic direction (Figure 2.13). The normalized magnetization (M/M_{sat}) vs. magnetic field (H) plots show distinct double-step switching behavior, attributed to the presence of both thick and thin MnAs layers in the DH structure, as described earlier.

The corresponding derivative curves (dM/dH) show sharp and symmetric peaks, particularly for DH 300 and DH 500, indicating well-defined and reproducible magnetic switching processes. These sharper features suggest strong interlayer coupling and stable magnetic behavior. DH 300 and DH 500, in particular, exhibit the most desirable magnetic properties for vertical spin valve (VSV) device fabrication, owing to their clear magnetic switching and stable magnetization steps. These characteristics highlight the potential of these samples for spin valve applications.

Summary

We successfully achieved the low-temperature growth of InAs single layers and MnAs/InAs/MnAs double heterostructures on GaAs (111)B substrates using molecular beam epitaxy (MBE). To identify optimal growth conditions, we systematically varied both the growth temperature and the V/III (As/In) ratio during the InAs deposition. Surface roughness measurements revealed that variations in the V/III ratio significantly influenced the roughness of the single InAs layers and, consequently, the top MnAs layers in the double heterostructures. This highlights the dominant role of InAs roughness in determining the overall surface quality of the heterostructures.

Cross-sectional SEM and EDS analyses confirmed the successful multilayer growth of the double heterostructures and provided precise layer thickness measurements. These analyses also revealed a strong correlation between the V/III ratio and the growth rate of the layers. Furthermore, the interface quality between the top and bottom MnAs layers and the central InAs layer varied with the V/III ratio, with a ratio of 10 yielding the most favorable results.

Magnetization measurements using a SQUID magnetometer showed in-plane easy magnetization for all samples. Differences in coercive fields were observed, attributed to the thickness disparity between the top and bottom MnAs layers and the quality of the MnAs/InAs interfaces. Room-temperature magnetization measurements further confirmed the ferromagnetic behavior of MnAs, demonstrating its stability well above 300 K.

Based on these findings, the V/III ratio of 10 was determined to provide the most optimal conditions for InAs growth. This ratio will be used in subsequent double heterostructure growths aimed at fabricating vertical spin valve devices.

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Chapter 3: Low-temperature grown InAs

3.1 Overview

In the previous chapters, we emphasized the importance of growing InAs at low temperatures for the successful fabrication of MnAs/InAs/MnAs double heterostructures. This approach ensures compatibility with the underlying MnAs layer, which requires lower growth temperatures to preserve its structural and magnetic properties. However, growing InAs below its standard growth temperature introduces challenges, including reduced adatom mobility, incomplete surface coverage, and increased roughness, resulting in defects such as islands or vacancies that compromise the crystalline quality and interface integrity. Additionally, significant lattice mismatch between InAs, MnAs, and GaAs induces residual strain in the InAs layer, which can trigger strain relaxation mechanisms like dislocation generation.

Excess arsenic (As) during growth also plays a critical role, as variations in As beam equivalent pressure (BEP) directly influence defect formation. Studies on LT-GaAs have shown that reduced substrate temperatures result in increased excess As incorporation, forming defects such as arsenic antisites (As_{Ga}) and interstitials (As_i) [1-4]. These defects lead to lattice expansion and enhanced carrier concentration. Similarly, in LT-InAs, which shares the zinc-blende (ZB) structure of GaAs, excess As from varying BEP and/or growth temperature exacerbates point defect formation. Arsenic antisite defects (As_{In}) or interstitial defects for instance, act as donors, introducing extra electrons per defect into the conduction band, thereby increasing n-type carrier concentration.

Furthermore, the MBE growth of GaAs (111) substrates at low temperatures frequently results in twin formation and the emergence of wurtzite (W) structures due to the

structural similarity between ZB (111) and W (0001) surfaces, which differ by a 60° rotation [5]. Such transitions are often observed in GaN growth and lead to defects like pyramidal structures, facets, stacking faults, and rotated twins, adding complexity to the growth process [6]. These issues, combined with the variable effects of As BEP on surface and defect formation, present significant challenges in optimizing LT-InAs growth conditions on GaAs (111).

In this chapter, we focus on the growth of InAs at low temperatures on GaAs (111) B substrates. We explore the potential lattice deformation in the grown layer, examining the underlying causes and their impact on the structural and electrical properties of the material. This includes analyzing factors such as low-temperature growth conditions, lattice mismatch, and strain relaxation mechanisms, and how these influence the overall quality and functionality of the layer.

3.2 MBE growth conditions

We used semi insulating (SI) GaAs (111) B as the substrate. The sample preparation and growth process in MBE has been described in the chapter 2. The growth temperatures were mainly monitored using an infrared pyrometer. In this work, initially we varied the V/III BEP ratio similar to the double heterostructure growth (2, 10 and 20, namely InAs-2, InAs-10 and ImAs-20 respectively) in a constant growth temperature (~235 ºC) and observed the direct effect of excess As. Afterward, the V/III ratio was kept ~10 for the growths while varying the growth temperatures (205, 235, 305 and 480 °C). The thickness of the InAs grown layers for the former part were around 1.2 μm and for the later part of the work, they were around 500 nm, with a growth rate of ~1 μm/hour.

3.3 LT-InAs at varied V/III ratio

The surface roughness of the single InAs layer varied significantly with the V/III ratios, measuring 18 nm, 8 nm, and 12 nm for V/III ratios of 2, 10, and 20, respectively. The low growth temperature contributed to reduced migration energy for In atoms, which in turn led to increased surface roughness [7]. In the case of the InAs-2 sample, the low V/III ratio resulted in an excess of indium compared to arsenic, creating an insufficient supply of As atoms to fully cover the surface during growth. This incomplete coverage caused the formation of surface defects such as adatom islands and vacancies, further increasing the roughness.

Conversely, for the InAs-20 sample, the higher V/III ratio encouraged a higher nucleation density, leading to the formation of numerous islands or nuclei on the surface. As these islands coalesced during growth, the merging process introduced irregularities, resulting in a moderately rough surface. Among the three conditions, the InAs-10 sample exhibited the lowest surface roughness, indicating that this V/III ratio provides more favorable conditions for low-temperature InAs growth, balancing surface coverage and nucleation dynamics effectively.

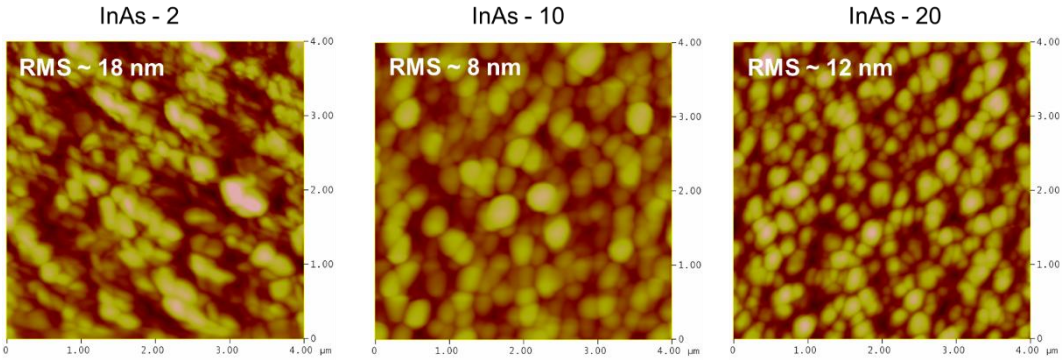

Figure 3.1 AFM surface morphology of LT-InAs at varied V/III ratio.

The electrical transport properties of LT-InAs layers were evaluated using Hall effect measurements via the van der Pauw method at room temperature. Indium electrodes were

directly attached to the samples without annealing, functioning as ohmic contacts. The growth conditions and corresponding electrical properties of the samples with varying V/III ratios are summarized in table 3.1. Despite the absence of intentional n-type doping, all samples exhibited n-type conduction with low resistivities, highlighting the intrinsic electrical characteristics of the InAs layers under the given growth conditions.

Table 3.1 Hall measurement results of LT-InAs

Samples (InAs/GaAs)	As BEP (torr)	In BEP (torr)	Growth temperature (°C)	Thickness (μm)	Mobility (cm^2/V-s)	Carrier conc. (cm^{-3})	Resistivity(ohm-cm)
InAs-2	1.6×10^{-6}	7.6×10^{-7}	~235	1.1	164	1.34×10^{19}	0.0028
InAs-10	7.6×10^{-6}			1.2	381	6.9×10^{18}	0.0024
InAs-20	1.6×10^{-5}			1.23	191	1.92×10^{19}	0.0017

The carrier concentration of all samples was notably high. It is suggested that the electron concentration in low-temperature-grown InAs layers may be influenced by the presence of arsenic-related defects, such as antisite arsenic (As_{In}) or interstitial arsenic (As_i) [8]. At low growth temperatures with excess arsenic, there is a possibility that some indium atoms are replaced by arsenic atoms in the lattice, which may act as double donors [9], contributing to an increase in n-type carrier concentration. For the InAs-20 sample, the high arsenic pressure likely promoted the formation of such defects, leading to a high carrier concentration and reduced mobility.

Interestingly, despite the lower arsenic pressure, the Hall effect measurement for the InAs-2 sample also showed a carrier concentration of a similar order to that of InAs-20. This could be attributed to the poor crystalline quality of the film, as the high surface roughness of the sample (discussed in the next section) may indicate the presence of a high density of structural defects, which could enhance carrier generation. Among the three samples, the InAs-10 sample exhibited significantly improved characteristics in terms of carrier

concentration and mobility. This also suggests that the V/III ratio of 10 provided more favorable conditions for stoichiometric growth and the formation of high-quality InAs epitaxial layers.

With these observations, we now focus on investigating the dependence of growth temperature while maintaining a V/III ratio of 10.

3.4 LT-InAs at varied growth temperature

3.4.1 Surface morphology

The AFM images (Figure 3.2) depict the surface morphology of InAs layers grown on GaAs (111) B substrates at different temperatures, with their corresponding root-mean-square (RMS) roughness values. The analysis reveals a clear trend in surface roughness as the growth temperature increases, providing insights into the impact of temperature on the growth dynamics and surface quality of InAs.

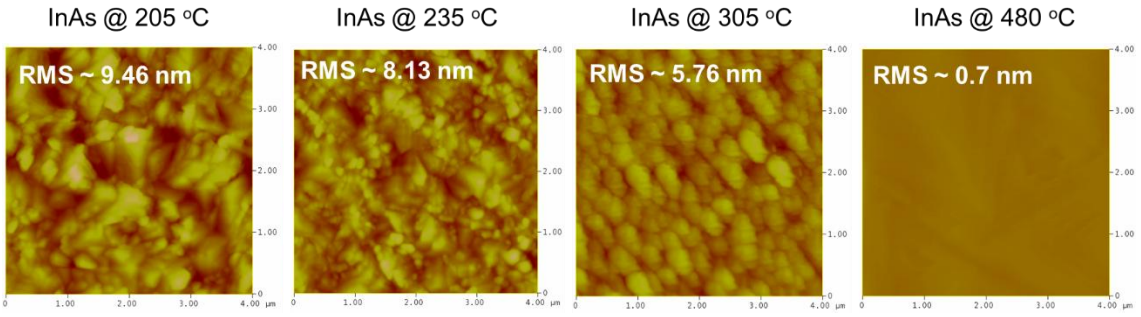

Figure 3.2 AFM surface observation of InAs samples.

The AFM images of InAs grown at lower temperatures (RMS ~9.46 nm and ~8.13 nm) reveal distinct surface features indicative of limited adatom mobility during growth. The surfaces exhibit a granular texture with irregularly shaped and unevenly distributed peaks and valleys, reflecting incomplete coalescence of islands. Clustered islands are prominent, where regions of higher material concentration form peaks, while void-like gaps are

visible between these clusters, suggesting insufficient surface diffusion to fill the gaps. Significant height variations across the surface, as indicated by the high RMS values, further highlight the non-uniform topography. As the growth temperature increases, adatom mobility improves, enabling better surface diffusion and coalescence of islands, which reduces roughness. At the highest temperature, the surface becomes exceptionally smooth (RMS ~0.7 nm), as increased thermal energy promotes efficient adatom migration and strain relaxation, minimizing defects and irregularities.

3.4.2 Lattice deformation due to residual strain

Table 3.2 briefly shows the growth conditions of the samples for temperature variable InAs growths. InAs crystallizes in the zinc-blende (ZB) structure, which is a cubic crystal system, with a lattice parameter of a ~ 6.0583 Å (assuming full relaxation) [10]. We performed XRD 2θ scanning to find out the lattice parameters of the InAs samples.

Table 3.2 Growth conditions of the samples.

Samples	Growth temperature (°C)	In BEP (Torr)	As BEP (Torr)	Thickness (nm)	InAs lattice constant (Å)
InAs/GaAs (111) B	~205	7.6×10^{-7}	7.6×10^{-6}	465	6.083
	~235			480	6.078
	~305			530	6.070
	~480			965	6.062

We observed a clear shift of the XRD peaks for InAs to the lower angle (2θ) region with decreasing growth temperature (Figure 3.3). This indicates an increase in the lattice parameter (a) of ZB InAs.

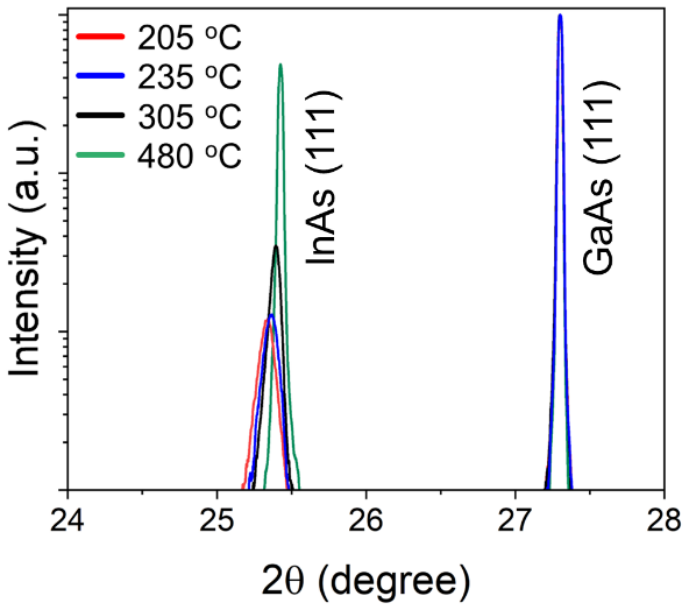

Figure 3.3 XRD peaks of InAs/GaAs (111) B obtained by 2θ-scanning.

We calculated the lattice parameters to be 6.083, 6.078, 6.07 and 6.062 Å for InAs which were grown at 205, 235, 305 and 480 °C respectively. InAs growth on GaAs is lattice mismatched (~ 7.2 %). It creates a significant compressive strain in the InAs layer when grown on a GaAs substrate. This compressive strain arises as the InAs lattice attempts to conform to the smaller lattice constant of GaAs, causing in-plane compression and out-of-plane expansion. The lattice distortion induced by this mismatch leads to strain relaxation mechanisms, such as lattice expansion in the out-of-plane direction (along the growth axis), to compensate for the in-plane compressive stress. At lower growth temperatures, the reduced atomic mobility limits the ability of the layer to fully relax through dislocation formation or other mechanisms, thereby maintaining a higher degree of residual strain. As a result, the observed lattice parameters of InAs layers grown at low temperatures are slightly larger than their bulk value, reflecting the effect of strain induced by the lattice mismatch.

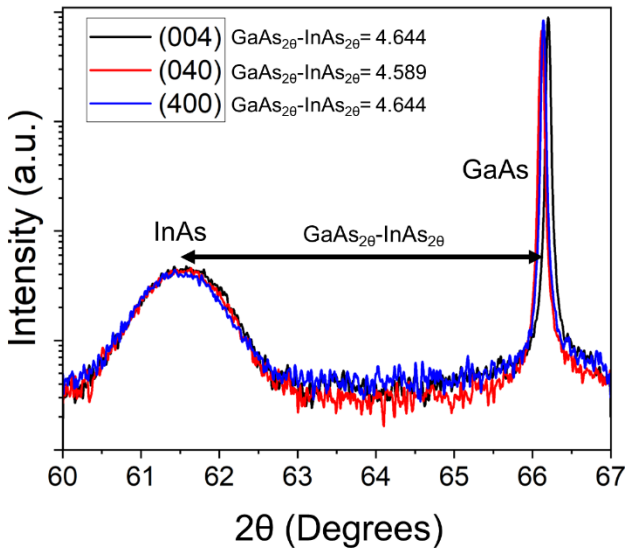

Figure 3.4 {400} asymmetric XRD scan of InAs grown at 205 °C.

To confirm the lattice deformation through strain, we performed {400} planes asymmetric XRD measurements of LT-InAs grown at 205 °C (Figure 3.4). We found a significant difference in the peak distance between InAs and GaAs than that of literature values. InAs {004} and GaAs {004} peak positions (2θ) are 61.146° and 66.058° respectively (considering full relaxation), making the distance about 4.912°. From figure 3.4 it is evident that in LT-InAs the distance is lower, implying in-plane shrinkage of the lattice. Figure 3.5 shows a simple illustration of the deformation mechanism in this situation.

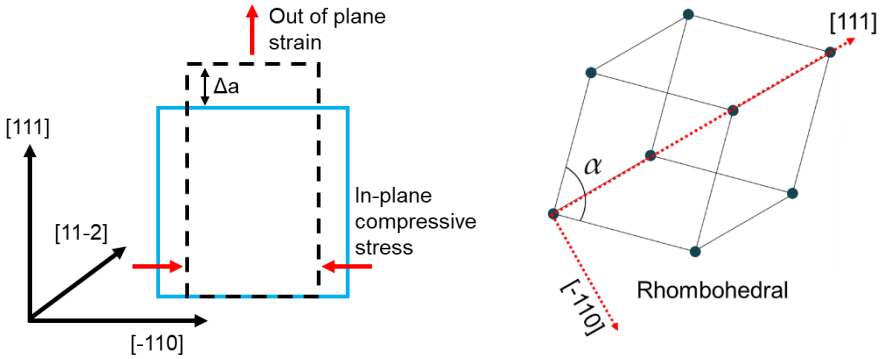

Figure 3.5 Deformation mechanism in LT-InAs.

Due to the lattice mismatch, InAs grown on GaAs (111) B experiences compressive stress along in-plane direction (for instance [-110], [11-2] and so on). Considering elastic deformation of the lattice, it elongates along out of plan [111] direction (i.e. growth direction). The anisotropic nature of this strain alters the symmetry of the lattice. Specifically, the uniform cubic symmetry of the zinc-blende structure is broken due to the differential stresses along the in-plane and out-of-plane axes. This transformation leads to the distortion of the lattice into a rhombohedral structure, characterized by a slight deviation from the 90° angle between lattice vectors. Such a transformation from cubic to rhombohedral symmetry reflects the material's response to strain under elastic deformation, where the lattice adjusts to minimize strain energy. The degree of this rhombohedral distortion depends on the magnitude of the strain, which is governed, in our case, mainly by growth conditions.

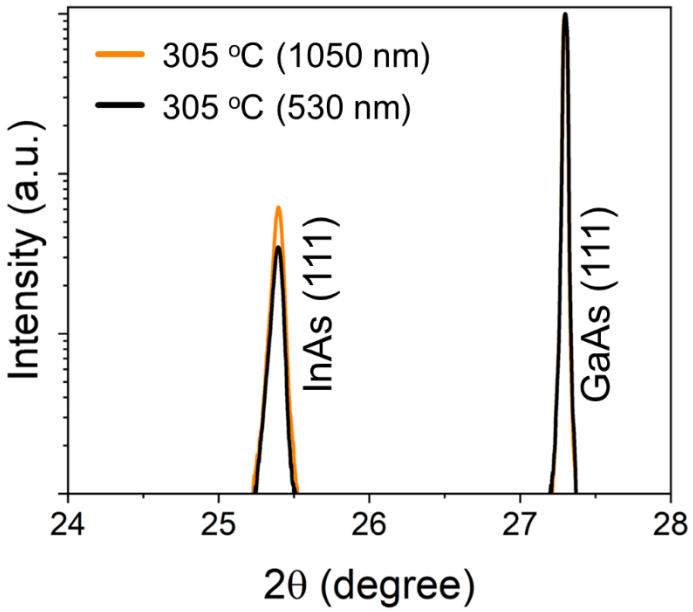

Figure 3.6 Effect of layer thickness on strain.

To evaluate the effect of layer thickness on the strain in low-temperature-grown (LT) InAs, we conducted XRD 2θ scans for samples grown at 305 °C with two different thicknesses

of approximately 530 nm and 1.05 μm (Figure 3.6). The results revealed a negligible peak shift between the two samples, indicating that the strain state in the LT-InAs layer does not significantly depend on thickness beyond a certain limit.

This behavior can be explained by the strain relaxation mechanism in lattice-mismatched heterostructures. Initially, when the InAs layer begins to grow on the GaAs (111) B substrate, the lattice mismatch induces compressive strain in the InAs layer. However, as the layer grows thicker, the strain energy accumulates and reaches a critical point where strain relaxation occurs through the formation of dislocations or other strain-relief mechanisms. Once these mechanisms are activated, further growth does not result in additional strain accumulation, leading to a saturation of the strain state in the layer.

3.4.3 Lattice deformation due to defects: Effect on electrical properties

Although it is evident that the lattice distortion is primarily driven by residual strain resulting from the lattice mismatch between InAs and GaAs, there may be additional contributing factors. These could include the incorporation of point defects such as antisite arsenic (As_{In}) or interstitial arsenic (As_i), which can locally distort the lattice. Furthermore, the low-temperature growth conditions may lead to reduced adatom mobility, resulting in incomplete strain relaxation and enhanced defect density. From here, we discuss these possibilities.

Figure 3.7 shows a relationship between growth temperature and lattice expansion. We compared our results with the results of LT-GaAs grown on GaAs (001) substrate by X. Liu *et al* [11]. We can observe the trend of lattice expansion for InAs similar to that of LT-GaAs, due to lower growth temperatures.

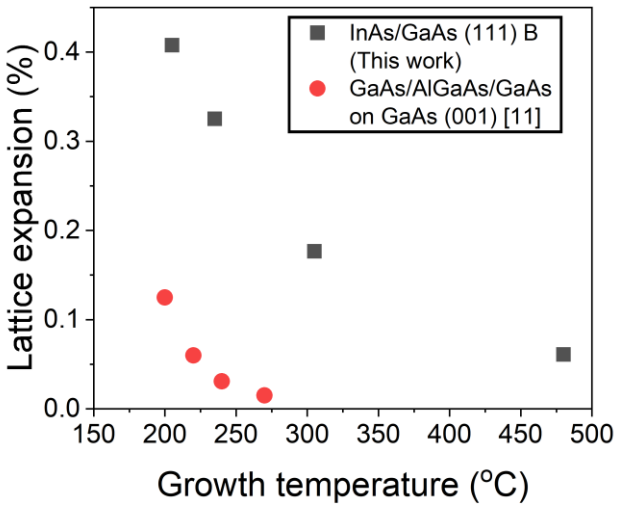

Figure 3.7 Growth temperature versus corresponding lattice expansion. Black squares represent data from this work and red circles are data from reference [11].

It is well known that reduction in growth temperature increases the concentration of excess As. The excess As may cause the interstitial As defects and the lattice spacing and expansion can be attributed to it [12]. Formation of antisite As defects is well established for LT-GaAs, and it can also be the reason of lattice expansion for LT-InAs. Both the lattice parameter and the antisite As concentration rise with decreasing growth temperature. As has a smaller atomic radius than In, yet the lattice distortion that results from replacing In with As can cause the lattice to expand. According to experimental estimates, the interatomic distance between As_{Ga}-As in LT-GaAs is 2.65 Å [11], which is substantially more than the interatomic distance between Ga-As (2.45 Å). Following the similar manner, M. Takushima *et al.* [13] calculated the As_{In}-As interatomic distance to be 2.66 Å , which is greater than the In-As interatomic distance (2.62 Å). It is also claimed by them that the atomic radius of As on the regular sites is 1.18 Å, whereas it is about 1.47 Å for As on the antisites. The As atoms closest to an As_{In} defect are expected to be

moved from their normal positions due to the larger As_{In}-As bond in LT-InAs. Considering these facts, it won't be unreasonable to assert that LT-InAs has a significant amount of As_{In} defects in it and that this leads to lattice expansion.

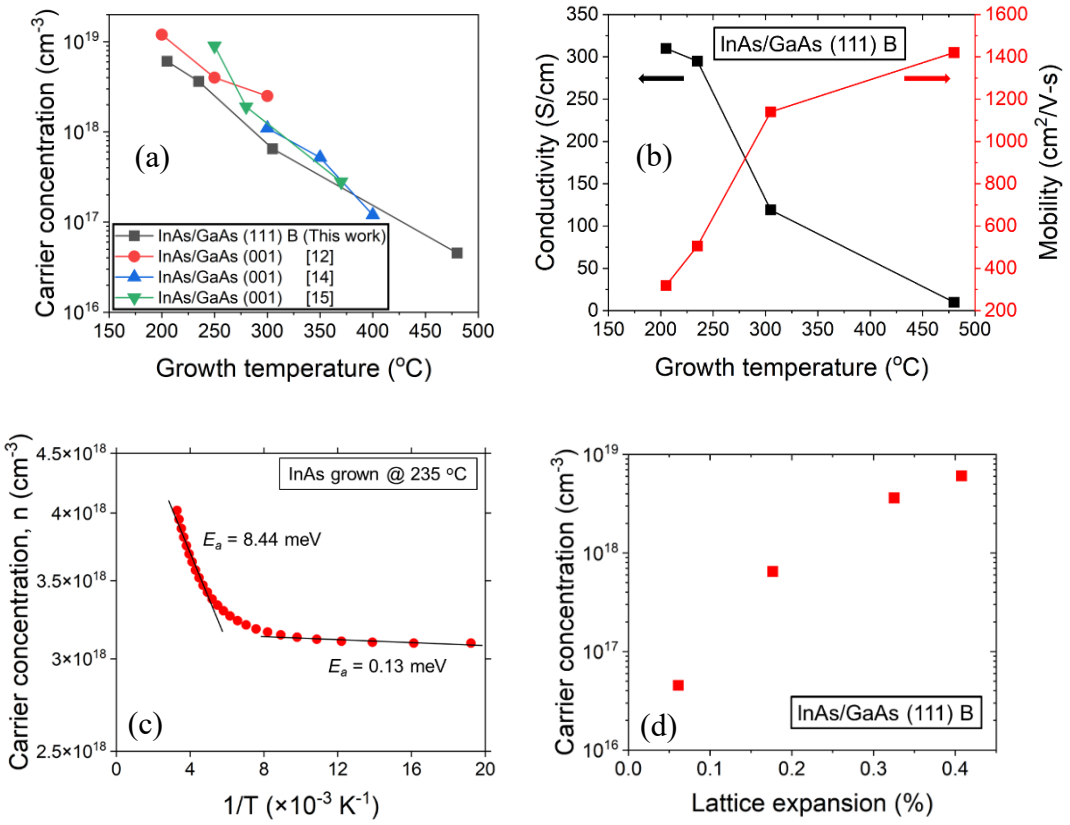

Figure 3.8 (a) Growth temperature vs. carrier concentration, (b) Growth temperature vs. conductivity and mobility (c) activation energy of the donors in LT-InAs and (d) lattice expansion vs. carrier concentration.

The carrier concentration of InAs exhibited a rise when the growth temperature decreased, as shown in Figure 3.8 (a). We conducted a comparative analysis of our research with the studies conducted by M. Shiba et al. [12], M. Yano et al. [14], and D.I. Westwood et al.

[15]. These studies also focused on similar work but utilized GaAs (001) as the substrate material. The InAs/GaAs (111) B structure has a comparable trend to that of InAs/GaAs (001), with a nearly comparable order of carrier concentration. All LT-InAs/GaAs (111) B samples had n-type conduction with significant conductivity (Figure 3.8 b), even though they were not intentionally doped. The high conductivities are similar to those observed in n-doped poly-InAs [16].

The higher carrier concentration observed in LT-InAs, as shown in Figure 3.8 (a), can be primarily attributed to the presence of excess arsenic in the form of As_{In} and As_i defects [8, 12], which are prevalent under low-temperature growth conditions [13]. These defects act as donor-like states within the InAs crystal lattice, contributing significantly to the free electron concentration. The formation of As_{In} occurs when arsenic atoms occupy indium sites, while As_i atoms occupy non-lattice positions. Both defect types introduce additional energy levels close to the conduction band, increasing the number of free carriers. As_{In} acts as a deep level donor (EL2, E_c-0.75 eV) in case of GaAs, but in case of InAs, it's rather shallow donor (E_c-10 to 110 meV) [17].

Figure 3.8 (c) shows the activation energy (E_a) of the donors, extracted from temperature variable Hall measurement. This plot represents the temperature dependence of the carrier concentration (*n*) in low-temperature-grown (LT) InAs. The natural logarithm of carrier concentration *ln(n)* is plotted against the inverse of temperature (1/T), revealing two distinct activation energy regions characterized by different slopes: Ea = 8.44 meV (E_c-8.44 meV) at higher temperatures and 0.13 meV (E_c-0.13 meV) at lower temperatures. It is quite evident that the excess carrier concentration is not due to intrinsic excitation, but because of almost fully ionized donors. The transition between the two activation energy regions indicates a shift in the dominant carrier generation mechanism. At higher

temperatures, the excitation of electrons from the deeper shallow donor states (likely As_{In}) dominates, while at lower temperatures, carriers from extremely shallow or nearly degenerate defect states (possibly As_i) maintain the conduction band population. These findings highlight the critical role of arsenic-related point defects in affecting the electrical properties of LT-InAs.

Figure 3.8 (d) shows a relationship between lattice expansion and carrier concentration for InAs grown on GaAs (111) B, which is indicative of the presence of substantial amount of point defects and their contribution to the electrical properties of LT-InAs.

The structural quality of the InAs films grown at varying temperatures was evaluated using XRD omega (ω) scans of the (111) reflection (Figure 3.9 a). The full width at half maximum (FWHM) of the ω-scans were measured to be 0.317°, 0.307°, and 0.096° for films grown at 205 °C, 305 °C, and 480 °C, respectively. It represents a gradual improvement in the c-axis deviation with increasing growth temperature. The peak positions are almost at zero, indicating negligible tilting of InAs layer to GaAs substrate [18].

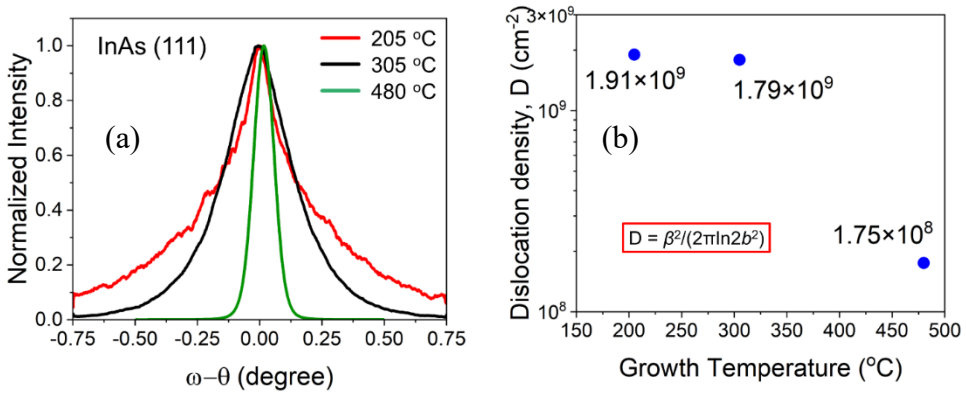

Figure 3.10 (a) XRD omega scan of InAs and (b) calculated threading dislocation density from peak broadening.

The observed trend of decreasing FWHM with increasing growth temperature suggests a significant enhancement in crystalline quality as the temperature rises. The FWHM is directly correlated with the degree of mosaicity, dislocation density, and strain in the crystal; broader peaks (higher FWHM values) are indicative of greater structural imperfections.

For the sample grown at 205 °C, the InAs film showed the widest diffraction peak with a FWHM of 0.317°. This suggests that lower growth temperatures lead to films with greater defect density and more noticeable strain. With an increase in the growth temperature to 305 °C, the FWHM fell to 0.307°, indicating an enhancement in the quality of the crystal structure. This improvement is likely attributed to the increased mobility of adatoms and reduced presence of defects during the development process. The film grown at a temperature of 480 °C exhibited the narrowest diffraction peak (FWHM = 0.096°), suggesting superior crystalline quality with minor structural imperfections. The significant decrease in peak broadening observed at higher temperatures can be attributed to the enhanced surface diffusion of adatoms, resulting in a more ordered growth of crystals and a consequent decrease in the density of dislocations and strain.

We roughly estimated the threading dislocation densities [19] from the peak broadening (Figure 3.9 b). In the equation D, β and b are dislocation density (in cm^{-2}), peak broadening (in radian) and length of Burgers vector (in cm) respectively. Increasing the growth temperature of InAs films significantly reduces threading dislocation density. This reduction in dislocation density highlights the critical role of elevated temperatures in enhancing film quality and structural integrity of InAs. Threading dislocations, which are line defects that traverse the crystal, can have a substantial influence on the electrical characteristics of LT-InAs films. These dislocations function as points where charge

carriers are scattered, leading to a decrease in carrier mobility as they divert from their intended routes while moving through the material. The scattering effect is especially detrimental in low-temperature-grown InAs, as the material is already susceptible to defect formation. The poor mobility of LT-InAs (Figure 3.8 b) may be attributed to this factor. In addition to line defects, planar defects, such as twin boundaries, may also have implications in this matter.

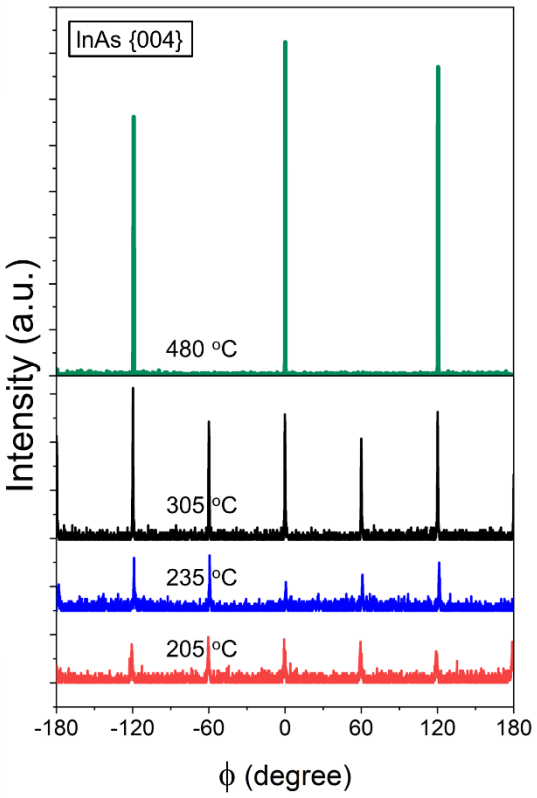

Figure 3.10 In-plane φ-scanning of InAs {004} shows unusual 6-fold rotational symmetry for LT-InAs samples.

Talking about planar defects, we also carried out in-plane phi (φ) scanning of InAs {004} planes as shown in Figure 3.10. An unusual 6-fold rotational symmetry was observed for LT-InAs (205, 235, and 305 °C), as opposed to the typical 3-fold symmetry seen in usual growth temperature InAs (e.g. 480 °C), suggests the presence of 60° rotated twin

boundaries within the crystal structure [5]. The GaAs (111) B substrate imposes a threefold rotational symmetry on the overgrown InAs film due to its crystallographic orientation. This symmetry is transferred to the InAs layer during epitaxial growth, typically resulting in 3-fold symmetry in the XRD phi scan due to its three equivalent {004} planes, which are 120° apart in a perfect crystal. Low temperature growth of InAs on the GaAs (111) B substrate is prone to generating planar defects such as stacking faults, leading to the formation of 60° twins. These twins result from the lattice mismatch and the particular strain conditions present at the InAs/GaAs (111) interface. When a twin forms, the crystal lattice within the twinned region rotates by 60° around the [111] axis relative to the untwined region (Figure 3.11).

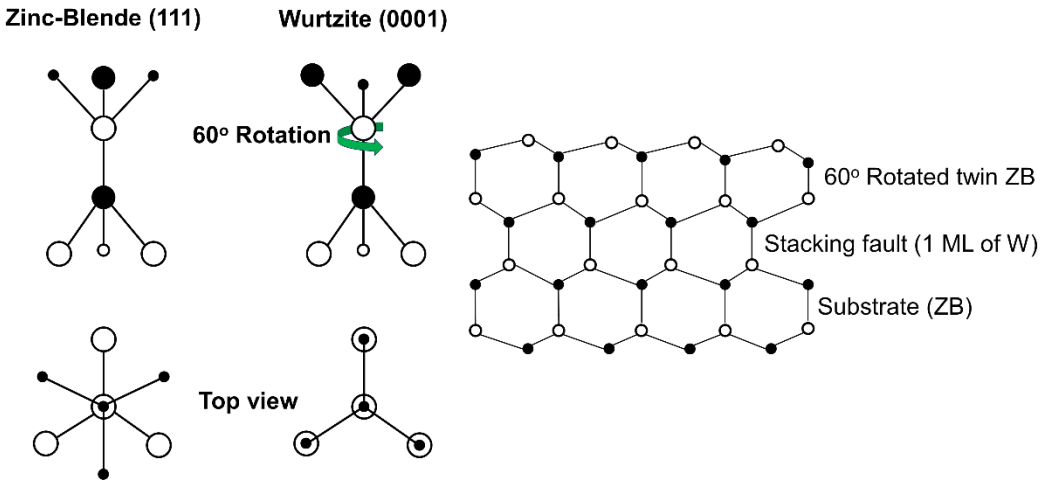

Figure 3.11 Formation of 60° rotated twin defects in zinc-blende structure.

During an XRD phi (φ) scan, the X-ray beam diffracts from the {004} planes of InAs. Due to the 60° rotation caused by twinning, additional diffraction peaks appear at intervals of 60 degrees. This doubling of peaks creates the observed 6-fold rotational symmetry, which directly indicates the presence of twin defects in the LT-InAs layer. The presence

of twinning in LT-InAs not only impacts its structural characteristics but also may have significant consequences for its electrical properties. Twin boundaries can serve as scattering sites for charge carriers, which may lead to a decrease in carrier mobility, as mentioned earlier. The identification of 60º twinning offers a vital understanding of the microstructural features of LT-InAs, highlighting the influence of growing conditions on the crystallographic and electrical properties of the material.

Summary

In this chapter we discussed the growth of low-temperature InAs (LT-InAs) on GaAs (111)B substrates using molecular beam epitaxy (MBE), focusing on the impact of growth conditions, including temperature and V/III ratio, on structural, morphological, and electrical properties. AFM analysis revealed a significant reduction in surface roughness with increasing growth temperature, where low temperatures resulted in granular structures, clustered islands, and voids due to limited adatom mobility. XRD analysis demonstrated lattice expansion from in-plane compressive stress caused by the lattice mismatch, leading to out-of-plane elongation along the [111] direction and transforming the zinc-blende cubic lattice into rhombohedral symmetry. Arsenic-related defects, such as arsenic antisites and interstitial arsenic, were estimated as key contributors to lattice distortion and enhanced n-type carrier concentration, with their prevalence more pronounced at lower growth temperatures. Electrical measurements confirmed high carrier concentrations, shallow donor levels, and the influence of defect density on mobility and resistivity. We underscored the importance of optimizing growth parameters, such as a V/III ratio of 10 and moderate growth temperatures, to improve stoichiometry, surface quality, and electrical performance.

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Chapter 4: Vertical spin valve device using MnAs/InAs/MnAs double heterostructure

4.1 Overview

Vertical spin valve devices (VSVs) have garnered significant attention in spintronics due to their ability to enable efficient spin injection and detection across stacked heterostructures.

spin valves incorporating MnAs and III-V semiconductor systems. M. Tanaka et al. investigated MnAs/III-V/MnAs magnetic tunnel junctions grown on GaAs (111) B, demonstrating a tri-layer structure with thin ferromagnetic layers and a III-As spacer, revealing its potential for tunneling magnetoresistance applications [1]. M. E. Islam et al. studied non-local lateral spin-valve transport in MnAs/InAs systems on GaAs (111) B, emphasizing the role of a thick (~1200 nm) InAs channel in spin injection and detection [2]. Additionally, works by D. Saha et al. [3], H. Kum et al. [4], and R. Adari et al. [5] explored non-local spin-valve effects in MnAs/n-GaAs and MnAs/InAs heterostructures on GaAs (001). These studies reported varying channel thicknesses (~150–200 nm) and multilayer designs, highlighting spin transport characteristics under different configurations. But there is no report on vertical spin valve fabrication and measurement using MnAs/thick-InAs/MnAs tri-layer system.

In this chapter, we will discuss vertical spin valve device fabrication using MnAs/InAs/MnAs double heterostructure on GaAs (111) B and its measurement results. We used DH 500 (described in section 2.2.3) sample for VSV fabrication and measurements.

4.2 Vertical spin valve (VSV) fabrication

We utilized a combination of advanced fabrication techniques to achieve high-quality and precise nanostructures for our device. Electron beam lithography (EBL) was employed to define nano-posts at the nanoscale with high resolution, followed by Argon-ion etching, which allowed for the controlled removal of material to create well-defined patterns. These methods are critical for achieving the desired structural features with nanoscale precision.

We used Hydrogen Silsesquioxane (HSQ) coating to separate the electrodes and the contact pads. The low-k insulator (HSQ) layer was then etched at certain positions on the top of electrodes to deposit the access contact pads. The etching was performed using a reactive-ion etching system, a technique that provides anisotropic etching with precise depth control, ensuring clean and uniform features necessary for reliable device insulation. For the fabrication of markers and contact pads, electron cyclotron resonance (ECR) sputtering was used for material (Au) deposition, ensuring uniform thin films with good adhesion and electrical properties. The patterning was done by photolithography, a widely used technique for patterning larger areas with high accuracy and throughput.

To establish electrical connections with the vertical spin valve (VSV), we employed high-precision dicing machines for cutting, followed by wet-bonding equipment to connect wires securely. Figure 4.1 briefly illustrates the VSV fabrication steps.

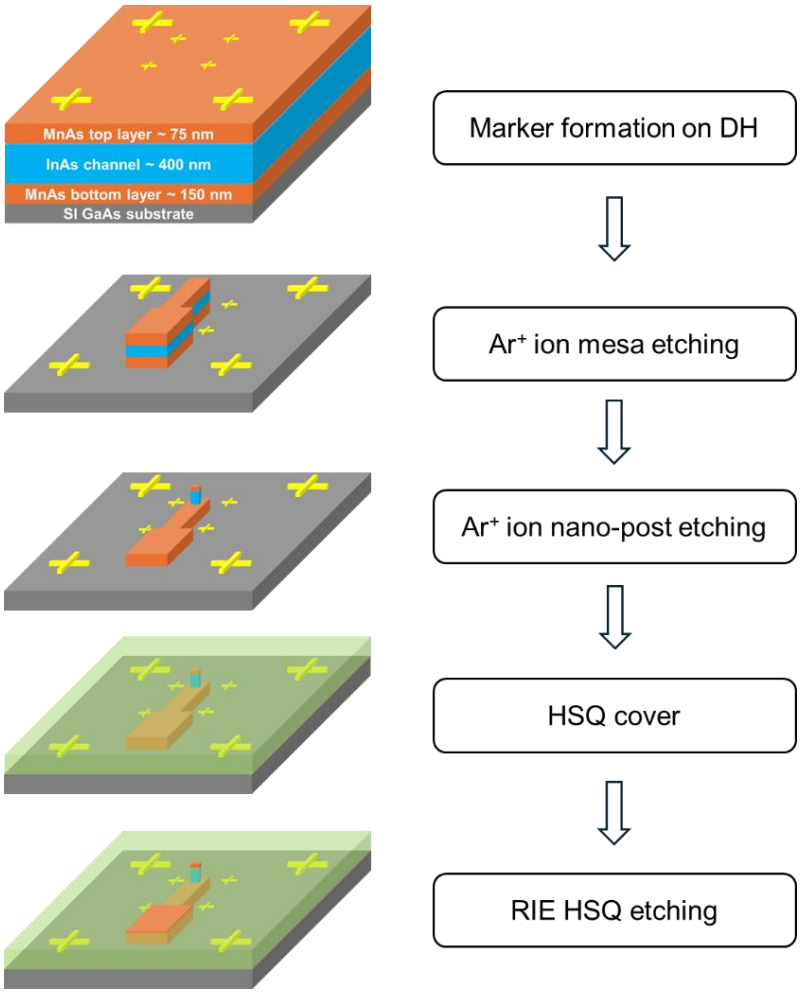


Figure 4.1 Flow-chart of VSV device fabrication.

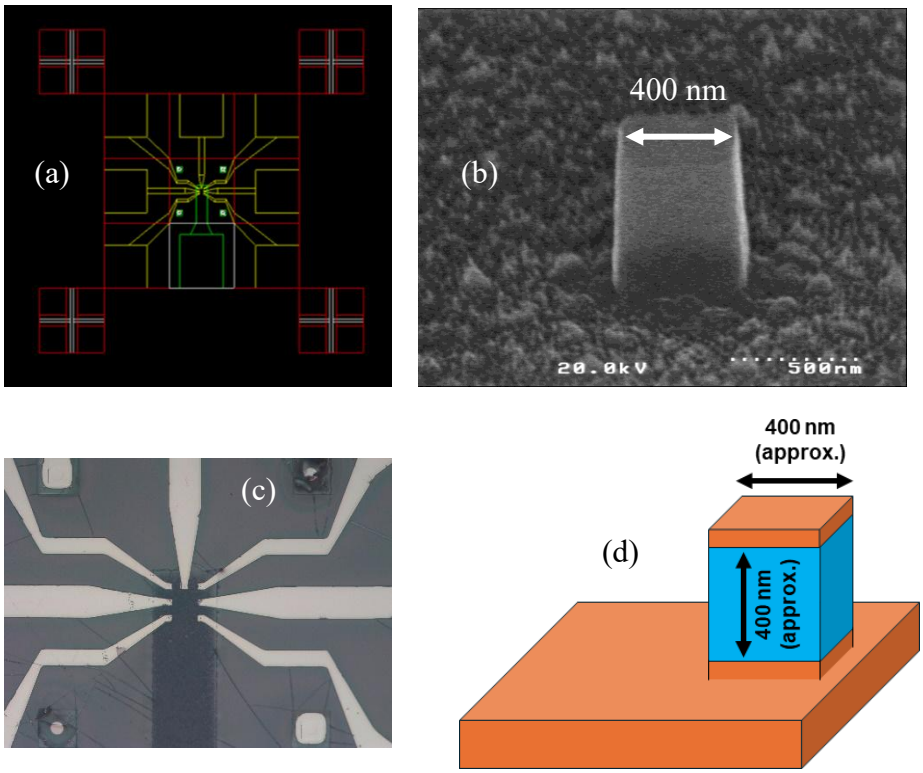


Figure 4.2 (a) Pattern design for electron beam lithography, (b) SEM image of the nano-post, (c) Optical microscopic image of the post-fabrication devices and (d) simple illustration of the fabricated VSV.

The diameter of the fabricated nano-post is about 400 nm. The detail of the fabrication method is described in Table 4.1. We confirmed the electrical transportation through source and drain by I-V measurements. Afterward, we measured the spin valve measurement in a superconducting magnet system.

Table 4.1 VSV device fabrication process details.

1. Marker formation		
Process	Action and condition	Comments
Cleaning	Acetone dipping (5 min) Methanol dipping (5 min) DIW dipping (5 min) N2 blowing Ashing (O_2, 25 Pa, 30 W, 10 sec) Semico-clean dipping (1 min) DIW dipping (5 min) N_2 blowing	
Baking	Hot-plate (110 ºC, 3 min)	
LOL2000 coat	N_2 blowing LOL2000 dropping 500 rpm, 3 sec Slope 2 sec 3000 rpm, 60 sec, Slope 2 sec Hot-plate (180 ºC, 3 min)	
ZEP520 coat	N_2 blowing ZEP520A7 dropping 500 rpm 5 sec Slope 2 sec 4000 rpm 60 sec Slope 2 sec Hot-plate (180 ◦ C, 3min)	
EB Lithography	Exposure (50 pA, 4.4 μs, 600 μm)	
Development	ZED-N50 (60 sec) ZMD-B (30 sec) N_2 blowing	

	NMD-W developer dipping (12 sec) DIW dipping (1 min) N_2 blowing	
Descum	Ashing (O_2, 25 Pa, 10 W, 30 sec) Semico-clean dipping (1 min) DIW dipping (1 min) N_2 blowing	25 nm
Sputtering	Vacuum pressure (10^{-4} Pa) Au (2 nm/sec, 50 min)	100 nm
Lift-off	1165 dipping on hot-plate (60 ºC) Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	30 min
2. Source fabrication		
Cleaning	Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	
Baking	Hot-plate (110 ºC, 3 min)	
OAP coat	N_2 blowing OAP 2000 dropping 500 rpm 3 sec Slope 2 sec 3000 rpm 60 sec Slope 2 sec Hot-plate (180 ºC, 3 min)	
SAL-601H-SR7	N_2 blowing SAL-601H-SR7 dropping 500 rpm 5 sec Slope 2 sec	

	4000 rpm 60 sec Slope 2 sec Hot-plate (110 ^{o}C, 2 min)	
EB Lithography	Exposure (50 pA, 0.2 μs, 600 μm)	
Post exposure baking (PEB)	Hot-plate (100 ^{o}C, 5 min)	
Development	NMD-W developer dipping (5 min) DIW dipping (7 min) N_2 blowing	
Ar^+ etching	ECR (Ar: 0.5 kV, 100 W, 3 min)	100 nm
Resist removal	1165 dipping in 60 ^{o}C (30 min) Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	
3. Nano-post fabrication		
Cleaning	Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	
Baking	Hot-plate (110 ^{o}C, 3 min)	
OAP coat	N_2 blowing OAP 2000 dropping 500 rpm 3 sec Slope 2 sec 3000 rpm 60 sec Slope 2 sec Hot-plate (180 ^{o}C, 3 min)	
SAL-601H-SR7	N_2 blowing SAL-601H-SR7 dropping 500 rpm 5 sec Slope 2 sec	

	4000 rpm 60 sec Slope 2 sec Hot-plate (110 ºC, 2 min)	
EB Lithography	Exposure (50 pA, 2.2 μs, 600 μm)	
PEB	Hot-plate (100 ºC, 5 min)	
Development	NMD-W developer dipping (5 min) DIW dipping (7 min) N_2 blowing	
Ar^+ etching	ECR (Ar: 0.5 kV, 100 W, 8 min)	450 nm
Resist removal	1165 dipping in 60 ºC (30 min) Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	
4. HSQ deposition		
Cleaning	Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	
Baking	Hot-plate (110 ºC, 3 min)	
HSQ coat	N_2 blowing HSQ dropping 300 rpm 5 sec 3000 rpm 60 sec Slope 2sec Hot-plate (110 ºC, 3 min) N_2 blowing HSQ dropping 300 rpm 5 sec 3000 rpm 60 sec Slope 2 sec Hot-plate (110 ◦ C, 3min) Hot-plate (300 ◦ C, 10min)	600 nm

LOL2000 coat	N_2 blowing LOL2000 dropping 500 rpm, 3 sec Slope 2 sec 3000 rpm, 60 sec, Slope 2 sec Hot-plate (180 ºC, 3 min)	
ZEP520 coat	N_2 blowing ZEP520A7 dropping 500 rpm 5 sec Slope 2 sec 4000 rpm 60 sec Slope 2 sec Hot-plate (180 ºC, 3 min)	
EB Lithography	Exposure (100 pA, 2.2 μs, 600 μm)	
Development	ZED-N50 (60 sec) ZMD-B (30 sec) N_2 blowing NMD-W developer dipping (12 sec) DIW dipping (1 min) N_2 blowing	
CHF_3 etching	20 sccm, 2.0 Pa, 50 W (7 min)	140 nm
Resist removal	1165 dipping in 60 ºC (30 min) Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	Exposed area for access electrodes (drain).
LOL2000 coat	N_2 blowing LOL2000 dropping 500 rpm, 3 sec Slope 2 sec 3000 rpm, 60 sec,	

	Slope 2 sec Hot-plate (180 ºC, 3 min)	
TSMR coat	N_2 blow TSMR dropping 500 rpm 5 sec Slope 2 sec 4000 rpm 60 sec Slope 2 sec Hot-plate (110 ºC, 2 min)	
Photolithography	Exposure (180 mJ/cm^{-2})	
Development	NMD-W developer dipping (1 min) DIW dipping (1 min) N_2 blowing	
CHF_3 etching	20 sccm, 2.0 Pa, 50 W (30 min)	600 nm
Resist removal	1165 dipping in 60 ºC (30 min) Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	Exposed area for access electrodes (source).
5. Electrodes deposition		
Cleaning	Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	
Baking	Hot-plate (110 ºC, 3 min)	
LOL2000 coat	N_2 blowing LOL2000 dropping 500 rpm, 3 sec Slope 2 sec 3000 rpm, 60 sec, Slope 2 sec	

	Hot-plate (180 ºC, 3 min)	
TSMR coat	N_2 blow TSMR dropping 500 rpm 5 sec Slope 2 sec 4000 rpm 60 sec Slope 2 sec Hot-plate (110 ºC, 2 min)	
Photolithography	Exposure (180 mJ/cm^{-2})	
Development	NMD-W developer dipping (1 min) DIW dipping (1 min) N_2 blowing	
Sputtering	Vacuum pressure (10^{-4} Pa) Au (2 nm/sec, 50 min)	100 nm
Lift-off	1165 dipping on hot-plate (60 ºC) Acetone dipping (3 min) Methanol dipping (3 min) DIW dipping (3 min) N_2 blowing	

4.3 VSV measurement: Low temperature measurement system

In this study, spin valve measurements were conducted in a low-temperature environment of approximately 95 K to a higher temperature of 240 K, using He cryostat, as illustrated in Figure 4.3. The system features a superconducting magnet (SCM) housed within a dewar, capable of applying magnetic fields up to ±8 Tesla. The sample is positioned within a variable temperature insert (VTI) unit, which is connected to the helium dewar through a needle pipe. The flow of helium into the VTI is precisely regulated using a needle valve to maintain temperature stability.

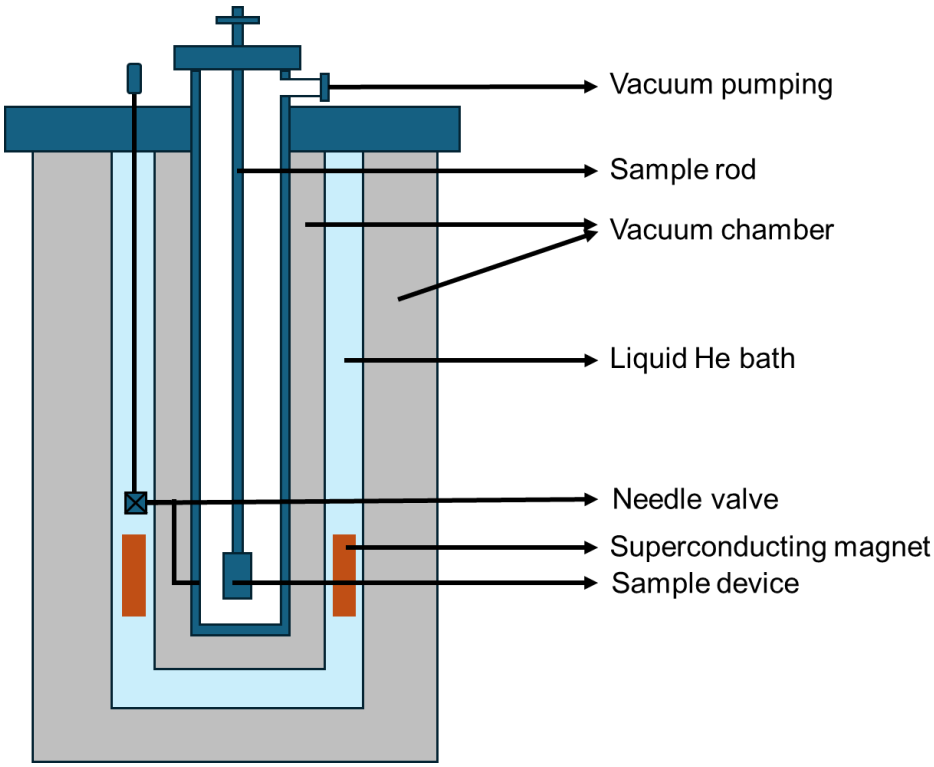


Figure 4.3 Low temperature measurement configuration.

The liquefaction temperature of helium at atmospheric pressure is approximately 4.2 K. However, by reducing the pressure through evacuation, the boiling point is further

lowered to about 1.5 K, creating the ultra-low-temperature environment. This setup ensures a highly controlled thermal and magnetic environment, enabling accurate and reproducible spin valve characterization at low temperatures. The combination of the SCM and the VTI provides flexibility in both temperature and magnetic field control.

The measurement setup, shown in Figure 4.4, is designed to maintain precise and stable current flow through the device and facilitate accurate signal detection. A 1 MΩ resistor and a standard 10 kΩ resistor are connected in series to achieve this. The 1 MΩ resistor serves to stabilize the current flow, while the voltage drop across the 10 kΩ resistor is used to monitor and measure the current, ensuring consistency and precision during the experiment.

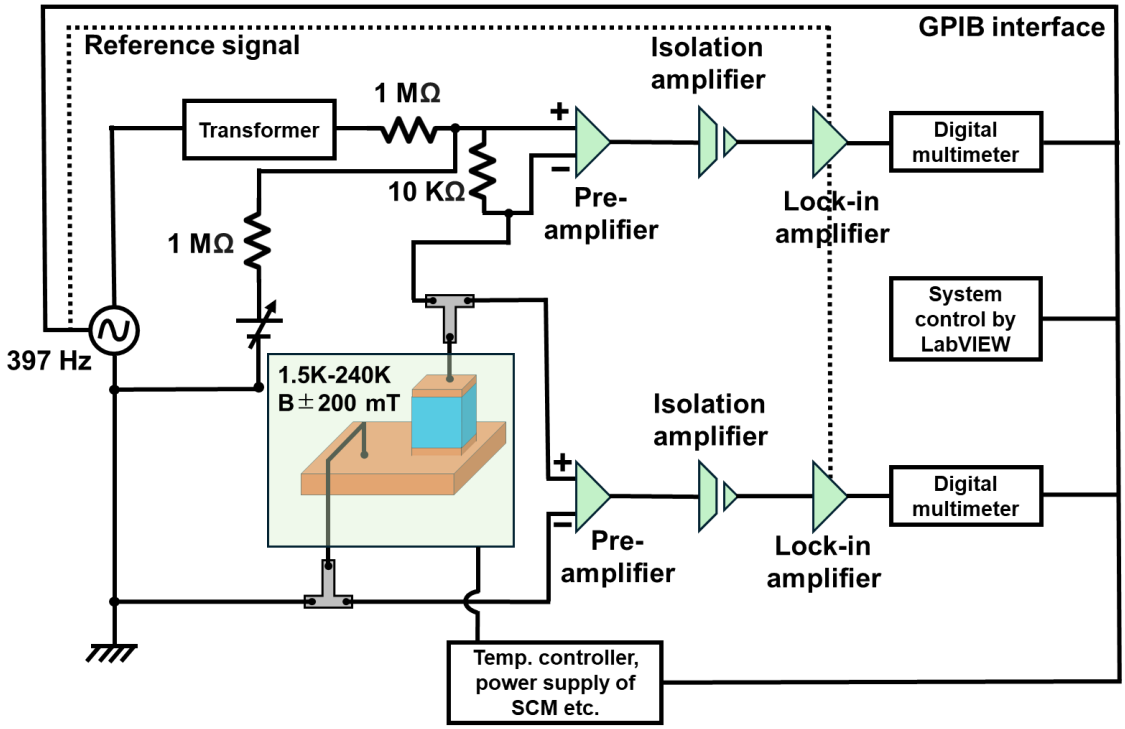


Figure 4.4 Spin-valve measurement setup.

Signal detection is performed using a series of high-precision instruments, including a preamplifier, an isolation amplifier, and a lock-in amplifier. These components are connected sequentially to process the signal efficiently. The lock-in amplifier acts as a highly selective band-pass filter, isolating the signal component that matches the frequency of the alternating current (AC). This filtered signal is then recorded using a digital multimeter for further analysis.

The entire setup is integrated and automated through a general-purpose interface bus (GPIB), which connects all the measuring instruments. This system is controlled using LabVIEW programming software, allowing for seamless synchronization, data collection, and real-time monitoring.

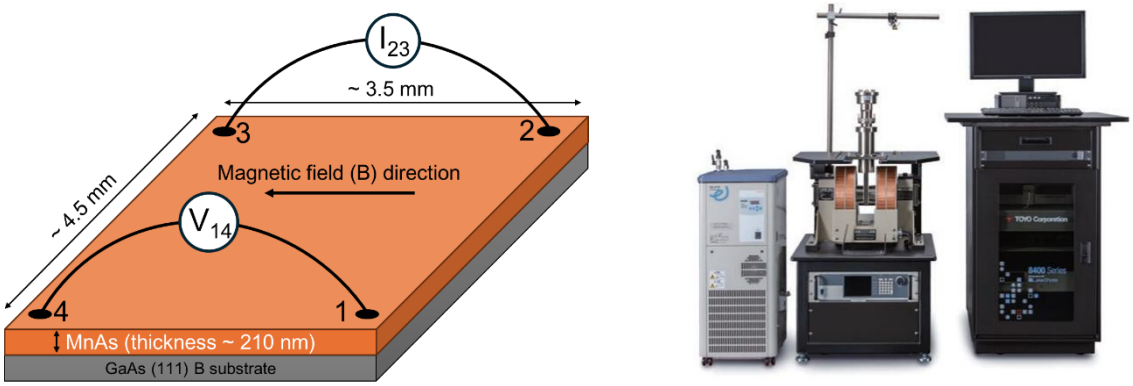
4.4 Magnetoresistance (MR) measurement of single MnAs layer

Magnetoresistance can be observed in epitaxially grown single MnAs layer also [6], usually referred to as anisotropic magnetoresistance (AMR). AMR is a phenomenon where the electrical resistance of a ferromagnetic material depends on the angle between the current direction and the magnetization direction [7]. This effect arises due to spin-dependent scattering of conduction electrons inside the ferromagnetic material.

Applying an external magnetic field affects the orientation of the MnAs magnetization. At zero or low fields, magnetic domains in MnAs may be randomly oriented. As the field increases, the magnetization aligns with the field direction, changing the relative angle between current and magnetization. This changes the resistance due to AMR.

Since the MnAs layers are part of the VSV structure, AMR could combine with spin-dependent scattering effects, enhancing the overall magnetoresistance signal. To identify the contribution of MR from MnAs in the VSV measurements, we carried out the MR

measurement of single MnAs layer grown on GaAs (111) B with a variable magnetic field DC measurement system.



ResiTest8400 system [8]

Figure 4.5 Magnetoresistance measurement setup for MnAs/GaAs(111)B.

Thickness of the MnAs layer was ~ 210 nm with an area of ~ 4.5×3.5 mm^2. Measurement was performed in Van der Pauw geometry with current (10 mA) parallel to the applied magnetic field (Figure 4.5).

4.5 VSV Measurement results: Local spin valve measurement

The local spin valve (LSV) measurement for a MnAs/InAs/MnAs vertical spin valve relies on detecting spin-polarized current through the heterostructure, leveraging the spin-dependent transport properties of the ferromagnetic MnAs layers and the non-magnetic semiconducting InAs spacer. In this configuration, spin-polarized electrons are injected from one MnAs layer into the InAs channel, with their transport influenced by the relative magnetization alignment of the top and bottom MnAs layers. The magnetization states, parallel or antiparallel, are controlled by an external magnetic field, with the layers having distinct coercive fields. The device exhibits a low resistance when the magnetizations are parallel, allowing efficient spin-polarized current transmission, and a high resistance when they are antiparallel, due to increased spin scattering. This resistance change, measured as a function of the magnetic field, reveals the spin valve effect and allows the calculation of the magnetoresistance (MR) ratio and spin injection efficiency (η). We will use the following model to extract injection efficiency [9]:

$$\frac{\Delta R}{R_o} = \frac{2\eta^2}{1-\eta^2} \qquad (4a)$$

$$\text{or,} \quad \eta^2 = \frac{\Delta R}{2R_o+\Delta R} \approx \frac{\Delta R}{2R_o} \qquad (4b)$$

Here, ΔR is the signal amplitude and R_o is the resistance at the parallel state.

Initially, we started measuring the device at 95 K with 1 μA applied current. We got a very small and noisy spin valve signal (Figure 4.6 a).

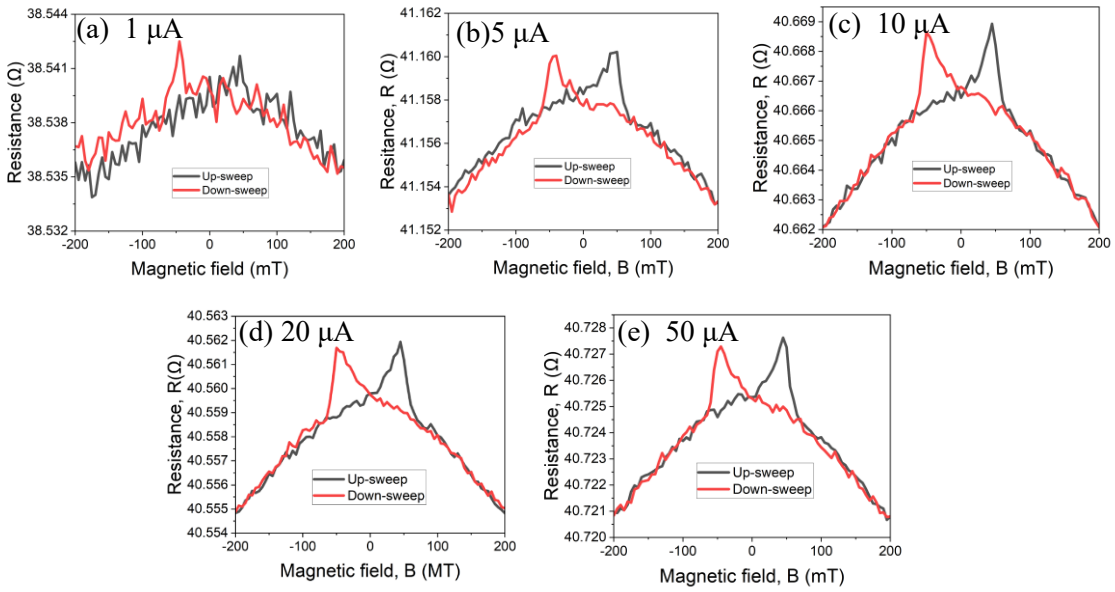


Figure 4.6 Spin valve measurement at 95 K with different applied current.

The excitation current applied to a spin valve device is critical for achieving a measurable signal with an adequate signal-to-noise ratio (SNR). A current that is too low may result in a voltage drop across the device that is insufficient to surpass the noise floor of the measurement system, leading to poor signal quality. Conversely, increasing the excitation current enhances the voltage signal, thereby improving the SNR and the clarity of the measured data [10]. Therefore, we increased the applied as indicated in the plots of Figure 4.6 (b-e). Increasing the excitation current improves the voltage signal (V=IR), enhancing the resolution of resistance changes due to the spin valve effect. This is evident as the signal transitions from noisy and indistinct in (a) to clear and sharp in (c) to (e).

However, it is essential to balance this increase against potential Joule heating effects ($P=I^2R$), which can alter the device's thermal equilibrium and affect its spin-dependent

transport properties, especially in low-temperature measurements [11].

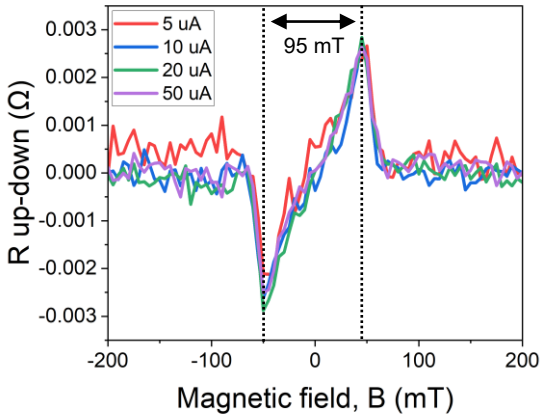


Figure 4.7 Hysteresis width at 95 K.

Figure 4.7 illustrates the hysteresis width (ΔB) at 95 K for the spin valve device, with measurements taken for various excitation currents (5 μA, 10 μA, 20 μA, and 50 μA). The plot shows the difference (R_{up}-R_{down}) in resistance between the up-sweep and down-sweep of the applied magnetic field (B), indicating the magnetization switching behavior of the ferromagnetic layers in the spin valve. The hysteresis width reflects the field range over which the magnetization of the layers switches, representing the coercive properties of the magnetic layers. The signal amplitude slightly increases with higher currents (e.g., 20 μA and 50 μA), improving the resolution of resistance changes. However, the hysteresis width remains constant at 95 mT, indicating that the magnetic switching behavior is independent of the excitation current in this range. This constancy highlights the stability of the spin valve's magnetic properties at low temperatures, while the improved signal clarity with increased current suggests better signal-to-noise performance at higher currents.

Afterward, we carried out the measurements at variable (higher) temperatures to observe the effect of temperature on the device performance (Figure 4.8 a-e).

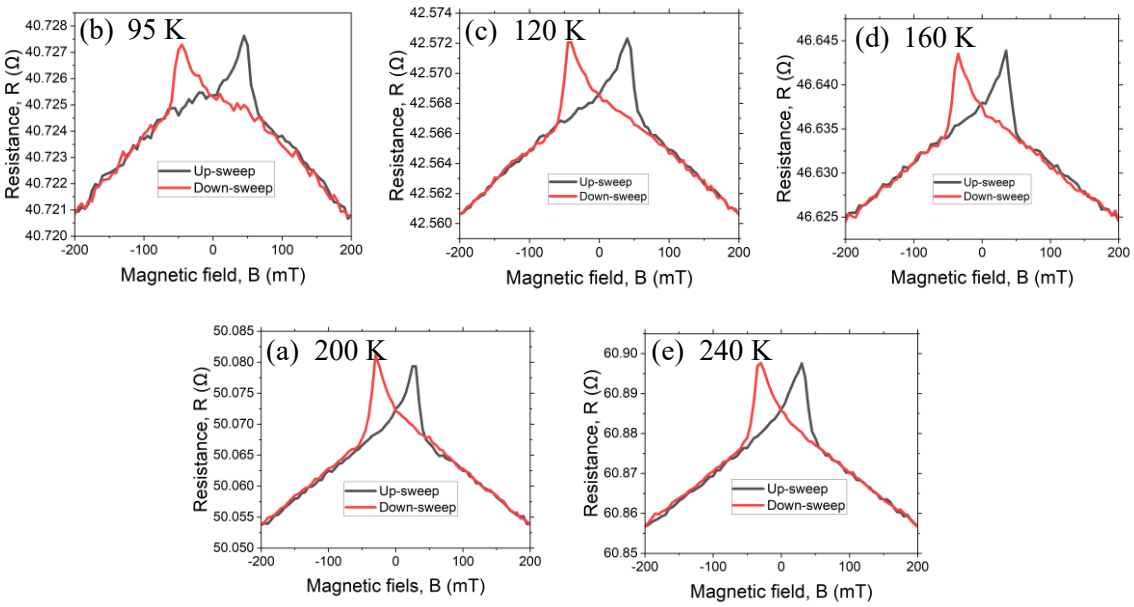


Figure 4.8 Spin valve signals at various temperatures with 50 μA applied current.

We observed a significant SNR with increasing the measurement temperature. At elevated temperatures, the electrical properties of InAs and MnAs, such as carrier density and resistivity, can become more compatible due to thermal activation. This improved impedance matching between the non-magnetic InAs spacer and the MnAs ferromagnetic layers reduces reflections or scattering of spin-polarized currents at the interfaces, resulting in smoother resistance transitions [12]. Additionally, InAs, as a narrow-bandgap semiconductor, exhibits increased carrier density and mobility at higher temperatures due to thermal excitation. This leads to better spin-polarized carrier transport across the channel, reducing noise or sharp fluctuations in the signal and producing a smoother response [13].

Afterward, we wanted to consider the MR contribution from single-MnAs into VSV measurements. Figure 4.9 shows the MR from MnAs at 95 K and 200 K.

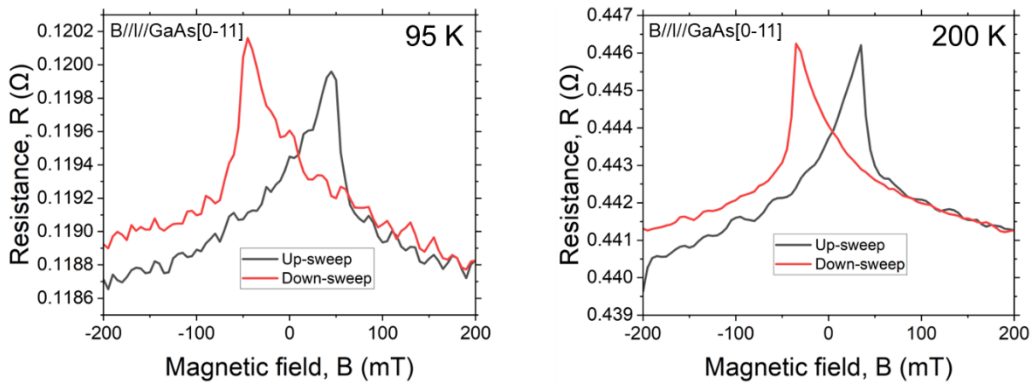


Figure 4.9 Magnetoresistance from MnAs/GaAs(111)B.

From the appearance of MR in MnAs, it's quite logical to think about its contribution and mechanism in VSV measurements, where there are two layers of MnAs are present.

So, we compared the peak and dip positions of magnetic switching from different measurement methods (Figure 4.10).

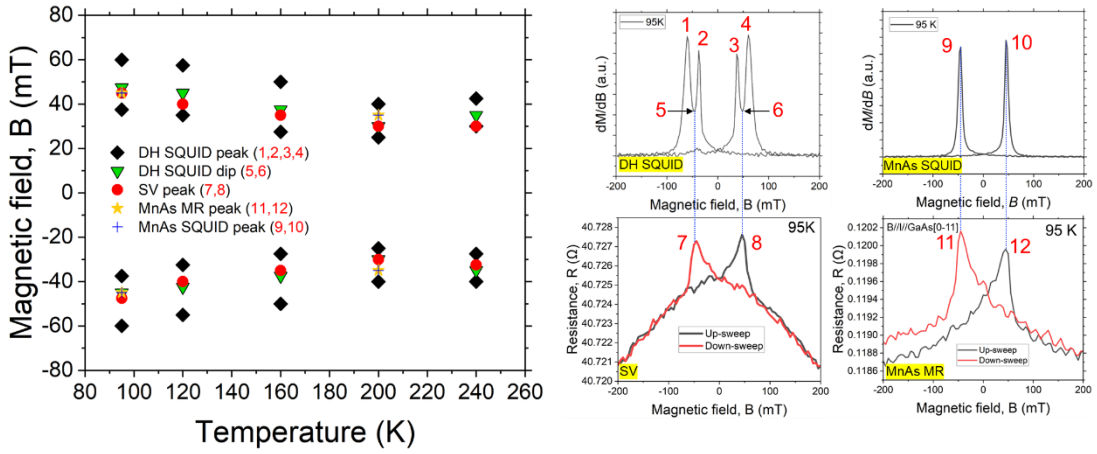


Figure 4.10 Magnetic switching in different measurement methods.

We can see that spin valve's magnetoresistance peaks (or DH SQUID dips) are located between the different switching fields of the upper and lower MnAs layers. Whereas the MR peaks from single MnAs comes from SQUID peaks. This emphasizes the different mechanism acting in VSV and single MnAs. We can also see the magnetic property of VSV device is almost consistent with as grown DH at all measurement temperatures and with single-MnAs at low measurement temperature. Thus, the influence of MR from single MnAs in SV measurements looks evident. We then investigated the dominant mechanism in VSV system.

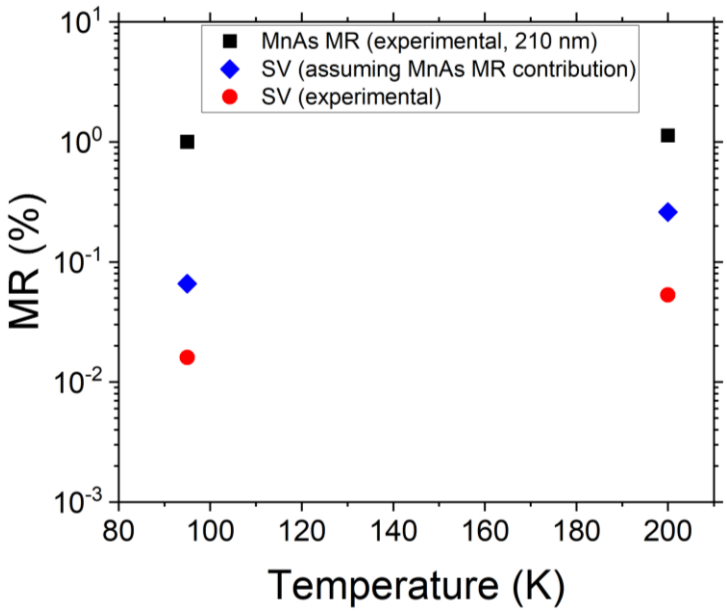


Figure 4.11 Comparison of MR in VSV, single MnAs and theoretical assumption.

From Figure 4.11 we can see a significant difference in MR between VSV and MnAs. We also assumed MnAs MR in VSV measurements and found it to be higher than actual results. This emphasizes more on the fact that contribution from single-MnAs MR might be mitigated in VSV measurements and Spin valve mechanism due to changing of

magnetic alignment between top and bottom MnAs looks dominating in VSV.

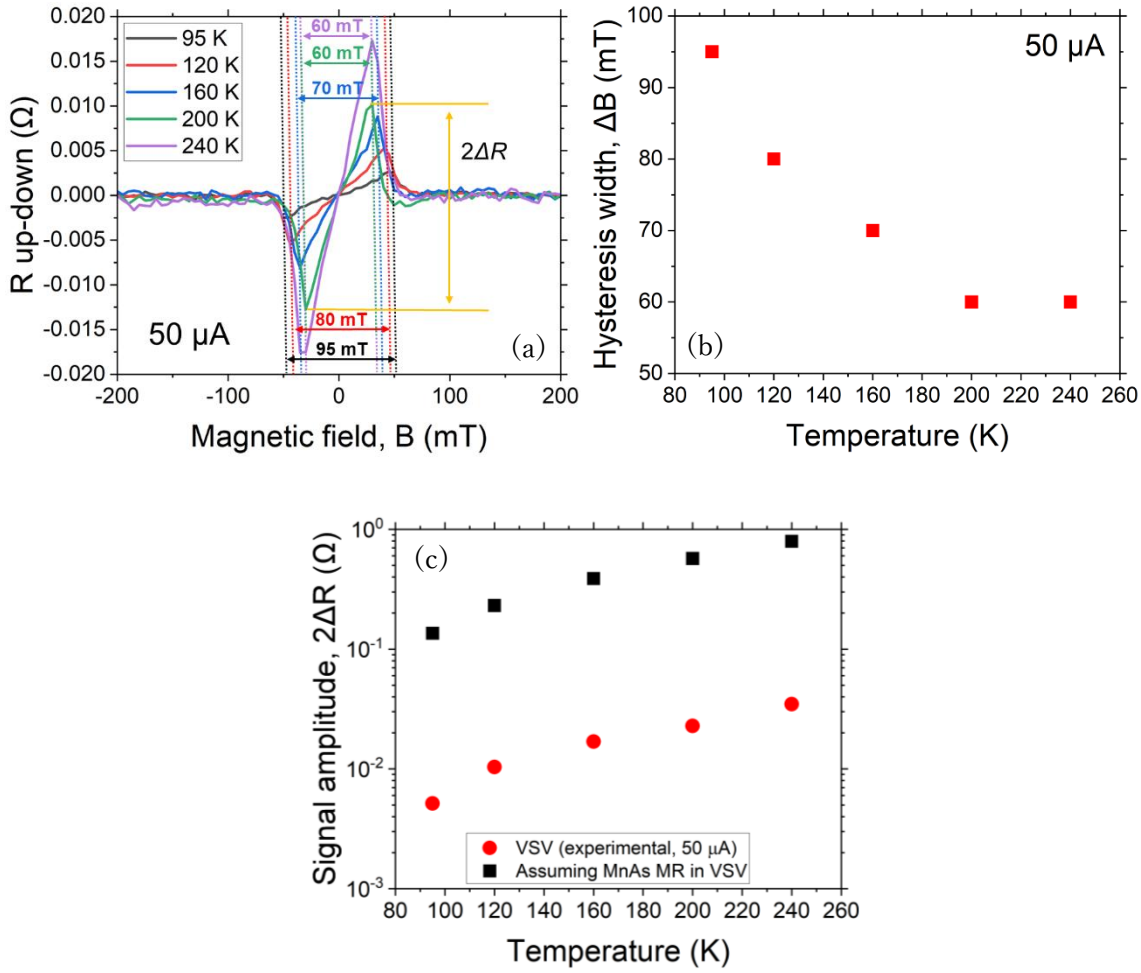


Figure 4.12 (a) Spin valve signal response at different temperatures, (b) change of hysteresis width (ΔB) with temperature, and (c) relationship of signal amplitude ($2\Delta R$) with temperature.

The discussion can be further strengthened from Figure 4.12, which presents the spin valve response and its temperature-dependent characteristics at a constant current of 50 μA. Figure 4.12 (a) shows the spin valve signal ($R_{up\text{-}down}$) as a function of the magnetic field (B) for different temperatures (95 K, 120 K, 160 K, 200 K, and 240 K). The

hysteresis width (ΔB) decreases with increasing temperature, as highlighted by the annotated hysteresis gaps. Figure 4.12 (b) quantifies this trend, demonstrating a clear reduction in ΔB with temperature, demonstrating reduced coercivity at higher temperatures results in easier magnetic switching. Figure 4.12 (c) illustrates the relationship between the signal amplitude ($2\Delta R$) and temperature, showing an increase in $2\Delta R$ with temperature. This behavior is attributed to improved spin transport efficiency at higher temperatures due to reduced impedance mismatch between the MnAs and InAs layers. We again compared the actual results with assuming MnAs MR in VSV and found that signal amplitude in VSV measurements are much lower than theoretical assumption, which indicates that the signals from VSV are due to the domination of carrier transport through channel.

To investigate the mechanism, let's consider the following two-current resistance model for spin-polarized current in a ferromagnetic/semiconductor/ferromagnetic (FM/SC/FM) trilayer system.

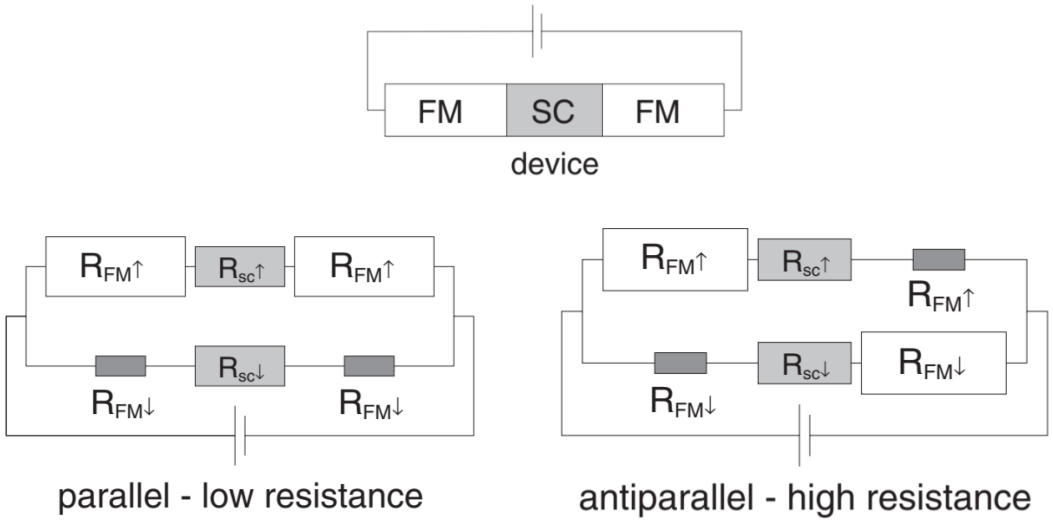


Figure 4.13 Two-current resistance model FM/SC/FM trilayer system. R_{FM} and R_{SC} correspond to resistances for ferromagnet and semiconductor channels respectively. Up and down arrows indicate the spin orientation. [14]

In a non-magnetic semiconductor, electron transport occurs equally for both spin orientations. When the spin flip length is sufficiently large, the semiconductor can be modeled as having two separate and independent spin channels that do not interact and share the same conductivity (Figure 4.13).

Spin polarization (α) quantifies the imbalance between spin-up ($j^{\uparrow}$) and spin-down ($j_{\downarrow}$) current densities:

$$\alpha = \frac{j^{\uparrow} - j^{\downarrow}}{j^{\uparrow} + j^{\downarrow}} \qquad (4c)$$

In the semiconductor, the resistances for the two spin channels ($R_{SC}^{\uparrow}$ and $R_{SC}^{\downarrow}$) are considered equal. For the ferromagnetic layers, the spin-dependent resistance depends on the magnetization alignment. In the parallel configuration, the spin-up resistances in both ferromagnetic layers are equal ($R_{FM1}^{\uparrow} = R_{FM2}^{\uparrow}$), as are the spin-down resistances ($R_{FM}^{\downarrow}$=$R_{FM}^{\downarrow}$). In the antiparallel configuration, the spin-up resistance of the first layer matches the spin-down resistance of the second ($R_{FM1}^{\uparrow} = R_{FM2}^{\uparrow}$), and vice versa ($R_{FM}^{\downarrow}$=$R_{FM2}^{\uparrow}$).

For the antiparallel magnetization configuration, the resistances of the two spin channels become equal, resulting in zero net current polarization (equation 4c). In contrast, the parallel magnetization scenario exhibits differing resistances between the spin channels, leading to a total current polarization expressed as [14]:

$$\alpha = \frac{\beta \frac{R_{FM}}{R_{SC}}}{\frac{R_{FM}}{R_{SC}} + (1 - \beta^{2})} \qquad (4d)$$

where, β is the spin polarization in ferromagnet. In this equation (4d), the dominating factor is the R_{FM}/R_{SC}, which defines the impedance mismatch between ferromagnet and semiconductor (MnAs and InAs in our system). Optimal impedance matching ($R_{FM} \approx R_{SC}$) ensures efficient spin-polarized current transport and high magnetoresistance ratios.

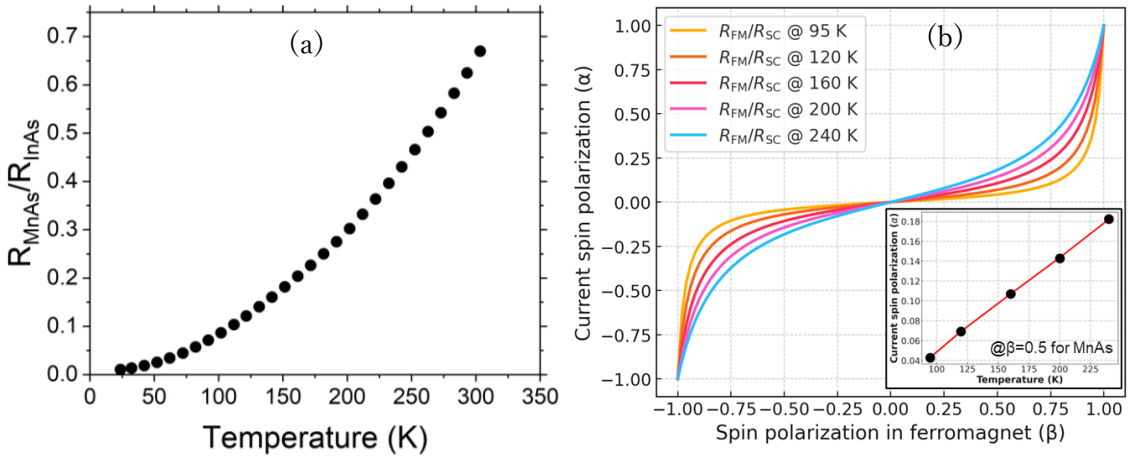


Figure 4.14 (a) Relationship of resistance ratio between MnAs and InAs with temperature and (b) Dependence of current spin polarization (α) on spin polarization in ferromagnet (β) at various temperatures (inset shows temperature dependence of α).

Figure 4.14 (a) was derived from the Hall measurements of the individual MnAs and LT-InAs layers, and it provides insight into the effect of temperature on the spin-dependent transport properties in the vertical spin valve (VSV) device structure. As the temperature increases, the resistance ratio rises significantly, reflecting a relative increase in the resistivity of MnAs compared to InAs.

The observed trend suggests an improvement in the spin-polarized current transport within the device (Figure 4.14 b). At higher temperatures, the reduced impedance mismatch between MnAs and InAs minimizes spin scattering at the interface, facilitating more efficient spin injection and transmission.

We extracted spin injection efficiency (η) from the local spin valve measurement we performed, using equation (4b). We also calculated our expectation of injection efficiency using the following relation [15]:

$$\eta = \frac{\alpha}{\beta} \times 100\ \% \qquad (4e)$$

where β is about 0.5 for MnAs.

Figure 4.15 shows the injection efficiencies at different temperatures with applied current of 50 μA. The data demonstrates a clear trend of increasing injection efficiency as the temperature rises from 95 K to 240 K. At lower temperatures, the spin injection efficiency is around 0.6%, indicating significant challenges in achieving effective spin-polarized current transport. As the temperature increases, η improves steadily, reaching about 1.2% at 240 K. These values are much lower than what was expected from the R_{FM}/R_{SC} of the structure.

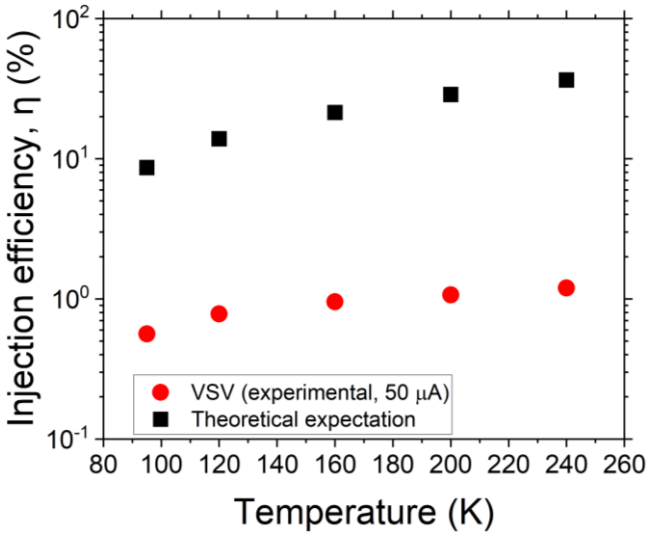


Figure 4.15 Spin injection efficiency at various temperatures.

The spin injection efficiency in the MnAs/InAs/MnAs structure is significantly

influenced by the electrical properties of LT-InAs, which inherently contains a high concentration of defects. These defects, such as antisite defects, interstitials, and dislocations, act as scattering centers for injected spin-polarized carriers. As a result, rather than maintaining their original spin polarization while traversing the InAs channel, these carriers undergo frequent scattering events, leading to spin relaxation and a reduced spin diffusion length.

Moreover, the high carrier concentration in LT-InAs, which arises due to donor nature of antisite As, results in an enhanced background conductivity. This elevated carrier density effectively shortens the spin relaxation time by increasing electron-electron and electron-defect interactions. Consequently, the spin polarization of the injected carriers rapidly diminishes before reaching the opposite MnAs electrode, thereby lowering the overall spin injection efficiency. These effects, which stem from the interplay between defect-induced scattering and high free-carrier concentration, were extensively analyzed in Chapter 3, where the structural and electronic properties of LT-InAs were discussed in detail.

Additional facts that may come into play are; **i)** Imperfections or defects at the MnAs/InAs interface, such as roughness, chemical inhomogeneity, or interfacial states, can act as scattering centers. These defects increase the probability of spin decoherence and reduce the efficiency of spin transfer. We observed in our material that it consists rough surface morphology as well as interface was compromised, and **ii)** interface damage during device fabrication and formation of magnetically inactive "dead layer" at the MnAs surface due to chemical reactions or fabrication steps, reduce the effective magnetization at the interface and limiting spin polarization.

However, despite the low spin injection efficiency observed in our device, this work

represents a significant milestone as the first successful demonstration of a vertical spin valve using a MnAs/thick-InAs/MnAs double heterostructure. This accomplishment highlights the feasibility of integrating thick InAs as a spin transport channel and showcases the potential of this unique material system for spintronic applications. The successful measurement of spin valve behavior in this novel structure reflects a significant advancement in device fabrication and characterization, providing a strong foundation for future research aimed at optimizing performance and unlocking new functionalities in spintronic devices. This work not only validates the concept but also opens new avenues for exploring complex spin-dependent phenomena in hybrid material systems.

Summary

The successful fabrication and characterization of a vertical spin valve (VSV) device using MnAs/InAs/MnAs heterostructures were presented for the first time. The MnAs layers, designed with distinct thicknesses to achieve separate coercive fields, enabled spin valve operation. The fabrication process resulted in well-defined vertical structures suitable for studying spin transport. Electrical measurements performed at low temperatures using the AC lock-in technique revealed a clear spin valve signal, demonstrating the functionality of the device. The temperature-dependent behavior of the device system was thoroughly studied, showing a significant influence on spin transport characteristics with varying measurement temperatures. Additionally, the excitation current was found to play a crucial role in determining the device performance.

Despite the observed spin valve behavior, impedance mismatch significantly impacted the overall efficiency of spin injection into the semiconductor channel. The device exhibited a maximum spin injection efficiency of 1.2%, highlighting the need for further improvement of the LT-InAs and interface properties to enhance performance.

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Chapter 5: Summary and Prospects

5.1 Summary of the work

This work presents a comprehensive investigation into the growth, fabrication, and characterization of MnAs/InAs/MnAs double heterostructures for spintronic applications. The successful integration of thick InAs channels with MnAs layers, achieved through molecular beam epitaxy (MBE), highlights the complexity and innovation involved in realizing functional vertical spin valve devices. Precise control of growth conditions and material optimization played a crucial role in overcoming challenges and ensuring high-quality heterostructures.

The MnAs layers were grown with optimized beam equivalent pressure (BEP) ratios to achieve smooth surfaces and uniformity. GaAs (111) B substrates were used as the base for epitaxial growth, with careful thermal cleaning and oxide removal to prepare the substrate for deposition. InAs was deposited at low temperatures (~250°C), which reduced thermal strain and minimized interface degradation. Cross-sectional SEM imaging revealed well-defined interfaces, while X-ray diffraction (XRD) analysis showed minimal residual strain in the optimized samples. The distinct coercive fields of the MnAs layers, as confirmed by magnetization measurements, indicated their suitability for spin valve applications.

Low-temperature InAs growth posed additional challenges, including reduced adatom mobility leading to defects such as stacking faults and voids. Excess arsenic contributed to antisite defects, which affected the electrical properties of the channel. To address these

issues, the V/III ratio during growth was optimized, with a ratio of 10 yielding the smoothest surfaces and best electrical performance. Temperature-dependent growth studies further highlighted the importance of fine-tuning deposition conditions. Growth temperatures below 235°C increased surface roughness, while higher temperatures (~480°C) improved the smoothness of the InAs channel. Electrical measurements demonstrated n-type conduction with high carrier concentration, primarily due to arsenic-related defects. The optimized InAs sample showed improved mobility and carrier concentration, validating the growth parameters used.

Fabrication of the vertical spin valve device involved a combination of advanced lithographic techniques and etching methods to define the geometry. MnAs layers were deposited as the top and bottom electrodes, while the thick InAs channel served as the spin transport medium. Marker and electrode fabrication utilized photolithography and sputtering techniques to achieve precise alignment and reliable electrical connectivity. Magneto-transport measurements were performed in a current-perpendicular-to-plane (CPP) geometry, providing insight into the spin-dependent transport behavior. Despite these efforts, the performance of the vertical spin valve did not surpass that of lateral spin valves, primarily due to the large impedance mismatch and the crystal quality limitations of the low-temperature-grown InAs channel.

While challenges such as impedance mismatch and interface imperfections limited spin injection efficiency, this work represents a significant milestone as the first successful demonstration of a vertical spin valve using MnAs/thick-InAs/MnAs double heterostructures. The findings establish a strong foundation for future advancements in

spintronic devices. Improvements in material growth, interface engineering, and device design could lead to enhanced spin injection efficiency and better device performance. This work opens new avenues for exploring spintronic phenomena and developing innovative applications using hybrid semiconductor/ferromagnet systems.

5.2 Future prospects

The findings of this work highlight several areas for further exploration and improvement to advance the performance and functionality of vertical spin valve devices based on MnAs/InAs/MnAs heterostructures. These future directions focus on improving material quality, device fabrication, and spin transport efficiency.

A key area for improvement is the growth of low-temperature InAs (LT-InAs). While this work has achieved considerable success in optimizing growth parameters, challenges such as surface roughness and defect formation remain. Exploring alternative growth methods, such as migration-enhanced epitaxy (MEE), could offer solutions by enabling finer control over adatom mobility during deposition. MEE alternates between supplying group III and group V elements, promoting smoother layer formation and minimizing defect densities. Such advancements would enhance the structural, electrical, and morphological properties of LT-InAs, making it a more robust channel material for spin transport.

Another critical focus is the improvement of the interface between MnAs and InAs. The quality of this interface directly impacts spin injection efficiency, as imperfections can act as scattering centers and reduce spin polarization. Techniques such as interface passivation or the use of interlayers to smooth the transition between the ferromagnet and

semiconductor could be explored. Advanced characterization methods, such as atomic-resolution transmission electron microscopy (TEM), can also provide insights into atomic-level interface structures, guiding strategies to minimize defects and optimize spin transparency.

Addressing the impedance mismatch between MnAs and InAs is another priority. This mismatch arises from the significant disparity in their electrical conductivities, which limits spin injection efficiency. One approach is to use semiconductor alloys with higher conductivity, such as InAs-based alloys doped with high-mobility elements. Alternatively, reducing the conductivity of the ferromagnet by alloying MnAs with other elements could balance the resistance mismatch. Such efforts would facilitate better impedance matching, reducing spin loss at the interface and improving overall device performance.

Improvements in the fabrication process are also crucial for advancing the technology. Greater precision in defining the device geometry, particularly in the formation of nanostructures, is necessary. Developing fabrication processes for non-local spin valve (NLSV) measurements would expand the range of spintronic functionalities explored. These measurements require creating highly precise vertical devices, emphasizing the need for advanced lithography and etching techniques. Enhanced control over the fabrication process would lead to more reliable devices with consistent spin transport properties.

Another exciting avenue involves the precise control of nano-post formation, which could pave the way for fabricating gate-all-around (GAA) vertical spin field-effect transistors (spin-FETs). This emerging device architecture combines spin transport with electrical

gating, enabling dynamic control over spin currents. Achieving such functionality requires exceptional precision in nanostructuring to form uniform posts and all-around gates. This would not only extend the functionality of spin valve devices but also position the technology at the forefront of spin-based logic and memory applications.

List of publications

Journals

1. **Md Tauhidul Islam**, Md. Faysal Kabir, Masashi Akabori, “Low-temperature grown MnAs/InAs/MnAs double heterostructure on GaAs (111) B by molecular beam epitaxy”, Jpn. J. Appl. Phys., Vol. 63, pp. 01SP40-1-5 (2024).
2. Md. Faysal Kabir, **Md Tauhidul Islam**, Soh Komatsu, Masashi Akabori, “Growth temperature dependence of MnSb synthesis on GaAs (111)B using molecular beam epitaxy”, Jpn. J. Appl. Phys., Vol. 63, pp. 01SP37-1-5 (2024).

Conferences

1. **Md Tauhidul Islam*** and Masashi Akabori, “Low Temperature Growth of InAs on GaAs (111) B”, JSAP Hokuriku/Shin-etsu Chapter (December, 2022).
2. **Md Tauhidul Islam*** and Masashi Akabori, “Low Temperature MBE Growth of InAs on GaAs (111) B”, International Symposium on Empathy and Symbiosis with Nature (December, 2022).
3. **Md Tauhidul Islam*** and Masashi Akabori, “Low Temperature MBE Growth of InAs on GaAs (111) B”, 2022 JAIST International Symposium of Nanomaterials and Devices Research Area. “Quantum Devices and Metrologies” (December, 2022).
4. **Md Tauhidul Islam*** and Masashi Akabori, “Growth and Structural Properties of Low-temperature grown InAs/MnAs Hybrid Structure on GaAs (111) B”, The 70th JSAP Spring Meeting (March, 2023).
5. **Md Tauhidul Islam*** and Masashi Akabori, “Low-temperature grown MnAs/InAs/MnAs double heterostructure on GaAs (111) B by molecular beam epitaxy”, The 9th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO) (June, 2023).
6. Md. Faysal Kabir*, **Md Tauhidul Islam**, Masashi Akabori, “Growth temperature dependence of MnSb synthesis on GaAs (111) B using molecular beam epitaxy”, The 9th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO) (June, 2023).
7. **Md Tauhidul Islam**, Md. Faysal Kabir, Masashi Akabori*, “Molecular beam epitaxial growth of MnAs/InAs and MnSb/InSb hybrid structures for spintronic device applications”, The 4th International Workshop on Advanced Materials and

Devices (IWAMD) (August, 2023).

8. **Md Tauhidul Islam**, Van Thuan Pham, Yingshu Ma, Masashi Akabori*, "Lateral And Vertical Spin Valve Devices Using Molecular Beam Epitaxial Grown MnAs/InAs Hybrid Structures", The 8th International Workshop on Nanotechnology and Application (IWNA) (November, 2023).
9. Van Thuan Pham, **Md Tauhidul Islam**, Masashi Akabori*, "Fabrication and Measurement of Vertical Spin Valve Based on MnAs/InAs/MnAs on GaAs (111) B Materials", JSAP Hokuriku Shin-etsu Chapter Meeting, (December, 2023).
10. **Md Tauhidul Islam***, Masashi Akabori, "Influence of InAs thickness on surface morphology in low-temperature grown MnAs/InAs/MnAs double heterostructure on GaAs (111) B", JAIST International symposium: Nano-Materials for Novel Devices (NMND) (January, 2024)
11. Md. Faysal Kabir*, **Md Tauhidul Islam**, Masashi Akabori, "MnSb and InSb grown on GaAs (111) B for spin-FET application", JAIST International symposium: Nano-Materials for Novel Devices (NMND) (January, 2024)
12. Van Thuan Pham*, **Md Tauhidul Islam**, Soh Komatsu, Masashi Akabori, "Fabrication and Characterization of Vertical Spin Valve Devices Based on MnAs/InAs/MnAs/GaAs(111)B with several hundred nanometer width", JSAP SPRING Meeting (March, 2024).
13. Van Thuan Pham*, **Md Tauhidul Islam**, Soh Komatsu and Masashi Akabori, "Vertical Spin Valve Devices using MnAs/InAs/MnAs on GaAs (111) B", 7th Organic and Inorganic Electronics Symposium (O&I Symposium) (June, 2024).
14. Jannatul Ferdousy*, Soh Komatsu, Yingshu Ma, Md. Faysal Kabir, **Md Tauhidul Islam**, Masashi Akabori, "Amorphous Fe^3O^4 thin film deposition on GaAs (001)

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