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ABSTRACT

We report normally-off operations in partially-gate-recessed Al_xTi_yO(AlTiO)/AlGaN/GaN metal-insulator-semiconductor (MIS) field-effect transistors (FETs), where aluminum titanium oxide AlTiO, an alloy of Al_2O_3 and TiO_2, is employed as a gate insulator. Since AlTiO is useful for interface charge engineering owing to a trend that the AlTiO/AlGaN interface fixed charge is suppressed in comparison with Al_2O_3, we investigated combining the interface charge engineering with a partial gate recess method for AlTiO/AlGaN/GaN MIS-FETs. For AlTiO with a composition of $x/(x+y) = 0.73$, a suppressed positive interface fixed charge at the AlTiO/recessed-AlGaN interface leads to a positive slope in the relation between the threshold voltage and the AlTiO insulator thickness. As a result, we successfully obtained normally-off operations in partially-gate-recessed AlTiO/AlGaN/GaN MIS-FETs with favorable performances, such as a threshold voltage of 1.7 V, an on-resistance of 9.5 Ω mm, an output current of 450 mA/mm, a low sub-threshold swing of 65 mV/decade, and a rather high electron mobility of 730 $cm^2/V\,s$. The results show that the interface charge engineering in combination with partial gate recess is effective for the GaN-based normally-off device technology.

I. INTRODUCTION

For a gate insulator of GaN-based metal-insulator-semiconductor (MIS) field-effect transistors (FETs), high-dielectric-constant (high-k) oxides Al_2O_3,[1] HfO_2,[2,3] TiO_2,[4] AlSiO,[5,6] AlTiO,[7–11] high-k oxynitrides TaON,[12] AlON,[13] and high-k nitrides BN,[14,15] AlN[16–20] have been investigated. In any case, understanding and controlling the insulator/semiconductor interface is indispensable for the development of the MIS device technology. In addition to the problem of device instability caused by the interface traps,[21] effects of the interface fixed charge are critical issues. When an insulator such as Al_2O_3 is deposited on a GaN-based semiconductor having a negative surface polarization charge, there is a tendency that a positive interface fixed charge is generated and neutralizes the polarization charge.[22–29] The interface fixed charge has significant effects on the MIS device characteristics, especially on the threshold voltage. A high-density positive interface fixed charge shifts the threshold voltage V_{th} negatively when the insulator thickness d_{ins} increases. While the semiconductor polarization is an intrinsic material property, the origin of the interface fixed charge is not clearly elucidated. Since the positive interface fixed charge is not a necessity,[26,27,30,31] if it is sufficiently suppressed, V_{th} increases as d_{ins} increases, being useful for normally-off operations of the MIS-FETs. The threshold voltage of the MIS devices can be controlled by controlling the interface fixed charge; the technology aimed at this is called "interface charge engineering."[26]

Toward realization of normally-off AlGaN/GaN devices, several methods, such as partial gate recess,[32] full gate recess,[33] fluoride plasma treatment,[34] p-type (Al)GaN capping,[35,36] selective electro-chemical oxidation,[37] and fin-structure formation,[38] have been investigated. The full gate recess method is considered to be effective to obtain a high threshold voltage, although low output currents and a high on-resistance due to a low channel electron mobility at the insulator/etched-GaN interface are major drawbacks. However, when using an Al_2O_3 gate insulator and the full gate recess method, a threshold voltage lower than the theoretical

value is often obtained, owing to the positive Al_2O_3/GaN interface fixed charge.[39,40] The partial gate recess is more suitable to obtain normally-off operations with high output currents and a low on-resistance. In order to avoid degradation of the channel electron transport properties due to recess etching damage and interface charge scattering, it is preferable to employ a thick remaining AlGaN layer, although a thin remaining AlGaN layer $\lesssim 2$ nm is often required owing to the positive Al_2O_3/etched-AlGaN interface fixed charge.[41] Therefore, if the interface charge engineering succeeds to suppress the positive Al_2O_3/etched-AlGaN interface fixed charge, normally-off operations with a good channel electron transport can be realized for partial recess with a thicker remaining AlGaN layer.

In this study, we employed Al_xTi_yO (AlTiO) as a gate insulator of partially-gate-recessed AlGaN/GaN MIS devices. AlTiO, an alloy of Al_2O_3 (energy gap $E_g \sim 7$ eV, dielectric constant $k \sim 10$) and TiO_2 ($E_g \sim 3$ eV, $k \sim 60$), is a versatile insulator, because it can be applied to dielectric constant engineering as well as energy gap engineering, via controlling its composition x:y.[42–45] Moreover, it has been shown that AlTiO is useful for interface charge engineering owing to a trend that the positive AlTiO/AlGaN interface fixed charge is suppressed in comparison with Al_2O_3.[9,11] Based on the interface charge engineering, for a composition of $x/(x+y) = 0.73$, a suppressed positive interface fixed charge at the AlTiO/recessed-AlGaN leads to a positive slope in the relation between the threshold voltage V_{th} and the AlTiO insulator thickness d_{ins}. As a result, we obtained normally-off operations in the partially-gate-recessed AlTiO/AlGaN/GaN MIS devices with a ~ 4 nm-thick remaining AlGaN layer, which thickness leads to normally-on operations for Al_2O_3/AlGaN/GaN MIS devices. The normally-off AlTiO/AlGaN/GaN MIS-FETs show favorable performances such as a threshold voltage of 1.7 V, an on-resistance of 9.5 Ω mm, an output current of 450 mA/mm, a low sub-threshold swing of 65 mV/decade, and a rather high electron mobility of 730 $cm^2/V\,s$.

II. DEVICE FABRICATION

The fabrication of the partially-gate-recessed AlTiO/AlGaN/GaN MIS devices, MIS-capacitors [Fig. 1(a)] and MIS-FETs [Fig. 1(d)], started from an $Al_{0.24}Ga_{0.76}N$ (20 nm)/GaN (3 μm) heterostructure on sapphire(0001), followed by Ti/Al/Ti/Au Ohmic electrode formation. As gate recess process, the AlGaN layer was etched by using electron cyclotron resonance (ECR) nitrogen plasma. The etching rate and depth were ~ 1.2 nm/min and ~ 16 nm (i.e., AlGaN remaining thickness $d_{AlGaN} \sim 4$ nm), respectively, as measured by atomic force microscopy (AFM) showing the etched-AlGaN surface morphology given in Fig. 1(c), where the roughness is ~ 0.5 nm. After etched-AlGaN surface cleaning to remove oxide and oxygen-related molecules, several compositions of AlTiO gate insulators with several thicknesses were formed by atomic layer deposition (ALD) using TMA (trimethyl aluminum), TDMAT (tetrakis-dimethylamino titanium), and water,[7,9,11] followed by post-deposition annealing at 350 °C in H_2-mixed Ar. After necessary device isolation by B^+ ion implantation, Ni/Au gate electrodes were formed. Finally, post-gate annealing at 400 °C in N_2 completed the device fabrication. The device size and the top view image of the MIS-capacitors are shown in Figs. 1(a) and 1(b), respectively, where the recessed area $S_1 = 65^2\,\mu m^2$ and the non-recessed area $S_2 = (70^2 - 65^2)\,\mu m^2$ under the gate are surrounded by the Ohmic electrodes. Figure 1(d) shows the device size of the MIS-FETs, where the recessed gate length of $L_G = 2.5\,\mu m$ is overlapped by the 3-μm-length gate metal, with the source-drain distance of 5 μm, and the gate width is $W_G = 50\,\mu m$.

Although the positive fixed charge density at the AlTiO/AlGaN interface decreases with a decrease in the Al compositions of AlTiO,[11] the decrease in the energy gap E_g and the insulator/AlGaN conduction band offset ΔE_C will lead to an increase in leakage currents of MIS devices. To avoid the leakage, gate insulators having $\Delta E_C \geq 1$ eV are preferable. Therefore, in this study, we employed three compositions of Al_xTi_yO gate insulators: $x/(x+y) = 1.0$ (Al_2O_3, $k \simeq 8$, $E_g \simeq 7$ eV, $\Delta E_C \simeq 1.7$ eV), $x/(x+y) = 0.84$ ($k \simeq 10$, $E_g \simeq 6.3$ eV, $\Delta E_C \simeq 1.4$ eV), and $x/(x+y) = 0.73$ ($k \simeq 13$, $E_g \simeq 6$ eV, $\Delta E_C \simeq 1.3$ eV).[11]

III. DEVICE CHARACTERIZATION

Capacitance-voltage (C-V_G) characteristics of the AlTiO/AlGaN/GaN MIS-capacitors were measured at 1 MHz. Figure 2 shows the C-V_G characteristics for several AlTiO insulator thicknesses d_{ins}, with the inset depicting the equivalent circuit of the devices, where the capacitance of the recessed area S_1 is in parallel with the capacitance of the non-recessed area S_2. We observe a step-like behavior of the C-V_G characteristics; the lower-voltage step corresponds to the threshold voltage of the non-recessed area, whereas the higher-voltage step to that of the recessed area. Only for $x/(x+y) = 1.0$, additional steps are observed in the range of $V_G \gtrsim 3$ V, owing to the spillover at the insulator/AlGaN in the non-recessed area, where rather large overdrive voltages are applied due to the negatively large threshold voltages. The two-dimensional electron gas (2DEG) sheet concentration n_S under the gate can be obtained by the integration of C as a function of V_G, as shown in Fig. 2 with two linear fittings corresponding to n_S increases in the non-recessed and recessed areas. The threshold voltage of the non-recessed area V_{th2} is determined at $n_S = 0$, while that of the recessed area V_{th1} is obtained by the intersection between the two fitting lines.

The threshold voltage V_{th} of an AlGaN/GaN MIS device dominated by an insulator/semiconductor interface fixed charge density σ_{ins} is given by a linear function of the insulator thickness d_{ins},

$$V_{th} = \frac{\sigma_{GaN} - \sigma_{ins}}{k_{ins}\epsilon_0} d_{ins} - \frac{\sigma_{AlGaN} - \sigma_{GaN}}{k_{AlGaN}\epsilon_0} d_{AlGaN} + (\phi - \varphi - \Delta E_C)/q, \quad (1)$$

using the elementary charge $q > 0$, the vacuum permittivity ε_0, the polarization charge densities σ_{GaN} and σ_{AlGaN}, the dielectric constants k_{ins} and k_{AlGaN}, the thicknesses d_{ins} and d_{AlGaN}, the metal-insulator barrier height ϕ, the insulator-AlGaN conduction band offset φ, and the AlGaN-GaN conduction band offset ΔE_C, where the slope is $(\sigma_{GaN} - \sigma_{ins})/(k_{ins}\varepsilon_0)$.[11] It should be noted that, in the

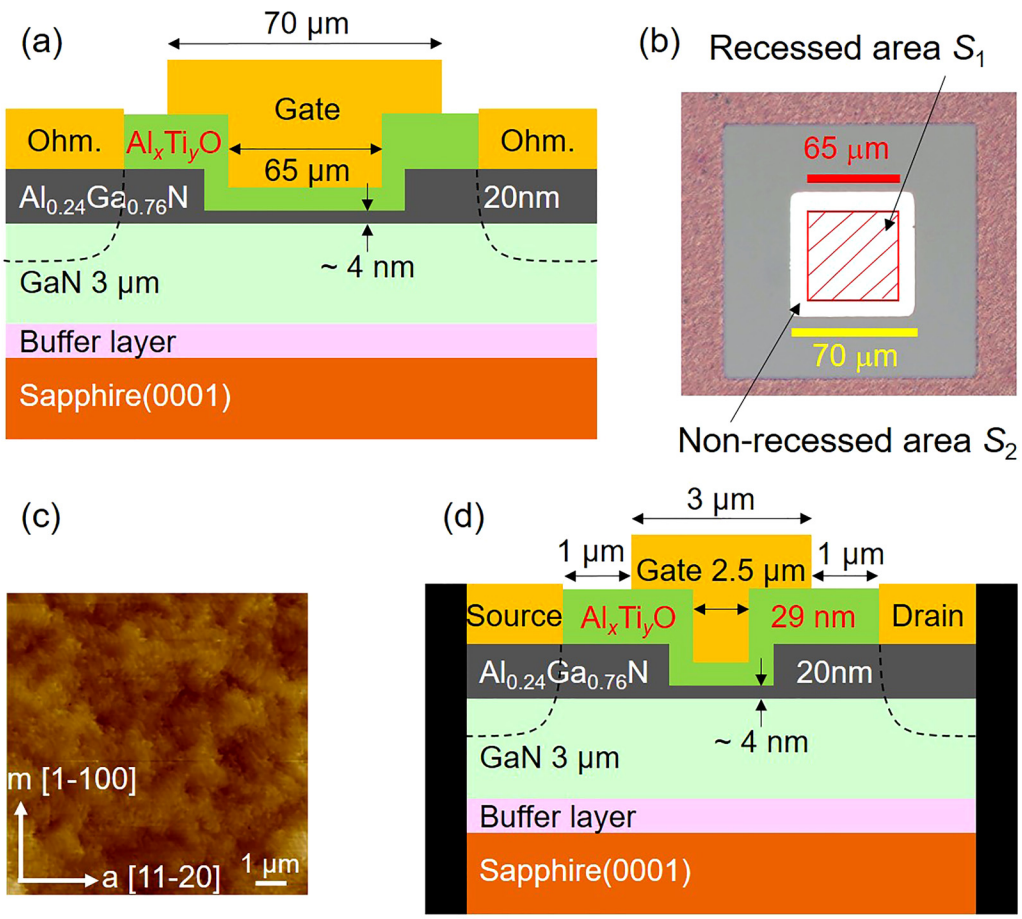

FIG. 1. (a) The structure and (b) the top view image of the partially-recessed AlTiO/AlGaN/GaN MIS-capacitors. (c) An AFM image of the etched-AlGaN surface. (d) The structure of the partially-recessed AlTiO/AlGaN/GaN MIS-FETs.

limit of $d_{ins} \rightarrow 0$, (1) gives

$$V_{th}(d_{ins} \rightarrow 0) = -\frac{\sigma_{AlGaN} - \sigma_{GaN}}{k_{AlGaN}\epsilon_0} d_{AlGaN} + (\phi - \varphi - \Delta E_C)/q, \quad (2)$$

where $(\phi - \varphi)$ can depend on the AlTiO composition. On the other hand, using the metal-AlGaN barrier height $\tilde{\phi}$, V_{th} of a Schottky device is given by

$$V_{th} = -\frac{\sigma_{AlGaN} - \sigma_{GaN}}{k_{AlGaN}\epsilon_0} d_{AlGaN} + (\tilde{\phi} - \Delta E_C)/q, \quad (3)$$

which can be different from (2). Figures 3(a) and 3(b) show the obtained threshold voltages as functions of d_{ins} for the non-recessed and recessed areas, respectively. Basically, we observe linear relations of V_{th}-d_{ins}, confirming that V_{th} is dominated by the interface fixed charge. Although the linearity is not good for the recessed area of $x/(x+y) = 1.0$, this can be attributed to data dispersion related to the interface fixed charge rather than the bulk charge, since the non-recessed area exhibits a linear behavior. We observe $V_{th} < 0$ of the recessed area for $x/(x+y) = 1.0$, showing that the AlGaN remaining thickness $d_{AlGaN} \sim 4$ nm leads to normally-on operations for Al_2O_3/AlGaN/GaN MIS devices. On the other hand, for $x/(x+y) = 0.84$ with $d_{ins} < 26$ nm and $x/(x+y) = 0.73$ with $d_{ins} > 12$ nm, we obtain $V_{th} > 0$, normally-off operations for AlTiO/AlGaN/GaN MIS devices, where a positive V_{th}-d_{ins} slope is observed for $x/(x+y) = 0.73$. From the fitting using the relation (1), we can directly obtain $\sigma_{GaN} - \sigma_{ins}$. It should be noted that, in order to evaluate σ_{ins}, the value of σ_{GaN} is required. Here, assuming $\sigma_{GaN}/q = 2.1 \times 10^{13}$ cm^{-2},[46–50] we evaluate σ_{ins} at the AlTiO/AlGaN interface for the non-recessed and recessed areas, as summarized in Fig. 4, where the error bars show the three-sigma asymptotic standard errors in the fitting, and the neutral interface is indicated by the black dotted line. While there was little effect of the post-gate annealing for the non-recessed area, the post-gate annealing decreased the positive interface fixed

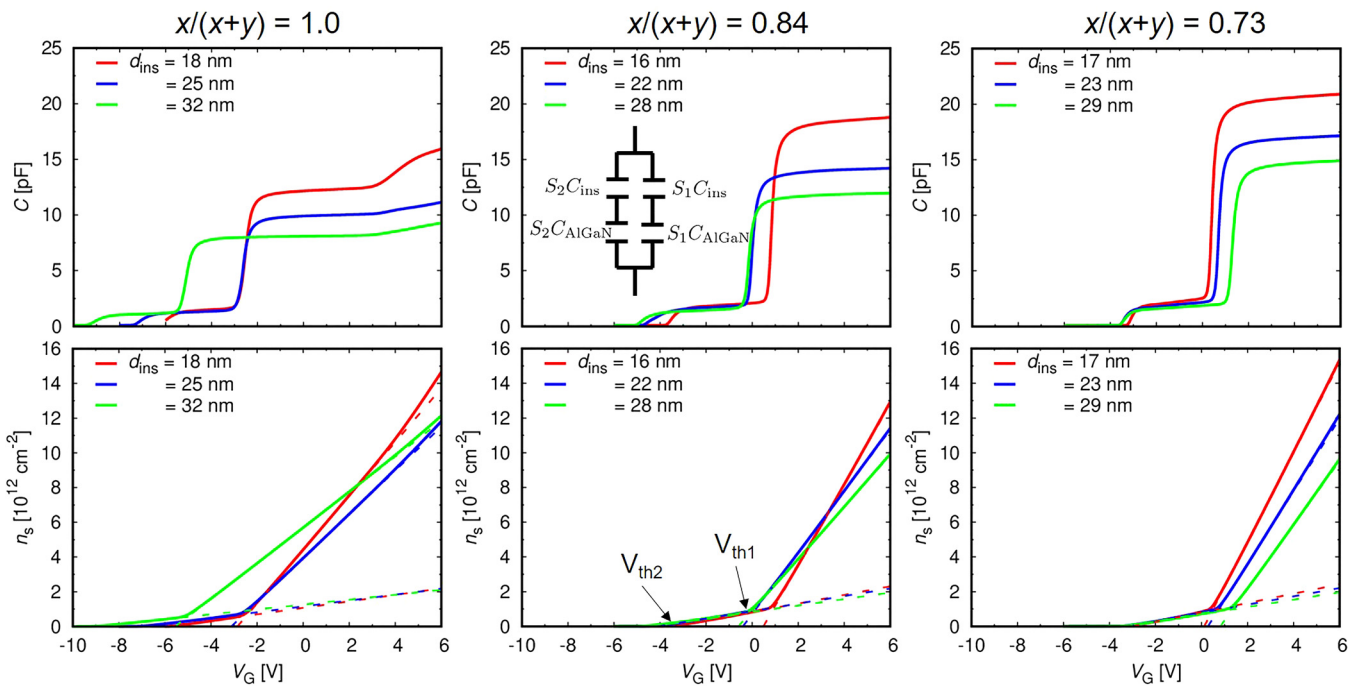

FIG. 2. C-V_G characteristics of the partially-recessed AlTiO/AlGaN/GaN MIS-capacitors at 1 MHz. The inset shows the equivalent circuit of the devices. The 2DEG sheet concentration n_S under the gate is obtained by integration of C as a function of V_G, from which the threshold voltages of non-recessed area (V_{th2}) and recessed area (V_{th1}) are determined.

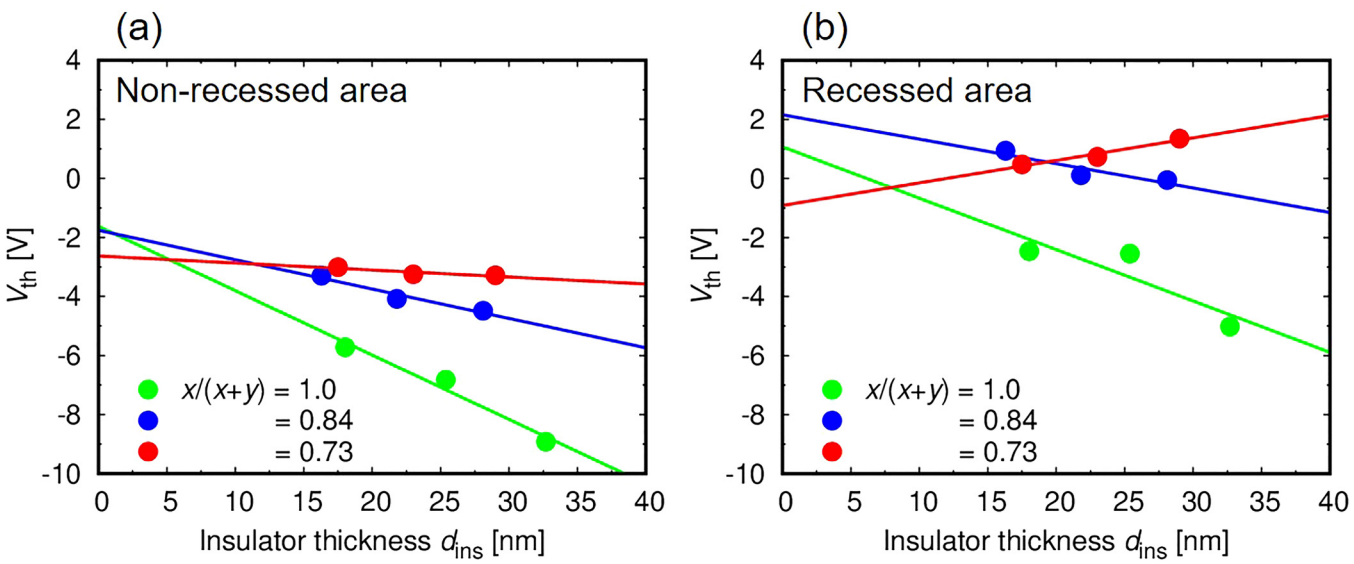

FIG. 3. The threshold voltage V_{th} for the (a) non-recessed and (b) recessed areas of the AlTiO/AlGaN/GaN MIS-capacitors as functions of d_{ins}.

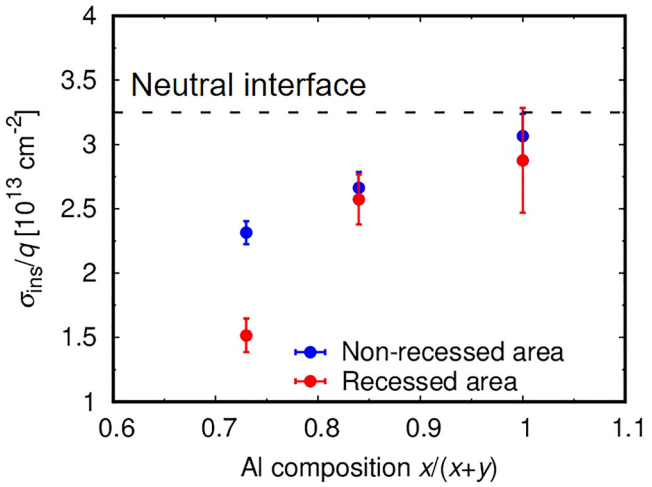

FIG. 4. The AlTiO/AlGaN interface fixed charge density σ_{ins} as functions of the Al composition of the AlTiO for the non-recessed and recessed areas. The error bars show the three-sigma asymptotic standard errors in the fitting. The neutral interface is indicated by the black dotted line.

charge in the recessed area by the order of mid 10^{12} cm^{-2}, similarly to Ref. 39. For the non-recessed AlGaN area, as reported in Ref. 11, AlTiO with low Al compositions can suppress the AlTiO/AlGaN interface fixed charge σ_{ins}. Moreover, it is found that σ_{ins} is further suppressed for the recessed AlGaN area. Considering the fact that σ_{ins} is the sum of positive and negative fixed charges (excluding the negative polarization charge) at the interface, the further suppression of σ_{ins} might be attributed to a negative charge introduced by the gate recess process. For the $x/(x+y) = 0.73$ composition, we observe a rather low σ_{ins} leading to the positive V_{th}-d_{ins} slope; although the mechanism is not elucidated, one possibility is that the interaction between the AlTiO and the recessed AlGaN depends on the AlTiO composition, affecting the interface fixed charge. The positive slope is useful for fabricating normally-off devices, since more positive threshold voltages can be obtained by increasing the insulator thickness.

Figure 5 shows calculated 1D Poisson-Schrödinger band diagrams of the partially-recessed AlTiO/AlGaN/GaN MIS structures with $d_{AlGaN} = 4$ nm and $d_{ins} = 30$ nm at $V_G = 0$ V, using σ_{ins} obtained by the experimental results. For the calculation, we determined the AlTiO-AlGaN conduction band offset φ and the metal-AlTiO barrier height ϕ as follows. Using the electron affinities ~ 1.9 eV of ALD-deposited Al_2O_3[51] and ~ 4.0 eV of ALD-deposited TiO_2,[52] we employed a linear approximation of the electron affinity $\sim [4.0 - 2.1x/(x+y)]$ eV of Al_xTi_yO. Assuming no vacuum level discontinuity at the AlTiO/AlGaN, the AlGaN electron affinity ~ 3.5 eV leads to an estimated AlTiO-AlGaN conduction band offset $\varphi \simeq [2.1x/(x+y) - 0.5]$ eV. On the other hand, from the intercept of the V_{th}-d_{ins} relation given by (1), we experimentally obtained $\phi - \varphi$, which gives the metal-AlTiO barrier height ϕ in combination with the above-estimated φ, where we obtain $\phi = (4.6 \pm 0.5)$ eV for $x/(x+y) = 1.0$, $\phi = (1.5 \pm 0.4)$ eV for $x/(x+y) = 0.84$, and $\phi = (1.6 \pm 0.2)$ eV for $x/(x+y) = 0.73$, including the three-sigma asymptotic standard errors in the fitting. The metal-AlTiO barrier heights ϕ for $x/(x+y) = 0.84$ and 0.73 are rather small in comparison with that for $x/(x+y) = 1.0$.

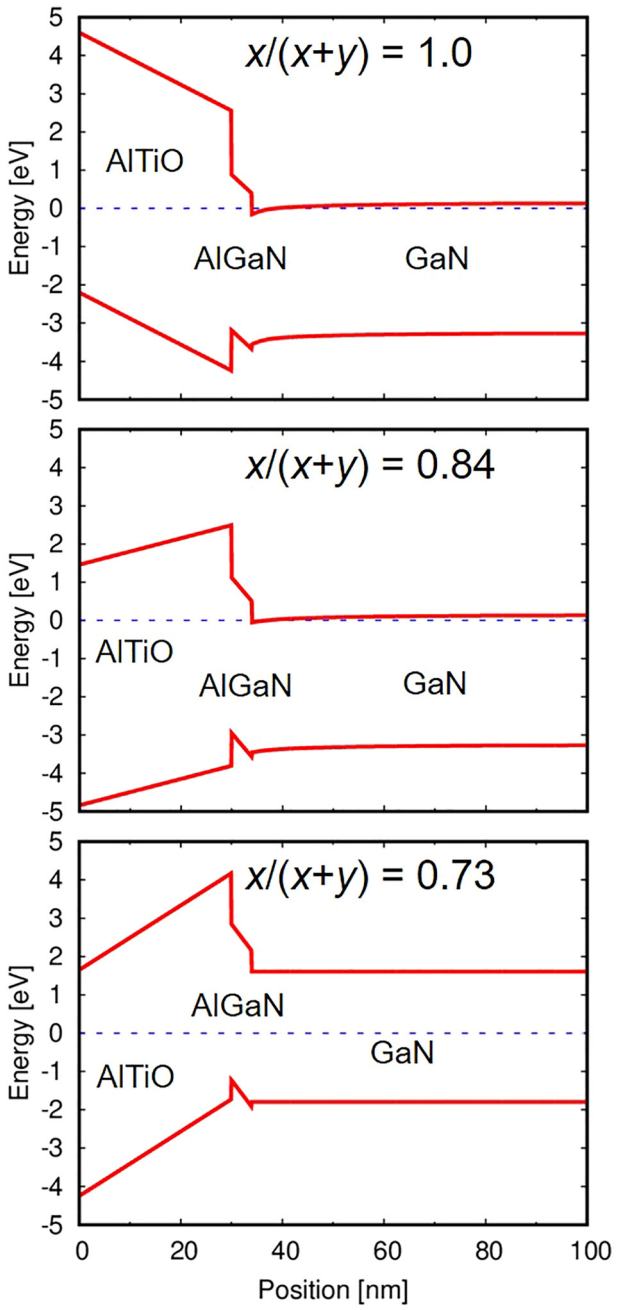

FIG. 5. Calculated 1D Poisson-Schrödinger band diagrams of the partially-recessed AlTiO/AlGaN/GaN MIS structures with $d_{AlGaN} = 4$ nm and $d_{ins} = 30$ nm at $V_G = 0$ V, using experimentally obtained σ_{ins}.

Although the average value of ϕ for $x/(x+y) = 0.84$ is slightly smaller than that for $x/(x+y) = 0.73$, they are similar and within error. We find that the decrease in the interface fixed charge density can reverse the direction of the electric fields in the AlTiO insulators for the $x/(x+y) = 0.84$ and 0.73 compositions. The larger the decrease in σ_{ins} is, the stronger the electric field is in AlTiO, shifting the threshold voltages positively. As a result, while $V_{th} < 0$ V for $x/(x+y) = 1.0$ and $V_{th} \lesssim 0$ V for $x/(x+y) = 0.84$, a clear normally-off operation $V_{th} > 0$ V is indicated for $x/(x+y) = 0.73$.

In order to examine the normally-off operation, we characterized a partially-recessed AlTiO/AlGaN/GaN MIS-FET for $x/(x+y) = 0.73$, where $d_{AlGaN} \sim 4$ nm and $d_{ins} = 29$ nm. The output and transfer device characteristics are depicted in Fig. 6, showing the drain current I_D, the gate current I_G, and the transconductance g_m normalized by the channel width. Figure 6(a) shows the transfer characteristics at $V_D = 10$ V, exhibiting a clear normally-off operation with a low leakage current, a high on/off current ratio $\sim 10^{10}$, and the maximum of $g_m \simeq 80$ mS/mm. The threshold voltage is estimated to be 1.7 V by linear fitting of I_D as a function of V_G shown in Fig. 6(b), being consistent with the estimation from the C-V_G characteristics. Since there is almost no hysteresis for positive voltage applications in the range of $V_G \leq +10$ V, we show the transfer characteristics for a voltage sweep for $V_G = +10 \rightarrow -6$ V. On the other hand, the negative voltage application down to $V_G = -6$ V leads to a negative threshold voltage shift of $\lesssim 0.5$ V. The output characteristics shown in Fig. 6(c) exhibits I_D as high as ~ 450 mA/mm, and a low on-resistance of 9.5 Ω mm.

Figure 7 shows the sub-threshold swing $SS = [\partial(\log I_D)/\partial V_G]^{-1}$ as functions of I_D for $V_D = 1$, 3, and 10 V. We observe excellent sub-threshold characteristics with the minimum $SS \sim 65$ mV/decade, which approaches the theoretical limit (60 mV/decade, plotted as the black dotted line) for a wide range of I_D.

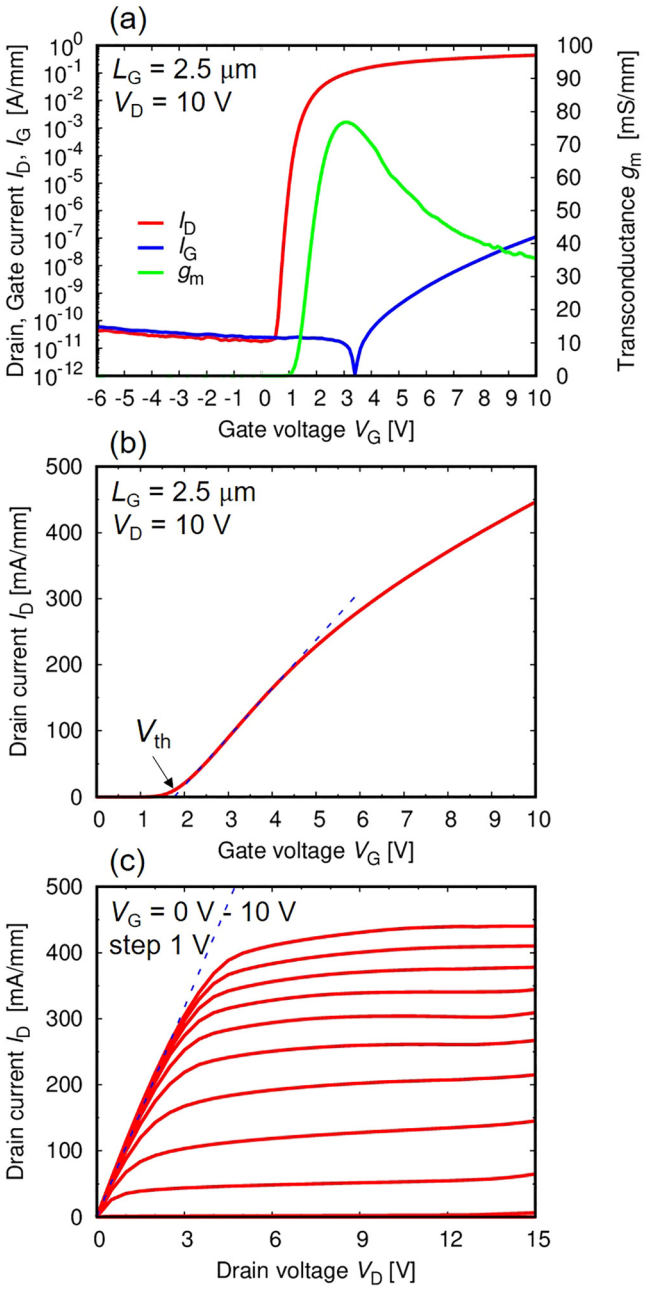

FIG. 6. Device characteristics of a partially-recessed AlTiO/AlGaN/GaN MIS-FET. (a) and (b) The transfer characteristics at $V_D = 10$ V. (c) The output characteristics.

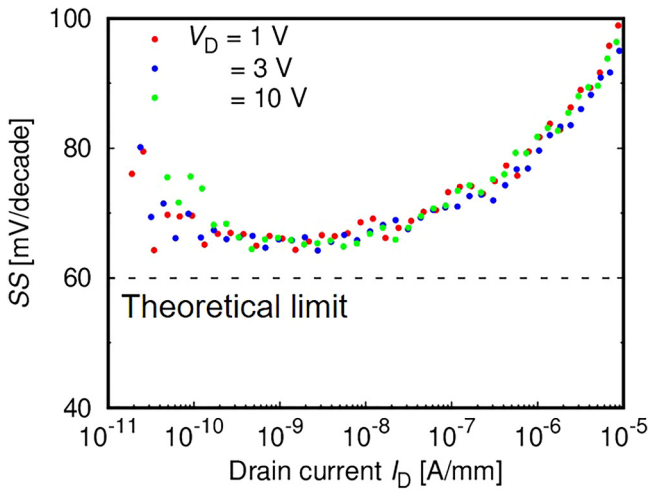

FIG. 7. The sub-threshold swing $SS = [\partial(\log I_D)/\partial V_G]^{-1}$ as functions of I_D for $V_D = 1$, 3, and 10 V; the black dotted line shows the theoretical limit 60 mV/decade.

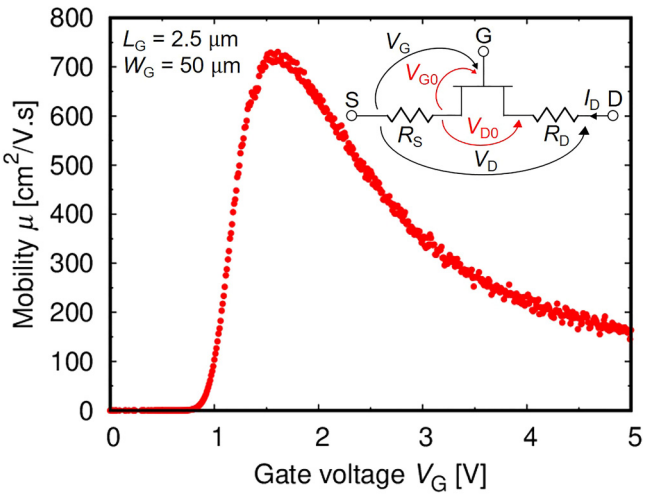

FIG. 8. The channel field mobility μ under the recessed gate as a function of V_G for $V_D \leq 0.1$ V, where the inset shows a FET equivalent circuit.

The FET channel field mobility under the gate is usually calculated by

$$\mu = \frac{L_G}{CV_D}\frac{\partial I_D}{\partial V_G}. \tag{4}$$

However, based on a FET equivalent circuit shown in the inset of Fig. 8, the effects of the source resistance R_S and the drain resistance R_D must be taken into account. The channel field mobility under the gate should be obtained by

$$\mu = \frac{L_G}{CV_{D0}}\frac{\partial I_D}{\partial V_{G0}}, \tag{5}$$

where $V_{D0} = V_D - I_D(R_S + R_D)$ and $V_{G0} = V_G - I_D R_S$. The source resistance R_S and the drain resistance R_D are calculated from the contact resistance R_C and the sheet resistance ρ_{Sh} for the non-recessed area, by using

$$\begin{cases} R_S = R_C + \rho_{Sh} \times L_{GS}, \\ R_D = R_C + \rho_{Sh} \times L_{GD}, \end{cases} \tag{6}$$

where L_{GS} and L_{GD} are the gate-source and gate-drain distance, respectively. From separate transfer length method (transmission-line model) measurements, we estimated $R_C \simeq 1.2\,\Omega$ mm and $\rho_{Sh} \sim 900\,\Omega/\square$ for the non-recessed area. Thus, as shown in Fig. 8, we obtain the channel field mobility μ under the recessed gate as a function of V_G for $V_D \leq 0.1$ V. We observe a maximum $\mu \simeq 730\,\text{cm}^2/\text{V s}$, which is rather high as a channel field mobility of gate-recessed GaN-based MIS-FETs.[53] However, we observe a decrease in μ-V_G and g_m-V_G relations for high V_G, which can be attributed to interface states impeding the gate-control efficiency.[18] Further works are necessary to suppress such interface states and improve the linearity of the transconductance.

IV. CONCLUSION

We investigated combining the interface charge engineering using Al_xTi_yO gate insulators with a partial gate recess method for AlGaN/GaN MIS-FETs. For a composition of $x/(x+y) = 0.73$, we successfully obtained normally-off operations in the partially-gate-recessed AlTiO/AlGaN/GaN MIS devices with a $\sim$4 nm-thick remaining AlGaN layer, which thickness leads to normally-on operations for Al_2O_3/AlGaN/GaN MIS devices. The normally-off AlTiO/AlGaN/GaN MIS-FETs show favorable performances, such as a threshold voltage of 1.7 V, an on-resistance of 9.5 Ω mm, an output current of 450 mA/mm, a low sub-threshold swing of 65 mV/decade, and a rather high electron mobility of 730 $\text{cm}^2/\text{V s}$. We conclude that combining the interface charge engineering with a partial gate recess method is advantageous toward normally-off operations in AlGaN/GaN MIS devices to achieve high threshold voltages, low on-resistances, and high output currents.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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