Semiconductor Science and Technology

Low-frequency noise in AlTiO/AlGaN/GaN metal-insulator-semiconductor field-effect transistors with non-gate-recessed or partially-gate-recessed structures

To cite this article before publication: Duong Dai Nguyen *et al* 2023 *Semicond. Sci. Technol.* in press https://doi.org/10.1088/1361-6641/acec64

Low-frequency noise in AlTiO/AlGaN/GaN metal-insulator-semiconductor field-effect transistors with non-gate-recessed or partially-gate-recessed structures

Duong Dai Nguyen, Yuchen Deng, and Toshi-kazu Suzuki*

Center for Nano Materials and Technology,

Japan Advanced Institute of Science and Technology (JAIST),

1-1 Asahidai, Nomi, Ishikawa 923-1292, JAPAN

(Dated: July 14, 2023)

Abstract

We have systematically investigated low-frequency noise (LFN) in AlTiO/AlGaN/GaN metal-insulator-semiconductor field-effect transistors (MIS-FETs) with non-gate-recessed or partially-gate-recessed structures, where gate insulators using AlTiO, an alloy of Al_2O_3 and TiO_2, are obtained by atomic layer deposition. For drain current LFN, we find pure $1/f$ spectra for the well-above-threshold regime, and superposition of $1/f$ and Lorentzian spectra near the threshold voltage. The Hooge parameters are evaluated from the $1/f$ contribution and found to be independent of the AlTiO thickness. However, the remaining AlGaN thickness strongly affects the Hooge parameter near the threshold voltage; in the low channel electron concentration regime of the partially-gate-recessed FETs, a smaller remaining AlGaN thickness gives a larger Hooge parameter proportional to the inverse of the electron concentration, indicating that channel electron number fluctuation dominates the Hooge parameter. We consider that the channel electron number fluctuation is caused by electron traps introduced by the recess etching process in the remaining AlGaN. On the other hand, the Lorentzian spectra give specific time constants almost independent of the AlTiO thickness and the remaining AlGaN thickness, corresponding to trap depths of 0.6-0.8 eV. This can be attributed to traps in AlTiO near the AlTiO/AlGaN interface.

* Author to whom correspondence should be addressed; electronic mail: tosikazu@jaist.ac.jp

I. INTRODUCTION

For high-speed and high-power applications, GaN-based metal-insulator-semiconductor field-effect transistors (MIS-FETs) have been extensively investigated using various gate insulators, such as high-dielectric-constant (high-k) oxides Al_2O_3 [1], HfO_2 [2, 3], TiO_2 [4], AlSiO [5, 6], AlTiO [7–12], high-k oxynitrides TaON [13], AlON [14], and high-k nitrides BN [15, 16], AlN [17–21]. In particular, Al_xTi_yO (AlTiO), an alloy of Al_2O_3 and TiO_2, is an important insulator, because it can be applied to dielectric constant engineering, energy gap engineering, and interface charge engineering [11]. Previously, we reported normally-off operations in partially-gate-recessed AlTiO/AlGaN/GaN MIS-FETs using gate insulators AlTiO with a rather thick remaining AlGaN thickness [12]. However, for gate-recessed AlGaN/GaN MIS-FETs, in addition to the problem of device instability [22, 23], low-frequency noise (LFN) will be enhanced [24–28], influenced by the insulator itself and the insulator/etched-semiconductor interface. Although several studies have shown that enhancement in LFN is ascribed to the channel mobility degradation/fluctuation in the partially-gate-recessed [24] and the fully-gate-recessed AlGaN/GaN MIS-FETs [25–28], the underlying physics is not clear. Moreover, in addition to $1/f$ LFN spectra [21, 29–34], Lorentzian LFN spectra are sometimes observed [7, 35–41], which are strongly related to the insulator materials and the device fabrication processes. Thus, LFN characterization is an important diagnosis for gate-recessed AlGaN/GaN MIS-FETs.

In this study, we systematically investigated LFN in AlTiO/AlGaN/GaN MIS-FETs with non-gate-recessed or partially-gate-recessed structures, using an Al_xTi_yO ($x/(x+y) = 0.73$, energy gap $E_g \sim 6$ eV, dielectric constant $k \sim 14$) gate insulator obtained by atomic layer deposition (ALD) [7, 9, 11, 12]. For drain current LFN, we find pure $1/f$ spectra for the well-above-threshold regime, and superposition of $1/f$ and Lorentzian spectra near the threshold voltage. The Hooge parameters are evaluated from the $1/f$ contribution and found to be independent of the AlTiO thickness. However, the remaining AlGaN thickness strongly affects the Hooge parameter near the threshold voltage; in the low channel electron concentration regime of the partially-gate-recessed FETs, a smaller remaining AlGaN thickness gives a larger Hooge parameter. We consider that this is owing to electron traps introduced by the recess etching process in the remaining AlGaN. On the other hand, the Lorentzian spectra give specific time constants almost independent of the AlTiO thickness and the remaining

AlGaN thickness, corresponding to trap depths of 0.6-0.8 eV. Since the gate leakage currents are dominated by Poole-Frenkel mechanism due to traps with the similar depth in AlTiO, we consider that the Lorentzian spectra are attributed to traps in AlTiO near the AlTiO/AlGaN interface.

II. DEVICE FABRICATION AND CHARACTERISTICS

The fabrication of the non-gate-recessed and partially-gate-recessed AlTiO/AlGaN/GaN MIS devices, MIS-FETs and MIS-capacitors, started from an $Al_{0.24}Ga_{0.76}N$ (20 nm)/GaN(3 μm) heterostructure on sapphire(0001), followed by Ti/Al/Ti/Au Ohmic electrode formation. For gate recess process, the AlGaN layer was etched by using electron cyclotron resonance nitrogen plasma, with the radio frequency power of 100 W, the acceleration voltage of 100 V, and the ion beam current density of 0.3 mA/cm^2. The etching rate was $\simeq$ 1.2 nm/minute and the etching depths were $\simeq$ 9 nm and $\simeq$ 15 nm (i.e., the remaining AlGaN thickness $d_{\rm AlGaN} \simeq 11$ nm and $\simeq 5$ nm, respectively), as measured by atomic force microscopy. After etched-AlGaN surface cleaning by acetone, methanol, oxygen plasma ashing, and a TMAH-diluted solution to remove oxide and oxygen-related molecules, Al_xTi_yO ($x/(x+y) = 0.73$, $E_{\rm g} \sim 6$ eV, $k \sim 14$) gate insulators with several thicknesses ($d_{\rm AlTiO} = 26, 18$, and 11 nm) were formed by ALD at 130 °C using TMA (trimethylaluminum), TDMAT (tetrakis-dimethylamino titanium), and water [7, 9, 11, 12], followed by post-deposition annealing at 350 °C in H_2-mixed Ar. After necessary device isolation by B^+ ion implantation, Ni/Au gate electrodes were formed. Finally, post-gate annealing at 400 °C in N_2 completed the device fabrication. Figure 1(a) and (b) show the device dimension of the non-recessed and partially-recessed MIS-FETs, respectively. In the latter, the recessed gate of length $L_{\rm RG} = 2$ μm is overlapped by the total gate of length $L_{\rm G} = 2.5$ μm. The source-drain distance is 5 μm, and the gate width is $W = 50$ μm. Figure 1(c) and (d) show the device dimension of the non-recessed and partially-recessed MIS-capacitors, respectively, where the recessed area $S_{\rm RG} = 70^2$ μm^2 is overlapped by the total gate area $S_{\rm G} = 75^2$ μm^2, which is surrounded by the Ohmic electrodes.

Basic characteristics were obtained for each device. Figure 2(a) and (b) are output and transfer characteristics for a non-recessed FET ($d_{\rm AlGaN} = 20$ nm, $d_{\rm AlTiO} = 26$ nm), respectively, where $I_{\rm D}$ is the drain current, $I_{\rm G}$ is the gate current, and $g_{\rm m}$ is the transconductance,

which are normalized by the gate width W and shown on the vertical axes. Fig. 2(c) and (d) are for a partially-recessed FET ($d_{\mathrm{AlGaN}} \simeq 11$ nm, $d_{\mathrm{AlTiO}} = 26$ nm). Figure 3(a) and (b) show capacitance-voltage (C-V) characteristics at 1 MHz of a non-recessed capacitor ($d_{\mathrm{AlGaN}} = 20$ nm, $d_{\mathrm{AlTiO}} = 26$ nm) and a partially-recessed capacitor ($d_{\mathrm{AlGaN}} \simeq 11$ nm, $d_{\mathrm{AlTiO}} = 26$ nm), respectively. The total electron number N under the gate is calculated by integration of C as a function of V_{G}, which is plotted in the same figure. The threshold voltage V_{th} can be determined by the N-V_{G} relation. For the non-recessed capacitors, V_{th} is determined by simple linear fitting with $qN \simeq C(V_{\mathrm{G}} - V_{\mathrm{th}})$ (q: the electron charge) for $V_{\mathrm{G}} > V_{\mathrm{th}}$ as in Fig. 3(a). On the other hand, since the recessed capacitors have the recessed area with the threshold voltage V_{th} and the non-recessed area with the threshold voltage $V_{\mathrm{th0}} < V_{\mathrm{th}}$, we obtain two lines $qN \simeq C_{\mathrm{nr}}(V_{\mathrm{G}} - V_{\mathrm{th0}})$ for $V_{\mathrm{th0}} < V_{\mathrm{G}} < V_{\mathrm{th}}$ and $qN \simeq C_{\mathrm{nr}}(V_{\mathrm{G}} - V_{\mathrm{th0}}) + C_{\mathrm{r}}(V_{\mathrm{G}} - V_{\mathrm{th}})$ for $V_{\mathrm{G}} > V_{\mathrm{th}}$ as in Fig. 3(b). Thus, the recessed device threshold voltage V_{th} is determined by the intersection point of the two lines [12].

III. LOW-FREQUENCY NOISE CHARACTERIZATION

The LFN measurement system consists of a shielded chamber for probe station, a battery-driven low-noise preamplifier (LNA, Stanford SR570), a dynamic signal analyzer (Agilent 35670A), and an RC passive low-pass filter (LPF). For measuring LFN in the MIS-FETs, the source is grounded, the drain is applied with a DC bias voltage and a DC offset current by the battery-driven LNA, and the gate is connected to a parameter analyzer through the LPF with a cut-off frequency ~ 0.05 Hz to eliminate the noise from the parameter analyzer [7, 21, 42]. The schematic of the LFN measurement setup is shown in Fig. 4. We measured LFN for each AlTiO/AlGaN/GaN MIS-FET in the linear regime for a frequency range $f = 0.1$-10^3 Hz. In Fig. 5, we show examples of the measurement results of the drain current noise power spectral density (PSD) normalized by the drain current square, $S_{I_{\mathrm{D}}}/I_{\mathrm{D}}^2$. In the well-above-threshold regime $V_{\mathrm{G}} - V_{\mathrm{th}} \gtrsim 3$ V, pure $1/f$ LFN spectra [43]

$$\frac{S_{I_{\mathrm{D}}}}{I_{\mathrm{D}}^2} = \frac{A}{f} \tag{1}$$

are observed, where A is a prefactor. On the other hand, near the threshold voltage, we find superposition of $1/f$ and Lorentzian spectra given by

$$\frac{S_{I_{\mathrm{D}}}}{I_{\mathrm{D}}^2} = \frac{A}{f} + \frac{B}{1 + (2\pi\tau f)^2}, \tag{2}$$

where B is a prefactor and τ is a time constant for the Lorentzian spectra. Since A and B respectively characterize the intensity of $1/f$ and Lorentzian noise, it is important to extract them from the measured spectra. We carried out fitting of $S_{I_\mathrm{D}}/I_\mathrm{D}^2$ using Eq. (2), which includes Eq. (1) as a special case of $B = 0$. Figure 6 shows examples of the fitting, where a current PSD in the well-above threshold regime is fitted by Eq. (2) with $B \simeq 0$, whereas a current PSD near the threshold voltage is well-fitted by Eq. (2) with $B \neq 0$.

From the fittings, we obtain A for all the spectra. In order to analyze A, we should consider the contributions from each region of the FETs. The on-resistance R_on for the non-recessed FETs is given by

$$R_\mathrm{on} = 2R_\mathrm{c} + R_\mathrm{ac} + R_\mathrm{nr} = R_\mathrm{ext} + R_\mathrm{nr}, \tag{3}$$

where R_c is the Ohmic contact resistance, R_ac is the resistance of the access region (total length $L_\mathrm{ac} = 2.5$ μm), R_nr is the resistance of the non-recessed gated region (length $L_\mathrm{G} = 2.5$ μm). For the partially-recessed FETs, the on-resistance is given by

$$R_\mathrm{on} = 2R_\mathrm{c} + R_\mathrm{ac} + \tilde{R}_\mathrm{nr} + R_\mathrm{r} = R_\mathrm{ext} + \tilde{R}_\mathrm{nr} + R_\mathrm{r}, \tag{4}$$

where $\tilde{R}_\mathrm{nr}$ is the resistance of the non-recessed gated region (total length $L_\mathrm{G} - L_\mathrm{RG} = 0.5$ μm) and R_r is the resistance of the partially-recessed gated region (length $L_\mathrm{RG} = 2$ μm). As a result, we obtain

$$\begin{aligned} A &= A_\mathrm{ext}\frac{R_\mathrm{ext}^2}{R_\mathrm{on}^2} + A_\mathrm{nr}\frac{R_\mathrm{nr}^2}{R_\mathrm{on}^2} && \text{(non-recessed FET)} \\ A &= A_\mathrm{ext}\frac{R_\mathrm{ext}^2}{R_\mathrm{on}^2} + \tilde{A}_\mathrm{nr}\frac{\tilde{R}_\mathrm{nr}^2}{R_\mathrm{on}^2} + A_\mathrm{r}\frac{R_\mathrm{r}^2}{R_\mathrm{on}^2} && \text{(partially-recessed FET).} \end{aligned} \tag{5}$$

A_ext is the factor for the PSD generated by the external region, the Ohmic contact resistance and the access region, which is independent of V_G. A_nr is the factor for the non-recessed gated region depending on V_G for the non-recessed FETs. $\tilde{A}_\mathrm{nr}$ and A_r are the factors for the non-recessed gated and the recessed gated regions for the partially-recessed FETs, respectively, which also depend on V_G. In order to determine the external factor A_ext, we measured LFN in the ungated non-recessed two-terminal devices, whose structure is shown in the inset of Fig. 7(a). Figure 7(b) shows $A_\mathrm{ext} = S_I f/I^2$ as a function of the access length L, where A_ext can be fitted with a decreasing function of L as in the previous report [21], because

$$A_\mathrm{ext} = 2A_\mathrm{c}\frac{R_\mathrm{c}^2}{R_\mathrm{ext}^2} + A_\mathrm{ac}\frac{R_\mathrm{ac}^2}{R_\mathrm{ext}^2} = \frac{2A_\mathrm{c}R_\mathrm{c}^2 + A_\mathrm{ac}R_\mathrm{ac}^2}{(2R_\mathrm{c} + R_\mathrm{ac})^2} \tag{6}$$

holds and the L dependence comes from $R_{\rm ac} \propto L$ and $A_{\rm ac} \propto 1/L$ (inversely proportional to the system size). For our FETs, since the access length is $L_{\rm ac} = 2.5$ μm, we obtain $A_{\rm ext} \simeq 4 \times 10^{-11}$, from which we can determine $A_{\rm nr}$ depending on $V_{\rm G}$ for the non-recessed FETs. Additionally, the length of non-recessed gated region in the partially-recessed FETs is $L_{\rm G} - L_{\rm RG} = 0.5$ μm, which is one-fifth of the length of non-recessed gated region in the non-recessed FETs ($L_{\rm G} = 2.5$ μm). Hence, we obtain $\tilde{R}_{\rm nr} = R_{\rm nr}/5$ and $\tilde{A}_{\rm nr} = 5A_{\rm nr}$. As a result, we can extract $A_{\rm r}$. In Fig. 8, $A_{\rm nr}$ and $A_{\rm r}$ are plotted as functions of $V_{\rm G} - V_{\rm th}$. We find that $A_{\rm nr}$ and $A_{\rm r}$ increase for low $V_{\rm G} - V_{\rm th}$, and approach constants at higher $V_{\rm G} - V_{\rm th}$.

The effective Hooge parameters $\alpha_{\rm H}$ in the intrinsic region can be evaluated by [43]

$$\begin{aligned} \alpha_{\rm H} &= A_{\rm nr} N = A_{\rm nr} n_{\rm s} L_{\rm G} W \qquad \text{(non-recessed FET)} \\ \alpha_{\rm H} &= A_{\rm r} N = A_{\rm r} n_{\rm s} L_{\rm RG} W \qquad \text{(partially-recessed FET)}, \end{aligned} \tag{7}$$

where $n_{\rm s}$ is the sheet electron concentration in the intrinsic region, which can be calculated from the electron number obtained by the C-V characteristics. Figure 9(a) and (b) plot $\alpha_{\rm H}$ as functions of $V_{\rm G} - V_{\rm th}$ for the non-recessed FETs and the partially-recessed FETs. We find that $\alpha_{\rm H}$ is independent of the AlTiO thickness but strongly dependent of the remaining AlGaN layer; a smaller $d_{\rm AlGaN}$ gives a larger $\alpha_{\rm H}$, although $\alpha_{\rm H}$ seems to approach the same constant at high $V_{\rm G} - V_{\rm th}$. We evaluate $\alpha_{\rm H}$ as a function of $n_{\rm s}$ for each FET in Fig. 10. We find that for $n_{\rm s} \lesssim 2 \times 10^{12}$ cm^{-2}, $\alpha_{\rm H} \propto n_{\rm s}^{-1}$ for the partially-recessed FETs, whereas $\alpha_{\rm H}$ is weakly dependent on $n_{\rm s}$ for the non-recessed FETs. The behavior of $\alpha_{\rm H} \propto n_{\rm s}^{-1}$ was observed for example in Schottky FETs [44], and can be attributed to the electron number fluctuation caused by electron traps. The trap density D_0 can be estimated by the relation [21, 43, 45]

$$\alpha_{\rm H} \simeq \frac{k_{\rm B} T D_0}{n_{\rm s} \ln(f_{\rm h}/f_{\rm l})}, \tag{8}$$

where $f_{\rm l}$ and $f_{\rm h}$ are the lower and higher limits of the $1/f$ spectrum, respectively. Thus, we obtain $D_0 \sim 3 \times 10^{11}$ and $\sim 5 \times 10^{10}$ cm^{-2} eV^{-1} for the partially-recessed FETs with $d_{\rm AlGaN} \simeq 5$ and $\simeq 11$ nm, respectively. We consider that the recess etching process may introduce electron traps in the AlGaN layer, the longer the etching process is carried out, the smaller the remaining AlGaN thickness is, and the higher the trap density becomes. This might also explain the weak dependence of $\alpha_{\rm H}$ on $n_{\rm s}$ for the non-recessed FETs, since the trap density is too low to have a pronounced effect as observed in the partially-recessed FETs. On the other hand, at high $n_{\rm s}$, we observe a strong, universal increase in $\alpha_{\rm H}$ for all

the FETs, which can be attributed to the fluctuation in the intrinsic gate voltage through the extrinsic source resistance [21].

In general, Lorentzian LFN strongly depends on the gate insulator quality, such as traps [7, 21]. In the present case, from the fittings, we obtain the prefactor B and the time constant τ in Eq. (2) for all the FETs as shown in Fig. 11, where B and τ are plotted as functions of $V_{\rm G} - V_{\rm th}$. It seems that B is almost independent of the AlTiO thickness and the remaining AlGaN thickness. Furthermore, B rapidly decreases with increase in $V_{\rm G} - V_{\rm th}$ and becomes negligible in the well-above threshold regime. The extracted specific time constant, $\tau \sim 0.5$ s, seems to be almost independent of $V_{\rm G} - V_{\rm th}$, the AlTiO thickness, and the remaining AlGaN thickness. The time constant τ corresponds to a trap level depth $E_{\rm a}$ via

$$\tau = \frac{1}{\sigma_{\rm e} N_{\rm c} v_{\rm th}} e^{E_{\rm a}/k_{\rm B}T}, \tag{9}$$

where $\sigma_{\rm e}$ is the electron capture cross-section, $N_{\rm c}$ is the effective density of states in the conduction band, $v_{\rm th}$ is the electron thermal velocity, and $k_{\rm B}$ is the Boltzmann constant. We assume $\sigma_{\rm e} = 10^{-16}$-$10^{-14}$ cm^2 for the traps in AlTiO; this is reasonable since ALD Al_2O_3 shows similar $\sigma_{\rm e}$ [46], while much smaller $\sigma_{\rm e}$ was observed in SiN [47]. An electron effective mass should be between $m^* = 0.3m_{\rm e}$ for Al_2O_3 [48] and $m^* = 30m_{\rm e}$ for TiO_2 [49]. Thus, the trap depth can be estimated to be $E_{\rm a} \simeq 0.6$-0.8 eV. The fact that B and τ are almost independent of the remaining AlGaN thickness and the AlTiO thickness suggests that the Lorentzian spectra are attributed to traps in AlTiO near the AlTiO/AlGaN interface.

IV. COMPARISON WITH POOLE-FRENKEL CURRENTS

Since the Poole-Frenkel analysis is effective to examine the traps in AlTiO, we investigated gate leakage currents of the MIS capacitors. Figure 12(a) and (b) show the gate leakage current density J as a function of $V_{\rm G}$ at reverse bias at $T = 300$-400 K for a non-recessed capacitor ($d_{\rm AlGaN} = 20$ nm, $d_{\rm AlTiO} = 26$ nm) and a partially-recessed capacitor, ($d_{\rm AlGaN} \simeq 11$ nm, $d_{\rm AlTiO} = 26$ nm), respectively. Leakage dominated by the Poole-Frenkel mechanism is given by [50]

$$\frac{J}{F} = De^{-\beta\phi} e^{\beta\sqrt{q^3F/(\pi\kappa\epsilon_0)}}, \tag{10}$$

where F is the electric field in the AlTiO insulators, $\beta = 1/k_{\rm B}T$, D is a constant, ϕ is the trap level depth in the AlTiO, κ is related to the dielectric constant, and ϵ_0 is the vacuum

permittivity. The electric field can be evaluated by [7]

$$F = \frac{\Delta\sigma_{\rm ins} - qn_{\rm s}}{k_{\rm AlTiO}\epsilon_0}, \tag{11}$$

where $\Delta\sigma_{\rm ins} = \sigma_{\rm ins} - \sigma_{\rm GaN}$ is the difference between the fixed charge density $\sigma_{\rm ins}$ at AlTiO/AlGaN interface and the GaN polarization charge density $\sigma_{\rm GaN}$, and $k_{\rm AlTiO}$ is the insulator dielectric constant. Based on measurements of MIS capacitors with several insulator thicknesses and 1D Poisson-Schrödinger calculation [9, 11, 12], we find that $\Delta\sigma_{\rm ins} \simeq 4\times10^{12}$ and 2×10^{12} cm^2 for the non-recessed and partially-recessed capacitors, respectively. Figure 13(a) and (b) show J/F-$\sqrt{F}$ relations for the non-recessed and partially-recessed capacitors, respectively, exhibiting the leakage dominated by the Poole-Frenkel mechanism according to Eq. (10) in the high field regime. From the fittings, we obtain $D\exp(-\beta\phi)$ as a function of $1/T$, which is plotted in Fig. 13(c). The trap level depth in the AlTiO insulator is extracted to be $\phi \simeq 0.6$ eV, which is independent of the remaining AlGaN thickness as expected, and similar to the one obtained from the Lorentzian spectra. This suggests that the traps in the AlTiO insulator are responsible for the Lorentzian LFN and the Poole-Frenkel mechanism. It should be noted that the Poole-Frenkel mechanism is caused by the whole of the bulk traps in the AlTiO insulator. On the other hand, since the Lorentzian noise is not influenced by the AlTiO thickness and the electric field or the gate voltage, we consider that the traps in AlTiO contributing the Lorentzian noise are those near the AlTiO/AlGaN interface, where the trap density might be high.

V. CONCLUSION

We investigated LFN in AlTiO/AlGaN/GaN MIS-FETs with non-gate-recessed or partially-gate-recessed structures. From drain current LFN characterization, we find pure $1/f$ spectra for the well-above-threshold regime, and superposition of $1/f$ and Lorentzian spectra near the threshold voltage. The Hooge parameters are evaluated from the $1/f$ contribution and found to be independent of the AlTiO thickness, but strongly dependent of the remaining AlGaN thickness near the threshold voltage. The Hooge parameters are proportional to the inverse of the channel electron concentration at low concentrations, dominated by the channel electron number fluctuation, which can be attributed to electron traps introduced by the recess etching process in the remaining AlGaN. On the other hand, the

Lorentzian spectra are almost independent of the AlTiO thickness and the remaining AlGaN thickness. Comparing with the gate leakage currents dominated by the Poole-Frenkel mechanism due to traps in AlTiO, we consider that the Lorentzian spectra are attributed to traps in AlTiO near the AlTiO/AlGaN interface.

ACKNOWLEDGMENT

This work was supported by JSPS KAKENHI Grant Number JP22H01545.

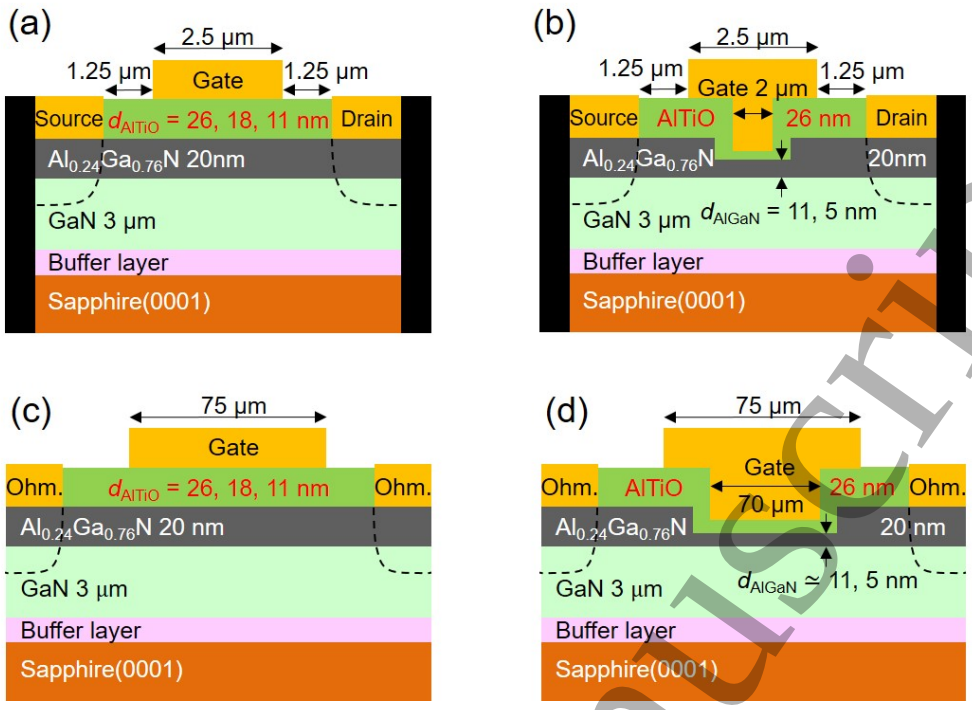

FIG. 1: The dimension of (a) non-recessed and (b) partially-recessed AlTiO/AlGaN/GaN MIS-FETs, and (c) non-recessed and (d) partially-recessed AlTiO/AlGaN/GaN MIS capacitors. The non-recessed devices have the remaining AlGaN thickness of $d_{\mathrm{AlGaN}} = 20$ nm, and AlTiO thicknesses of $d_{\mathrm{AlTiO}} = 26, 18$, and 11 nm. The partially-recessed devices have remaining AlGaN thicknesses of $d_{\mathrm{AlGaN}} \simeq 11$ and 5 nm, and an AlTiO thickness of $d_{\mathrm{AlTiO}} = 26$ nm.

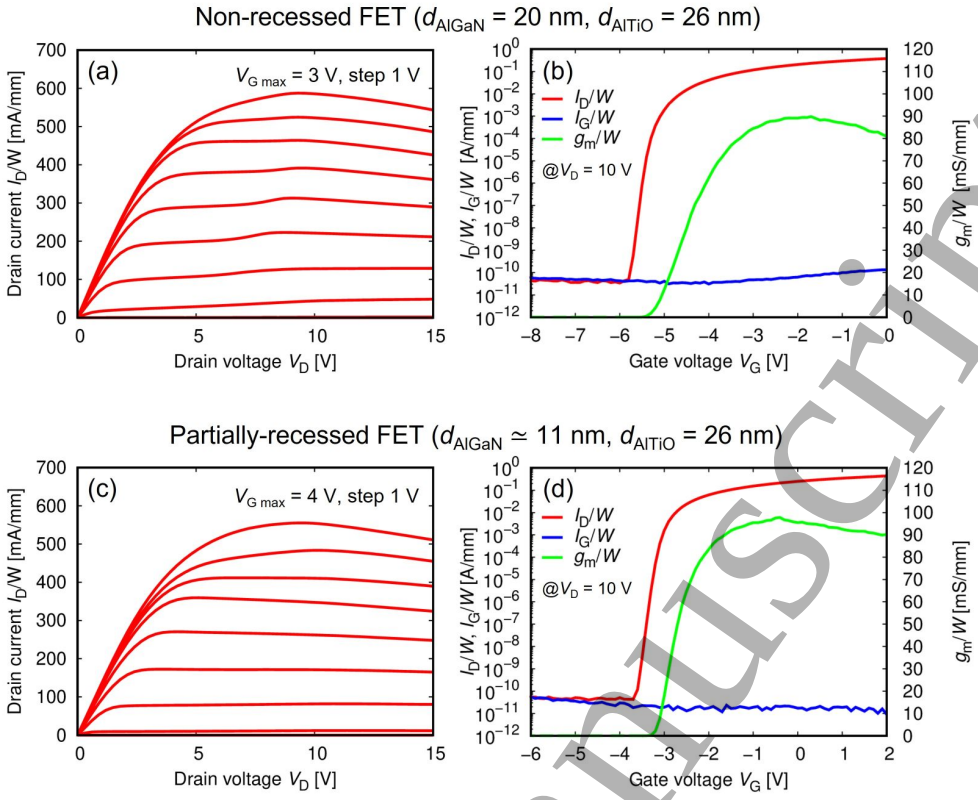

FIG. 2: Device characteristics of FETs with the gate length $L_G = 2.5$ μm and the gate width $W = 50$ μm. (a) Output and (b) transfer characteristics for a non-recessed FET ($d_{AlGaN} = 20$ nm, $d_{AlTiO} = 26$ nm). (c) Output and (d) transfer characteristics for a partially-recessed FET ($d_{AlGaN} \simeq 11$ nm, $d_{AlTiO} = 26$ nm). I_D is the drain current, I_G is the gate current, and g_m is the transconductance, which are normalized by W and shown on the vertical axes.

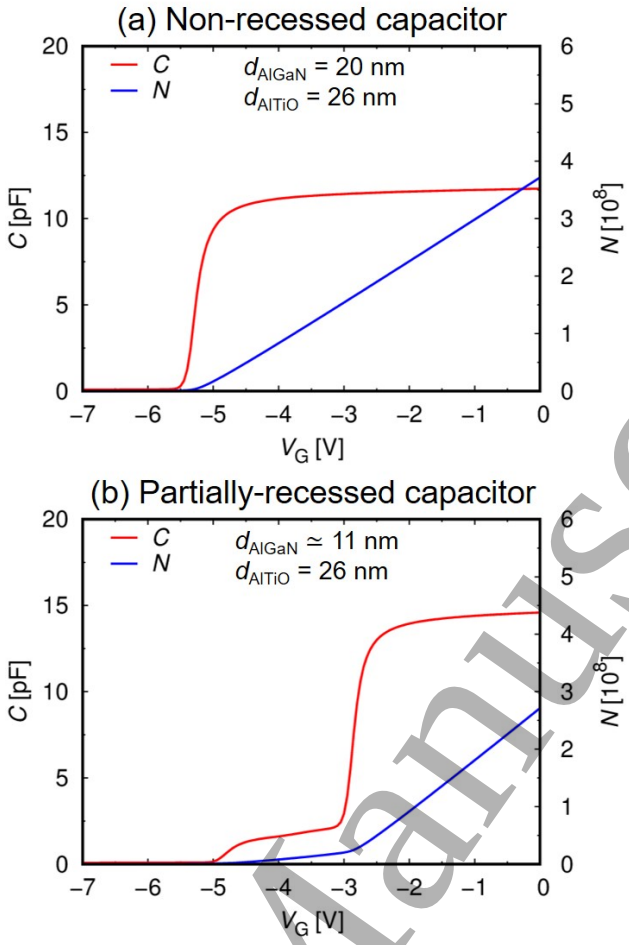

FIG. 3: The C-V characteristics of (a) a non-recessed capacitor ($d_{\mathrm{AlGaN}} = 20$ nm, $d_{\mathrm{AlTiO}} = 26$ nm) and (b) a partially-recessed capacitor ($d_{\mathrm{AlGaN}} \simeq 11$ nm, $d_{\mathrm{AlTiO}} = 26$ nm). The carrier number N is calculated by integrating C as a function of V_{G}.

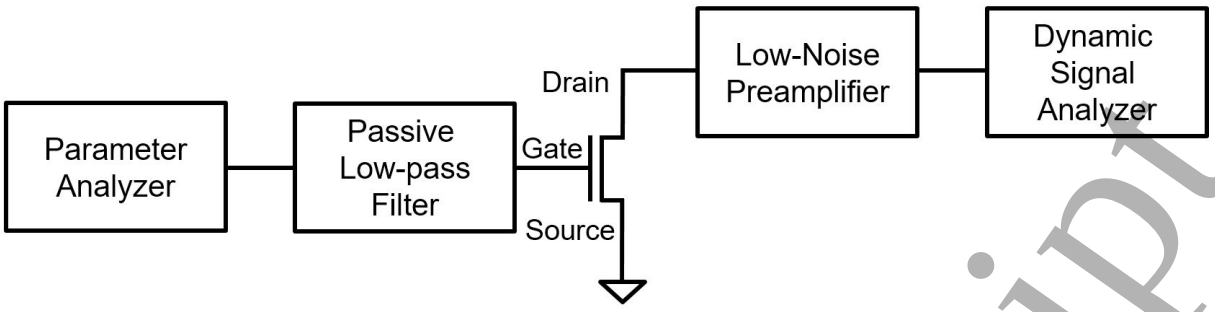

FIG. 4: The schematic of the LFN measurement setup. A low-noise preamplifier (Stanford SR570), a dynamic signal analyzer (Agilent 35670A), and an RC passive low-pass filter (cut-off frequency ~ 0.05 Hz) are used. The FET gate is connected to a parameter analyzer through the low-pass filter to eliminate the noise from the parameter analyzer.

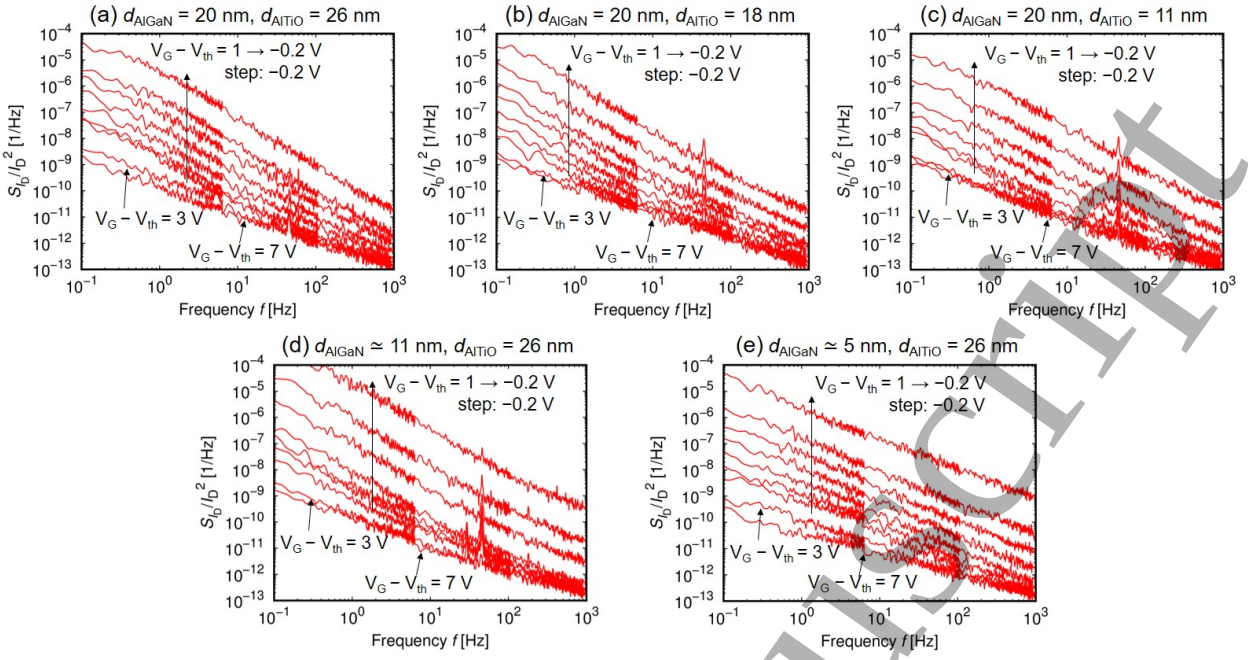

FIG. 5: Examples of LFN spectra normalized by the drain current square, S_{I_D}/I_D^2, for the non-recessed FETs (a), (b), and (c), and the partially-recessed FETs (d) and (e).

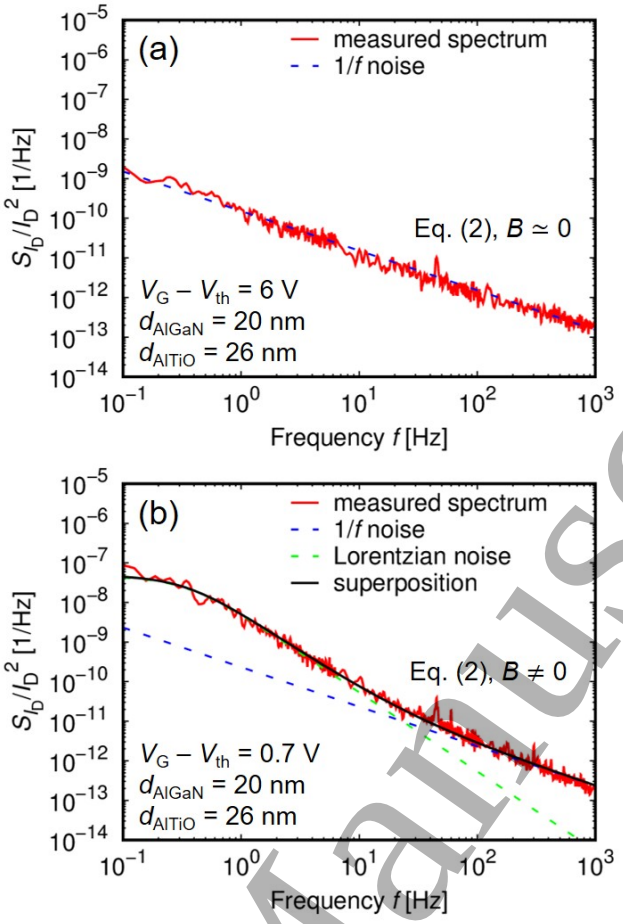

FIG. 6: Examples of fitting of current PSD (a) in the well-above threshold voltage regime using Eq. (2) with $B \simeq 0$, and (b) near the threshold voltage using Eq. (2) with $B \neq 0$.

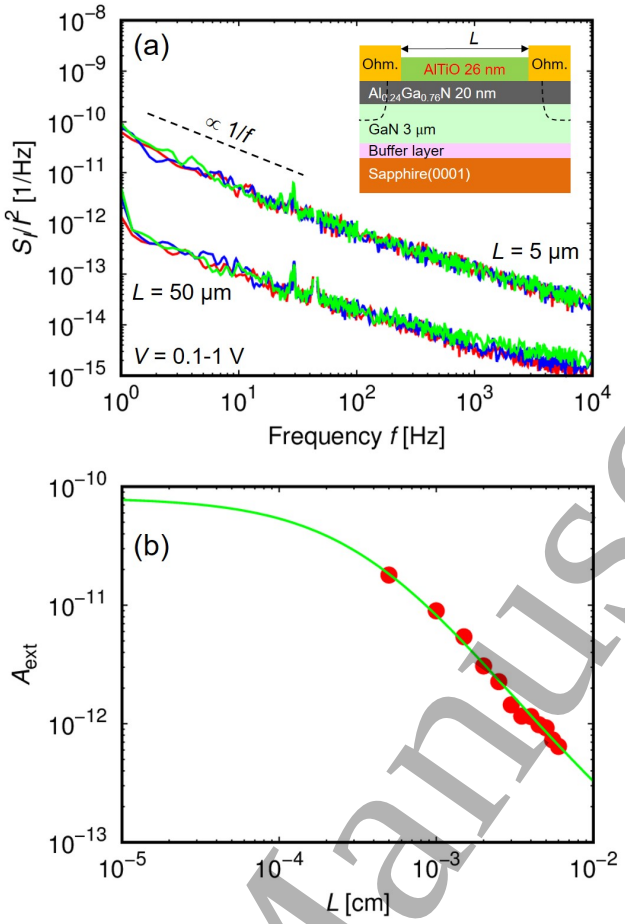

FIG. 7: (a) LFN spectra of the AlTiO/AlGaN/GaN ungated 2T devices (the inset). (b) A_{ext} depending on the access length.

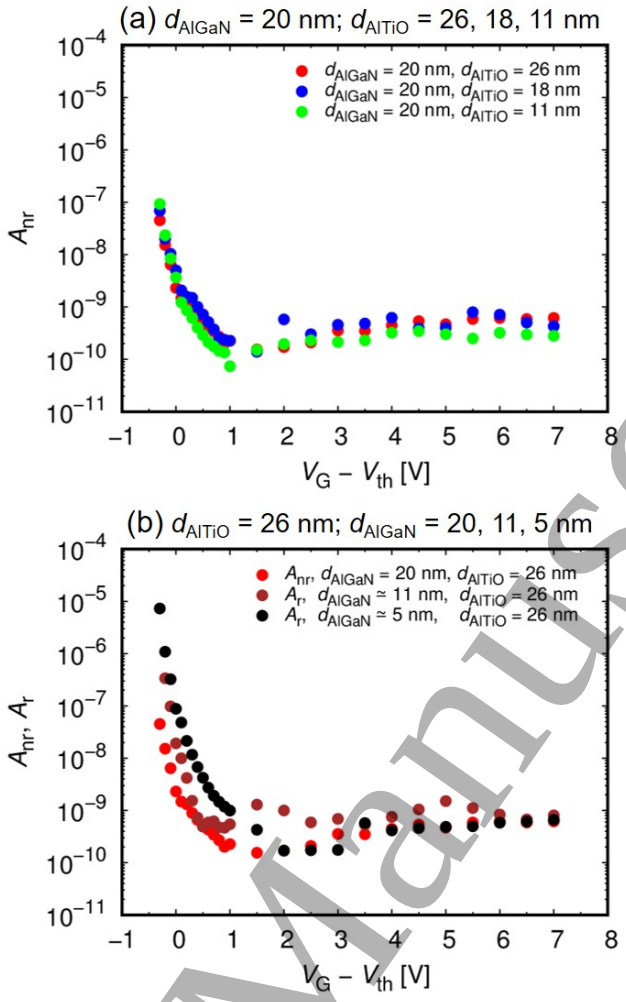

FIG. 8: $A_{\rm nr}$ of the non-recessed FETs and $A_{\rm r}$ of the partially-recessed FETs as functions of $V_{\rm G}-V_{\rm th}$. (a) $d_{\rm AlGaN} = 20$ nm; $d_{\rm AlTiO} = 26$, 18, 11 nm. (b) $d_{\rm AlTiO} = 26$ nm; $d_{\rm AlGaN} = 20$, 11, 5 nm.

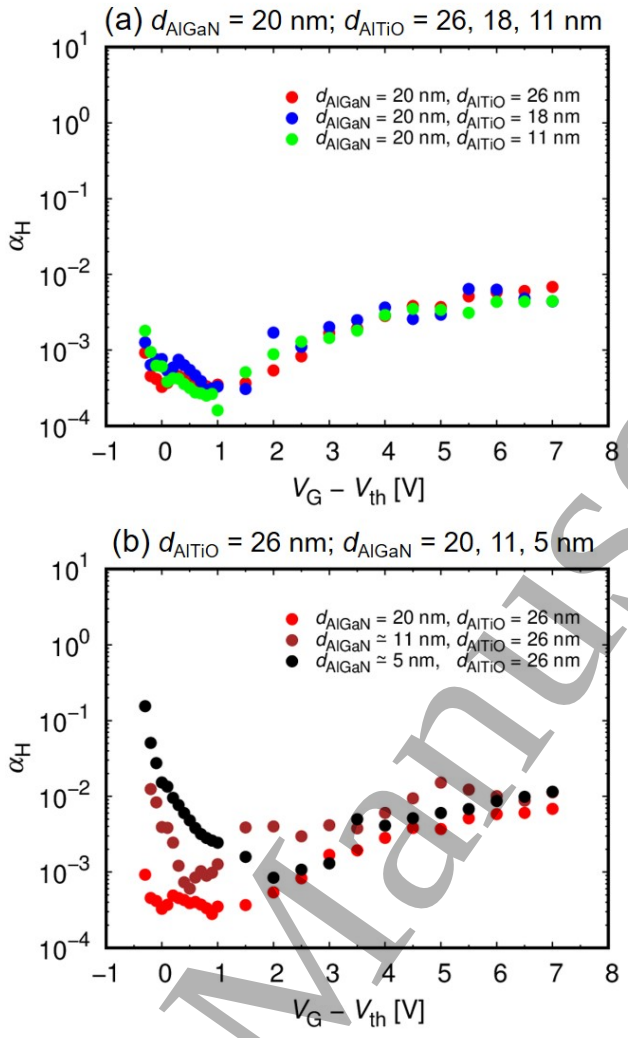

FIG. 9: Hooge parameters α_H of the non-recessed FETs and the partially-recessed FETs as functions of $V_G - V_{th}$. (a) $d_{AlGaN} = 20$ nm; $d_{AlTiO} = 26$, 18, 11 nm. (b) $d_{AlTiO} = 26$ nm; $d_{AlGaN} = 20$, 11, 5 nm.

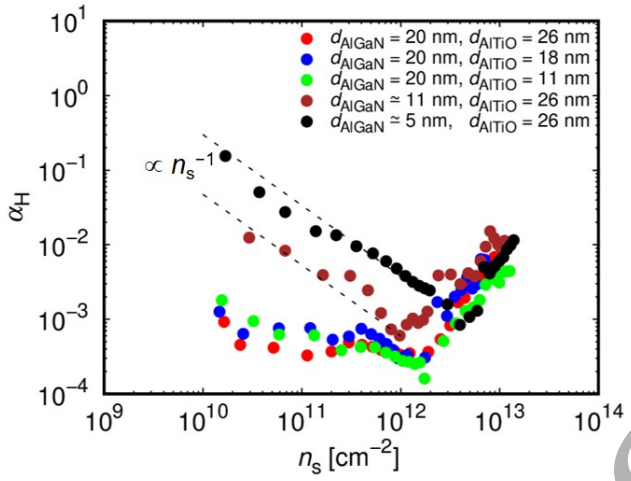

FIG. 10: The Hooge parameter α_{H} of each FET as a function of the sheet electron concentration n_{s}.

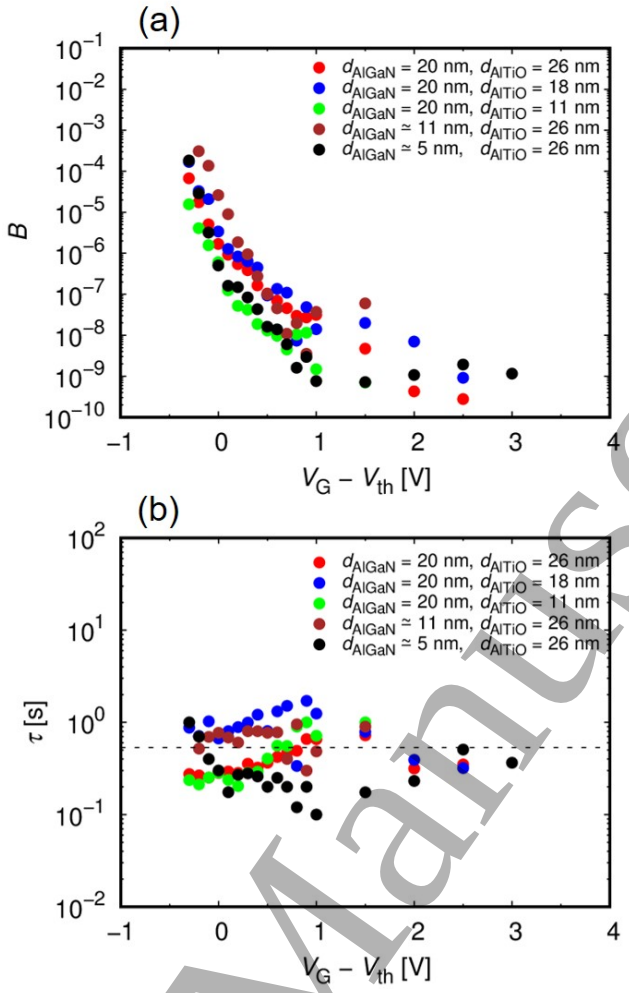

FIG. 11: (a) The prefactor B and (b) the time constant τ for the Lorentzian spectra as functions of $V_{\mathrm{G}} - V_{\mathrm{th}}$.

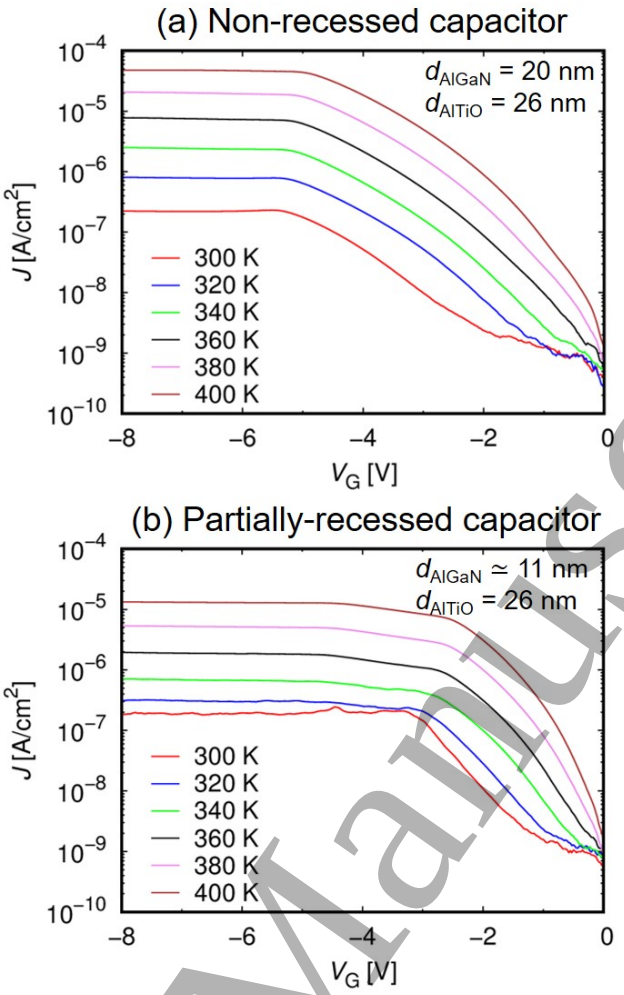

FIG. 12: The gate leakage current density J as a function of V_G at T = 300-400 K for (a) the non-recessed capacitor and (b) the partially-recessed capacitor.

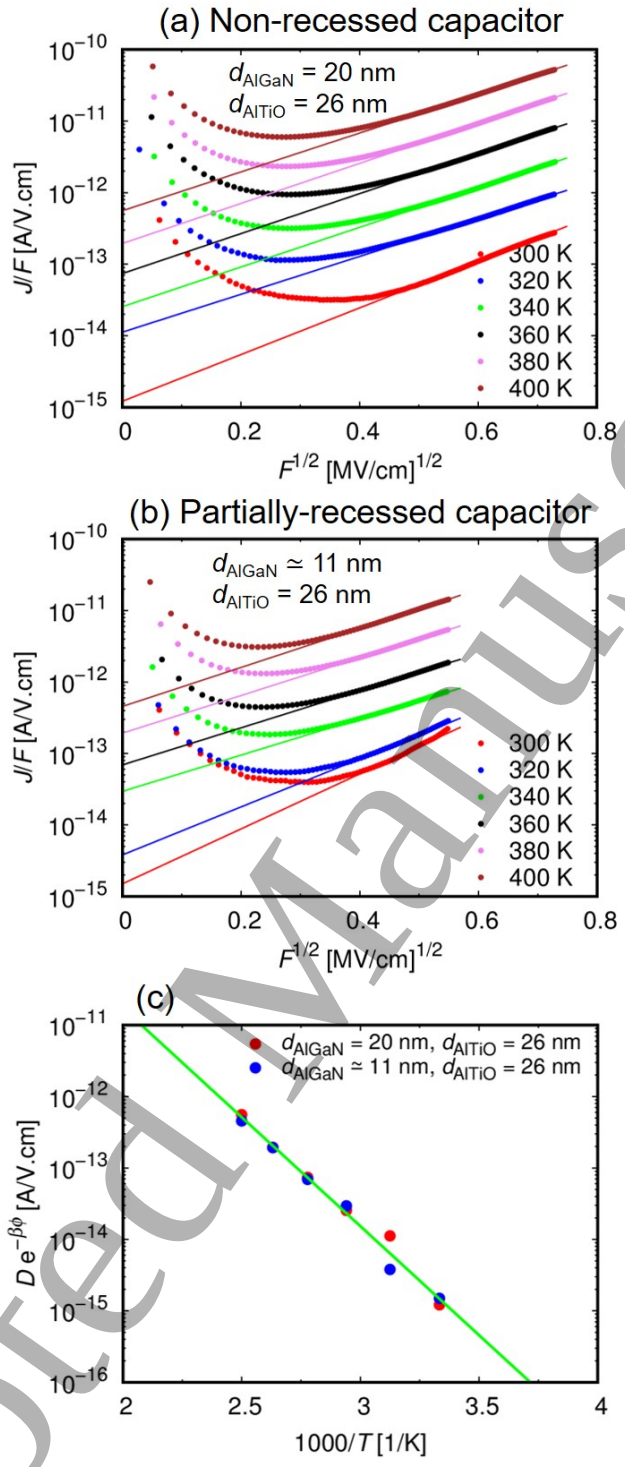

FIG. 13: Poole-Frenkel plots (J/F-$\sqrt{F}$) for (a) the non-recessed capacitor and (b) the partially-recessed capacitor. (c) $D\exp(-\beta\phi)$ as a function of $1/T$ with a fitting line.

REFERENCES

[1] T. Hashizume, S. Ootomo, and H. Hasegawa, Appl. Phys. Lett. **83**, 2952 (2003).

[2] C. Liu, E. F. Chor, and L. S. Tan, Appl. Phys. Lett. **88**, 173504 (2006).

[3] A. Kawano, S. Kishimoto, Y. Ohno, K. Maezawa, T. Mizutani, H. Ueno, T. Ueda, and T. Tanaka, Phys. Status Solidi C **4**, 2700 (2007).

[4] S. Yagi, M. Shimizu, M. Inada, Y. Yamamoto, G. Piao, H. Okumura, Y. Yano, N. Akutsu, and H. Ohashi, Solid-State Electron. **50**, 1057 (2006).

[5] C. Gupta, S. H. Chan, A. Agarwal, N. Hatui, S. Keller, and U. K. Mishra, IEEE Electron Device Lett. **38**, 1575 (2017).

[6] D. Kikuta, K. Ito, T. Narita, and T. Kachi, Appl. Phys. Express **13**, 026504 (2020).

[7] S. P. Le, T. Ui, T. Q. Nguyen, H.-A. Shih, and T. Suzuki, J. Appl. Phys. **119**, 204503 (2016).

[8] A. Colon, L. Stan, R. Divan, and J. Shi, J. Vac. Sci. Technol. A **35**, 01B132 (2017).

[9] S. P. Le, D. D. Nguyen, and T. Suzuki, J. Appl. Phys. **123**, 034504 (2018).

[10] S. Dutta Gupta, A. Soni, V. Joshi, J. Kumar, R. Sengupta, H. Khand, B. Shankar, N. Mohan, S. Raghavan, N. Bhat, and M. Shrivastava, IEEE Trans. Electron Devices **66**, 2544 (2019).

[11] D. D. Nguyen and T. Suzuki, J. Appl. Phys. **127**, 094501 (2020).

[12] D. D. Nguyen, T. Isoda, Y. Deng, and T. Suzuki, J. Appl. Phys. **130**, 014503 (2021).

[13] T. Sato, J. Okayasu, M. Takikawa, and T. Suzuki, IEEE Electron Device Lett. **34**, 375 (2013).

[14] M. Nozaki, K. Watanabe, T. Yamada, H.-A. Shih, S. Nakazawa, Y. Anda, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, Jpn. J. Appl. Phys. **57**, 06KA02 (2018).

[15] J.-C. Gerbedoen, A. Soltani, M. Mattalah, M. Moreau, P. Thevenin, and J.-C. D. Jaeger, Diamond Relat. Mater. **18**, 1039 (2009).

[16] T. Q. Nguyen, H.-A. Shih, M. Kudo, and T. Suzuki, Phys. Status Solidi C **10**, 1401 (2013).

[17] Y. Liu, J. Bardwell, S. McAlister, S. Rolfe, H. Tang, and J. Webb, Phys. Status Solidi C **0**, 69 (2003).

[18] H.-A. Shih, M. Kudo, and T. Suzuki, Appl. Phys. Lett. **101**, 043501 (2012).

[19] H.-A. Shih, M. Kudo, M. Akabori, and T. Suzuki, Jpn. J. Appl. Phys. **51**, 02BF01 (2012).

[20] H.-A. Shih, M. Kudo, and T. Suzuki, J. Appl. Phys. **116**, 184507 (2014).

[21] S. P. Le, T. Q. Nguyen, H.-A. Shih, M. Kudo, and T. Suzuki, J. Appl. Phys. **116**, 054510 (2014).

[22] M. Ťapajna, Crystals **10** (2020).

[23] J. T. Asubar, Z. Yatabe, D. Gregusova, and T. Hashizume, J. Appl. Phys. **129**, 121102 (2021).

[24] H.-C. Chiu, J.-H. Wu, C.-W. Yang, F.-H. Huang, and H.-L. Kao, IEEE Electron Device Lett. **33**, 958 (2012).

[25] H.-S. Choi, IEEE Electron Device Lett. **35**, 624 (2014).

[26] S. Sakong, S.-H. Lee, T. Rim, Y.-W. Jo, J.-H. Lee, and Y.-H. Jeong, IEEE Electron Device Lett. **36**, 229 (2015).

[27] F. Crupi, P. Magnone, S. Strangio, F. Iucolano, and G. Meneghesso, IEEE Trans. Electron Devices **63**, 2219 (2016).

[28] K.-S. Im, IEEE Electron Device Lett. **42**, 18 (2021).

[29] M. E. Levinshtein, F. Pascal, S. Contreras, W. Knap, S. L. Rumyantsev, R. Gaska, J. W. Yang, and M. S. Shur, Appl. Phys. Lett. **72**, 3053 (1998).

[30] J. A. Garrido, B. E. Foutz, J. A. Smart, J. R. Shealy, M. J. Murphy, W. J. Schaff, L. F. Eastman, and E. Muñoz, Appl. Phys. Lett. **76**, 3442 (2000).

[31] S. L. Rumyantsev, N. Pala, M. S. Shur, R. Gaska, M. E. Levinshtein, M. A. Khan, G. Simin, X. Hu, and J. Yang, J. Appl. Phys. **88**, 6726 (2000).

[32] S. L. Rumyantsev, N. Pala, M. S. Shur, M. E. Levinshtein, M. Asif Khan, G. Simin, and J. Yang, J. Appl. Phys. **93**, 10030 (2003).

[33] L.-H. Huang, S.-H. Yeh, and C.-T. Lee, Appl. Phys. Lett. **93**, 043511 (2008).

[34] H.-C. Chiu, C.-H. Chen, H.-L. Kao, F.-T. Chien, P.-K. Weng, Y.-T. Gau, and H.-W. Chuang, Microelectron. Reliab. **53**, 1897 (2013).

[35] A. Balandin, S. Morozov, G. Wijeratne, S. J. Cai, R. Li, J. Li, K. L. Wang, C. R. Viswanathan, and Y. Dubrovskii, Appl. Phys. Lett. **75**, 2064 (1999).

[36] C. Kayis, J. H. Leach, C. Y. Zhu, M. Wu, X. Li, Ü. Özgür, H. Morkoç, X. Yang, V. Misra, and P. H. Handel, IEEE Electron Device Lett. **31**, 1041 (2010).

[37] C. Kayis, J. H. Leach, C. Zhu, M. Wu, X. Li, Ü. Özgür, H. Morkoç, X. Yang, V. Misra, and P. H. Handel, Phys. Status Solidi C **8**, 1539 (2011).

[38] C. Kayis, C. Y. Zhu, M. Wu, X. Li, Ü. Özgür, and H. Morkoç, J. Appl. Phys. **109**, 084522 (2011).

[39] N. K. Subramani, J. Couvidat, A. A. Hajjar, J.-C. Nallatamby, D. Floriot, M. Prigent, and R. Quéré, IEEE Electron Device Lett. **38**, 1109 (2017).

[40] K. Takakura, V. Putcha, E. Simoen, A. R. Alian, U. Peralagu, N. Waldron, B. Parvais, and N. Collaert, IEEE Trans. Electron Devices **67**, 3062 (2020).

[41] M. Glória Caño de Andrade, L. Felipe de Oliveira Bergamim, B. Baptista Júnior, C. Roberto Nogueira, F. Alex da Silva, K. Takakura, B. Parvais, and E. Simoen, Solid State Electron. **183**, 108050 (2021).

[42] S. P. Le, T. Ui, and T. Suzuki, Appl. Phys. Lett. **107**, 192103 (2015).

[43] L. K. J. Vandamme and F. N. Hooge, IEEE Trans. Electron Devices **55**, 3070 (2008).

[44] S. L. Rumyantsev, N. Pala, M. S. Shur, R. Gaska, M. E. Levinshtein, P. A. Ivanov, M. A. Khan, G. Simin, X. Hu, and J. Yang, Semicond. Sci. Technol. **17**, 476 (2002).

[45] J. Lee, J. Brini, A. Chovet, and C. Dimitriadis, Solid-State Electron. **43**, 2185 (1999).

[46] F. Werner, A. Cosceev, and J. Schmidt, J. Appl. Phys. **111**, 073710 (2012).

[47] H. Zhang, X. Zheng, X. Wang, T. Zhu, Y. Wang, X. Ma, and Y. Hao, Micro and Nanostructures **178**, 207579 (2023).

[48] M. L. Huang, Y. C. Chang, C. H. Chang, T. D. Lin, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **89**, 012903 (2006).

[49] M. D. Stamate, Appl. Surf. Sci. **205**, 353 (2003).

[50] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices,* p. 227 (John Wiley & Sons, 2007).