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Studies on Current Modulation of Charge-Density-Wave Field-Effect Transistor

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Mechanisms of the current modulation due to the gate bias in charge-density-wave field-effect transistors (CDW FETs) with CDW materials were investigated. It was clarified that the CDW dislocations do not modulate the CDW current and that the current is modulated under the gate electrode. Further, the current modulation is caused by the modulation of the sliding motion of CDW.

Recently, a novel electronic device, a charge-density-wave field-effect transistors (CDW FETs), has been fabricated.[1] The structure of this device is similar to that of the metal-oxide-semiconductor field-effect transistor (MOS FET), but the channel layer is made of charge-density-wave (CDW) materials. This CDW FETs has a potential to become a useful functional device, because its characteristics are different from one of conventional FETs. The most important feature of this device is current modulation by the gate bias V_{G} in the nonlinear conduction region. The conduction between the source and drain electrodes of this device is similar to that of bulk CDW materials.[2] The conductivity is ohmic when the voltage V_{DS} between the source and the drain is lower than a threshold voltage V_{T}, but the current increases nonlinearly above V_{T}. In this nonlinear region, the positive gate bias V_{G} reduces and the negative gate bias enhances the nonlinear current. This current modulation is considered to be related to the sliding motion of the CDW, because the current modulation in the ohmic region is negligible. The observed modulation was asymmetric or stronger for negative V_{G} than for positive V_{G}.

Several possible mechanisms for the current modulation have been proposed. The gate bias is screened by carriers, and the chemical potential is varied from chain to chain. Consequently, the characteristic parameters of the CDW condensate, such as the gap, the amplitude, and the wavenumber, are modulated near the surface of the CDW material. These modulations should influence the CDW current. On the other hand, the modulation of the wavenumber causes frustration on the three-dimensional order of the CDW as well as CDW dislocations. The dislocations may enhance the CDW current, because they facilitate the phase slip required for current conversion at the current contact. The current modulation by this mechanism should have even symmetry, because the dislocations are induced for both negative and positive V_{G}.

Our purpose is to clarify the mechanism of the current modulation of CDW FETs. For this purpose, we first attempt to clarify whether the phase slip at the current contacts is related to the observed current modulation or not. Further, it is desirable to know the position where the nonlinear current is modulated. For this purpose, we investigate the influences of the gate length and the distance between electrodes. We investigate narrow band noise (NBN) in order to clarify whether the sliding motion of CDW is modulated by the gate bias.

Figure 1 shows the structure of our CDW FETs. During the fabrication process, we placed a cleaved CDW material of about 0.2 μm thickness on a glass substrate. The source and drain electrodes of gold paste were formed at both ends of the CDW material, and on SiO_2 insulator of 100 nm thickness was deposited by rf sputtering. Finally, the gate electrode of indium was formed on the SiO_2 insulator. This is different from the FETs fabricated by Adelman et al. in which the gate electrode completely covers the back surface where the source and drain electrodes are formed. In our structure, the gate bias does not modulate the CDW condensate near the current contacts and we can adjust the gate length and the source-gate and gate-drain distances without changing the source-drain length.

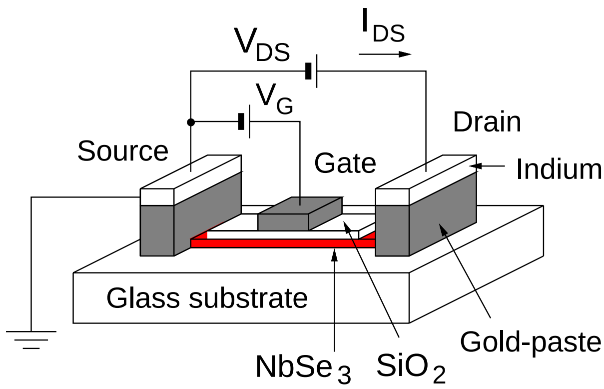

Fig.1: Structure of our CDW FET.

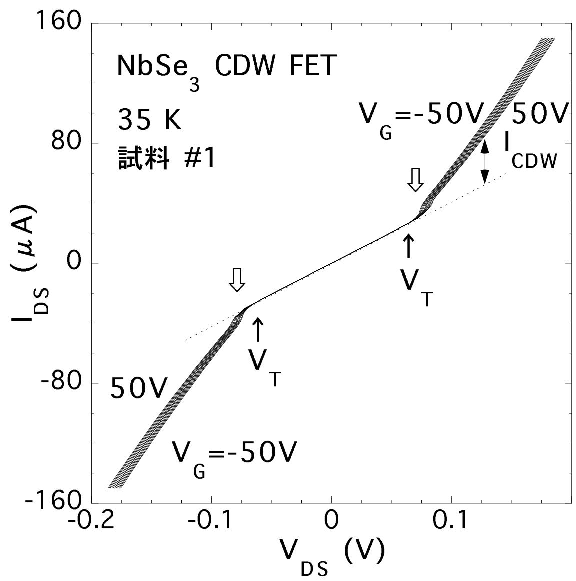

Fig.2: $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristics for several gate voltages.

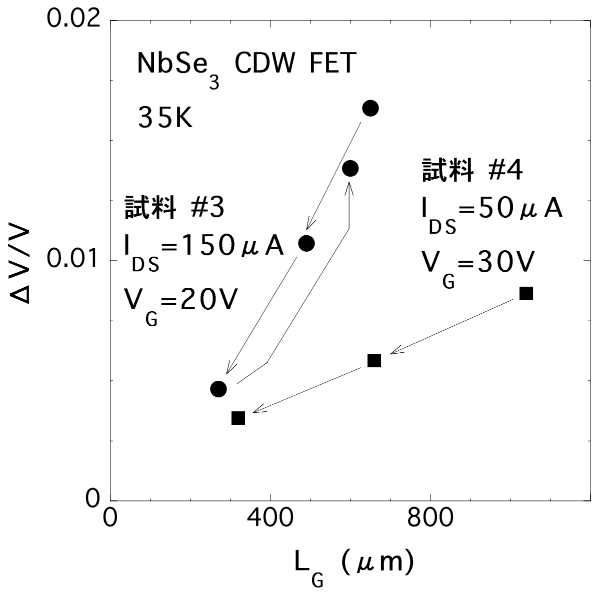

Fig.3: Gate length dependence of the fractional voltage modulation.

Figure 2 shows the $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristics for several gate voltages at 35 K for sample #1, where I_{DS} and V_{DS} are, respectively, the current and voltage between the source and drain electrodes. The conduction is ohmic below the threshold voltage V_{T}, but I_{DS} increases nonlinearly above V_{T} and is strongly modulated by the gate bias V_{G}. The nonlinear current is reduced by the positive gate bias and is enhanced by the negative one. The $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristics has steplike structures near V_{T}, which are not identified in previous work. A similar structure due to extended defects is observed in the bulk CDW materilas. The fractional voltage modulation, $\Delta V/V = [V_{\mathrm{DS}}(V_{\mathrm{G}}, I_{\mathrm{DS}}) - V_{\mathrm{DS}}(0, I_{\mathrm{DS}})]/V_{\mathrm{DS}}(0, I_{\mathrm{DS}})$, has odd symmetry with respect to V_{G}. The current modulation by CDW dislocation should have even symmetry, because the dislocations are induced for both negative and positive V_{G}.

The gate length L_{G} dependence of the fractional voltage modulation $\Delta V/V$ for sample #3 and #4 is shown in Fig. 3. We reduced L_{G} by removing a part of the gate electrode. In order to confirm that this removal of the gate electrode does not induce any damage in the

FETs, we reformed a along gate electrode for sample #3. The fractional voltage modulation is almost proportional to L_{G}. When L_{G} is changed, however, the source-gate and gate-drain lengths are also changed at the same time. Thus, it is necessary to investigate the effect of these lengths. The modulation is almost the same, in spite of large difference of the source-gate length. Therefore, it is confirmed that the current is modulated under the gate electrode.

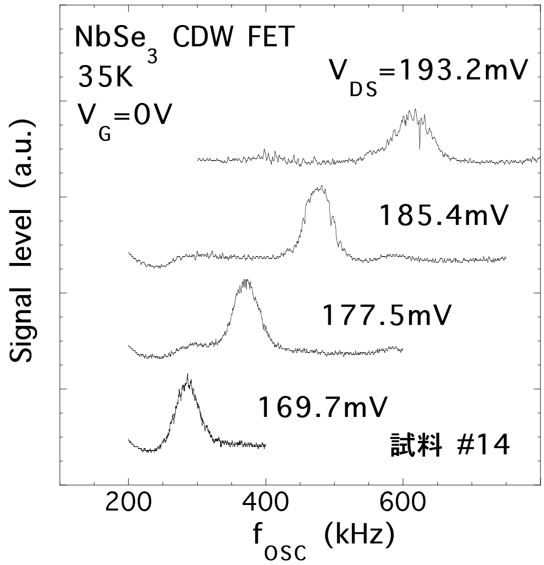

Fig.4: Frequency dependence of noise level.

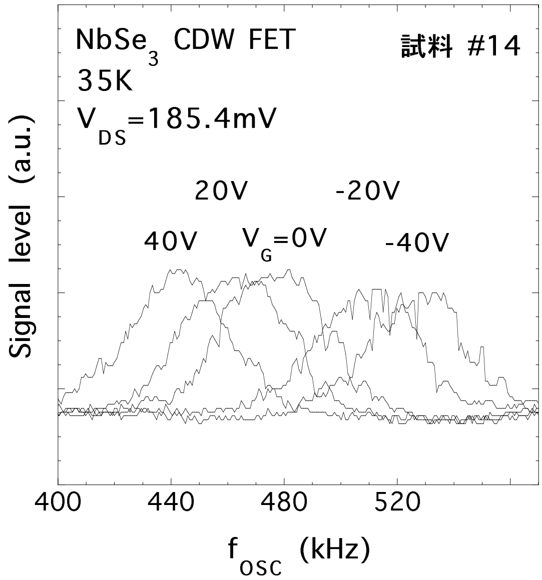

Fig.5: Gate bias dependence of NBN.

NBN is a direct evidence that the nonlinear conduction is due to the sliding motion of CDW. NBN has, however, not been observed in CDW FETs, and it is not confirmed whether the nonlinear conduction is due to the sliding motion of CDW or not. It is necessary for both the appearance of noise only above the threshold voltage and the proportion between the frequency of noise and the nonlinear current to clarify NBN. Figure 4 shows the frequency dependence of noise level when the applied voltage is enhanced. The peak of noise level appears only above the threshold voltage, and the frequency of noise shifts higher frequency when the applied voltage is higher. Threfore, it is clarified that the nonlinear conduction in CDW FETs is due to the sliding motion of CDW.

In this study, we investigated CDW FETs with CDW materials channel. In our CDW FET, the gate electrode is distant from the current contacts and the gate length and distance between electrodes can be changed. In spite of the large difference between the gate electrodes and the current contacts, the nonlinear CDW current is modulated. This means that phase slip at the current contacts is not related to the current modulation. Further, NBN shifts by the gate bias. Therefore, the current modulation is caused by the modulation of the sliding velocity of CDW, and sliding velocity of CDW is modulated completely under the gate.

Reference

[1] T. L. Adelman, S.V. Zaitsev-Zotov, and R.E. Thorne, Phys. Rev. Lett. **74** (1995) 5264.
[2] See for example, G. Grüner, *Density Waves in Solids*, (Addison-Wesley New York, 1994).

Publication list

1. Mikio Koyano and Ryo Kurita, *"Magnetization of Quasi-Two-Dimensional Conductor η-Mo_4O_{11}", Solid State Comm.* **105** (1998) 743.

2. Ryo Kurita, Mikio Koyano, and Shin'ichi Katayama, *"Field Modulation Effects on Charge-Density-Wave Conductor in $NbSe_3$", Physica B*, in press

3. Ryo Kurita, *"Current Modulation of Charge-Density-Wave Field-Effect Transistors with $NbSe_3$ channel", J. Phys. Soc. Jpn.* (submitted to)