Operation characteristics of integrated FET type ferroelectric memory with an intermediate electrode on an Si substrate

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Introduction

Ferroelectric random access memory (FeRAM) has attracted much interest as a next-generation memory because it has the ideal characteristics as high-speed operation, low power drive, high rewriting endurance and so on. Because, in addition to the above-mentioned advantages, the field-effect transitor (FET) type ferroelectric memory with the gate of ferroelectric material (FeFET) is non-destructive reading, it is expected as an ultimate memory. The structure of the conventional FeFET is Metal- Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) or MFIS. In order to prevent the chemical reaction between Si and ferroelectric film, the insulator buffer layer with a high dielectric constant must be inserted between them. Due to this buffer layer, this structure has many problems.

1. Operation voltage becomes large due to voltage drop on the buffer layer.
2. In the memory retention state in which the gate is grounded, depolarization field occurs in a ferroelectric layer by the electric charge held at the buffer layer. So remanent polarization is reduced small and the retention time becomes short.
3. Since the interface characteristic between a buffer layer and Si substrate is poor, the interface electrical property is bad.

On the other hand, the ferroelectric memory with an intermediate electrode proposed by our laboratory has the following advantages.

1. High operation voltage is avoided by applying writing voltage V_W only to ferroelectric capacitor C_f, which means that there is no voltage drop on the gate insulating buffer layer.
2. The short retention time is improved because the depolarization field is not generated due to keeping the polarization state under zero bias condition.
3. Instability of an electrical property is improved by using SiO_2 as a buffer layer instead of high dielectric constant material because a low voltage is enough to saturate the ferroelectric capacitor without voltage drop on the SiO_2 layer in this memory.

Until now, the integrated new ferroelectric memory with an intermediate electrode on the Si substrate was already produced and the memory was able to confirm nondestructive memory operation. The purpose of this study is to change the production process of a memory and to improve the nondestructive memory operation. This thesis is described as

follows; first, the basic operation principle of ferroelectric memory with an intermediate electrode is mentioned Secondly, the fabrication process of this memory is mentioned. Thirdly, the crystallinity and electrical property of a thin film are evaluated. Finally, the resalts of the operation characteristics of fabricated memory are shown, when the pulse response of output voltage V_O to reading pulse voltage V_R is measured.

Basic Operation Principle

The schematic diagram of the integrated memory and an approximated P-E hysterisis loop of the ferroelectric capacitor C_f are shown in Fig.1 and Fig.2, respectively. The ferroelectric capacitor C_{fl} from the positive remanent polarization Pr^+ to the positive saturated region is much smaller than C_{fh} from the negative remanent polarization Pr^- through V_{fcl}, where V_{fcl} is a critical ferroelectric voltage V_f at which the C_f is drastically changed. For data writing, a negative or positive voltage V_W is applied only to C_f using the word line with the ON-state MIS-FET2. For data retention, the ferroelectric thin film is maintained at a positive remanent polarization Pr^+ state or a negative remanent polarization Pr^- state with the OFF-state MIS-FET2. For data reading, a reading voltage V_R is applied to both the C_f and the MIS-FET1 between the word line and the Si substrate. At a given V_R, the intermediate voltage V_I between the source and gate of the MIS-FET1 depends on the value of C_f as well as the input capacitor C_{FET} of the MIS-FET. If C_f is C_{fh} and V_I is higher than threshould voltage V_{TR} of MIS-FET1, the drain current I_D flows. If C_f is C_{fl} and V_I is lower than V_{TR}, the MIS-FET1 is still in OFF state, so the drain current I_D doesn't flow. Memory operation is performed by detecting the difference in I_D, which corresponds to "1" or "0".

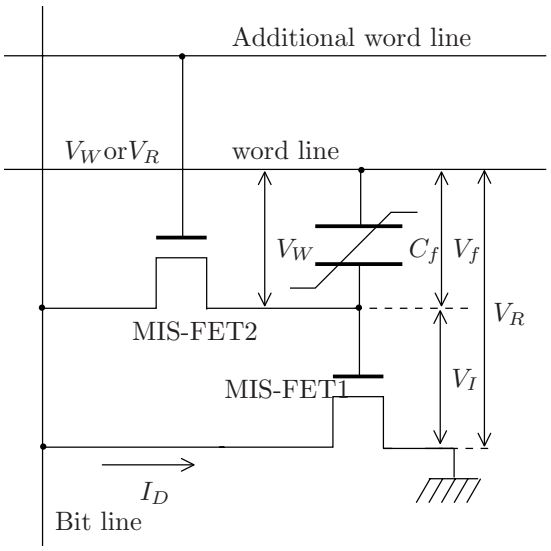

Fig.1 Schematic diagram of the integrated memory structure.

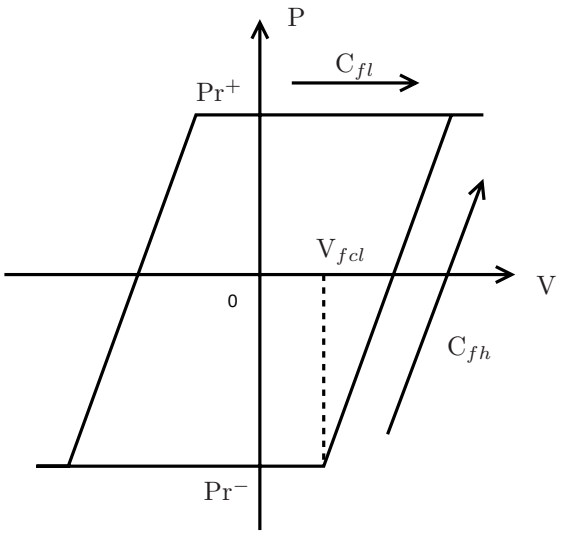

Fig.2 Approximated P-E hysterisis loop of the ferroelectric capacitor.

Fabrication Process and Measurement

Figure 3 shows the schematic top view of the fabricated FET-type ferroelectric memory with an intermediate electrode. Figure 4 shows the schematic cross section view along the A and B line of MFMIS-FET shown in Fig.3. The MFMIS-FET with the RuO_2(200nm)/PZT(200nm)/Ir(50nm)
/YSZ(15nm)/Si structure is a memory cell. The Writing-FET with Ir(50nm)/YSZ(15nm)/Si structure is connected with intermediate electrode of MFMIS-FET. All films except SiO_2 and Al films were deposited onto p-type Si substrate by the sputtering method.

The measuring method of the memory operation is mentioned as follows; For data writing, a positive or negative pulse V_W was applied only to the ferroelectric capacitor between the RuO_2 and Ir electrodes as shown in Fig.5(a). For reading, a positive reading pulse voltage V_R was applied to the gate of MFMIS-FET (between RuO_2 and Si), then the output voltage V_O was measured and the two values of V_O in the Pr^+ and Pr^- states were compared (Fig.5(b)). A resistor R is connected with the drain in order to measure the drain current I_D.

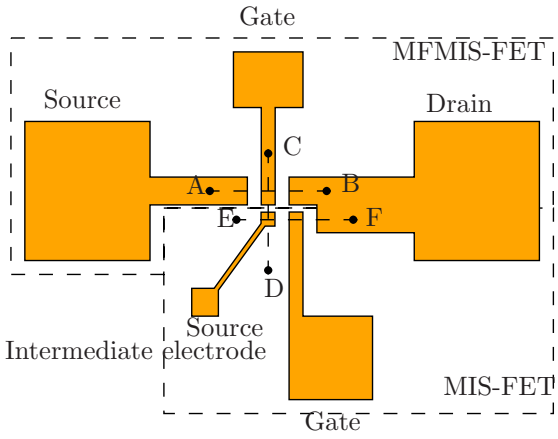

Fig.3 Schematic top view of the memory cell.

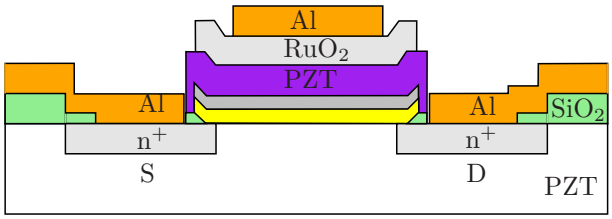

Fig.4 Schematic cross section along the A-B line in Fig.3

Results and Discussion

The pulse response of the output voltage V_O to positive reading voltages V_R for MFMIS-FET is shown in Fig.6, where the measurement condition is as follows; $V_W = \pm 5$ V, $V_R = 5$ V, the $V_D = 2$ V and R =47 kΩ . From this figure, it can be seen that the two signals of V_O for both the Pr^+ and Pr^- states correspond to V_R with 180 °out of phase, which suggests that it operate the transistor normal action. Also, the difference in V_O between the Pr^+ and Pr^- states (ΔV_O) is observed. So, it can be confirmed that this MFMIS-FET operates as a memory. Since the C_f is dependent on the polarization state of the PZT film, the V_I for the Pr^+ and Pr^- states are different from each other, corresponding to C_f.

The ΔV_O of 0.98 V was observed. Moreover, after consecutive 5 pulses train of the reading voltage is applied, it is found that the initial value of ΔV_O was kept for each

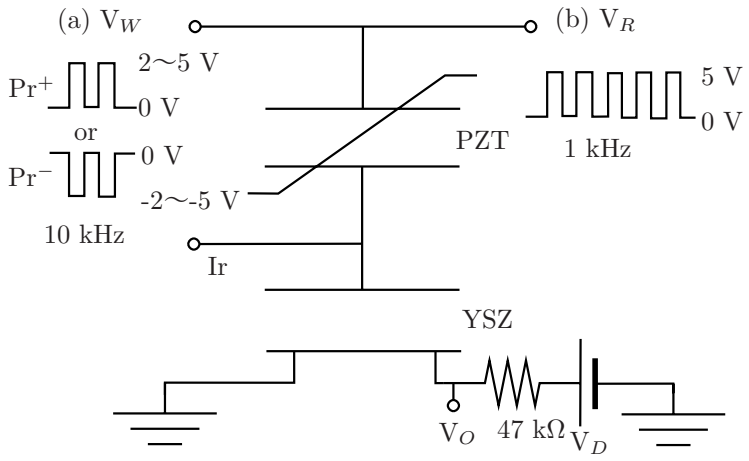

Fig.5 Measurement circuit of pulse response of the output voltage V_O.

reading pulse.This means that this memory operates with nondestructive reading.

In this study, since the etching method of the PZT thin film was changed from Wet-etching to Dry-etching, degradation of the PZT thin film was reduced. Therefore, the ratio difference between C_{fl} and C_{fh} is increased due to of the improved qualty of the ferroelectric film. Also the improvement of the transconductance $g_m$of the MIS-FET from the previaous value of 4.45×10^{-5} to the present value of 1.69×10^{-4} enhaces the ratio of C_{fl}/C_{fh} to make a large signal diffrent in V_O between the Pr^+ and Pr^- states. The reasons of the improvement of g_m are redution of the damge in duaring the etching process of the PZT thin film from Wet to Dry processes.

Conclusion

In this study, the operation principle of a new ferroelectric memory with an intermediate electrode was described. This memory was integrated and fabricated onto the Si substrate. In the pulse response of the output voltage V_O to the reading voltages, difference in V_O between the two remnant polarization states was observed and no destructive operation was confirmed. In this study, ΔV_O has improved greatly from 0.02 to 0.89V. The reason why V_O becames large is mainly improved g_m. This result indicates the possibility to fabricate this new ferroelectric memory with an intermediate electrode in the Si substrate as an integrated circuit.

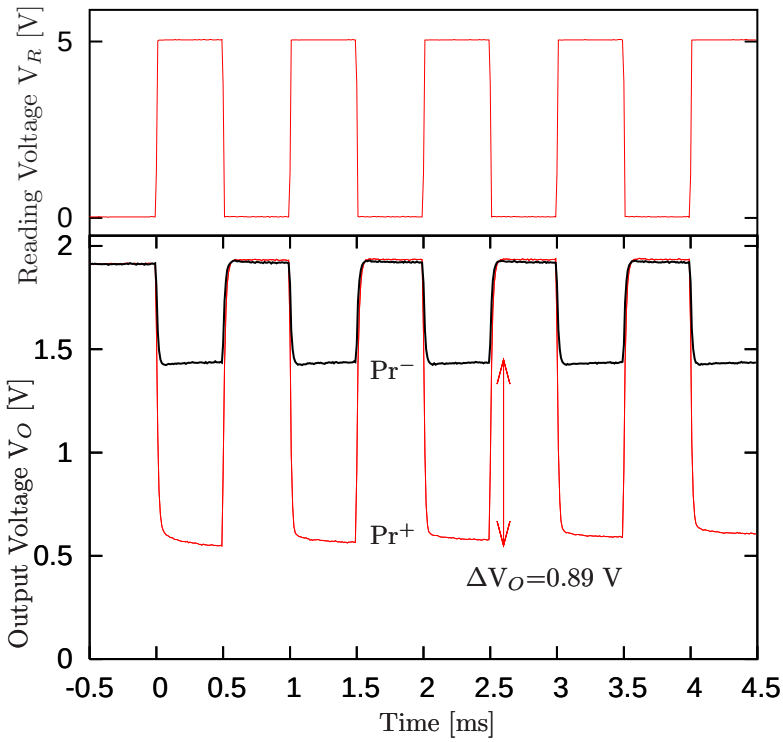

Fig.6 Pulse responses to the output voltage V_O.