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Description				



Japan Advanced Institute of Science and Technology

## Intrinsic transport and contact resistance effect in C<sub>60</sub> field-effect transistors

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The autors report size dependence of characteristics of  $C_{60}$  field-effect transistors (FETs). The transport properties of the channel and the contact resistance between the channel and electrodes are extracted from size dependence. Contact resistances are comparable to those of channel resistances, and the gate voltage dependence of contact resistance is greater than that of channel resistance even at linear region. Results show that the Schottky barriers between the channel and the electrodes still affect device characteristics in the on state of  $C_{60}$  FETs. © 2006 American Institute of Physics. [DOI: 10.1063/1.2372596]

Organic field-effect transistors (OFETs) have great potential in the next-generation electronic devices, due to their inexpensive price, light weight, mechanical flexibility, and high shock resistance.<sup>1</sup> Performance of *p*-type OFETs has been dramatically improved, and mobility has become comparable to that of amorphous Si during recent years.<sup>2,3</sup> Systematic and detailed characterization of *p*-type OFETs has also been performed intensively because their transport properties are very stable in air. $^{4-6}$  On the other hand, the characteristics of *n*-type OFETs are very sensitive to chemically and physically adsorbed  $O_2$  and/or  $H_2O$  molecules<sup>7-9</sup> and depend strongly on sample. This has resulted in difficulties in specifying these precise characteristics. For the application of OFETs to electronic devices, such as complementary metal-oxide semiconductors, detailed characterization and improvement of performance of *n*-type OFETs are required.

A report on a high performance  $C_{60}$  FET with field mobility ( $\mu$ ) of 0.6 cm<sup>2</sup>/V s and current on-off ratio larger than  $10^8$  as *n*-type OFETs(Ref. 10) has stimulated a number of investigations on fullerene FETs.<sup>11,12</sup> In the present study, in order to clarify transport properties of *n*-type OFETs by reducing strong sample dependence, we have fabricated a series of  $C_{60}$  FETs of different sizes in a chip. Properties of the intrinsic channel resistance and of the parasitic resistance between the organic semiconductor and inorganic metal electrodes are extracted from size dependence.

 $C_{60}$  FETs were fabricated with a bottom contact configuration as shown in Fig. 1(b). A heavily doped *n*-type silicon wafer, with a 400 nm thick layer of thermally oxidized SiO<sub>2</sub> on the surface, was used as substrate. The Au source and drain electrodes with thickness of 100 nm were patterned on the insulating SiO<sub>2</sub> layer, using the electron-beam lithography method. In order to extract the channel resistance ( $R_{ch}$ ) and the contact resistance ( $R_c$ ) from the total device resistance ( $R_t$ ), a series of FETs with fixed channel resistance in different sizes was fabricated. The ratio of channel length *L* and channel width *W* (L/W) was fixed to be 0.05. Device dimensions are summarized in Table I. The doped silicon layer of the wafer was used as a gate electrode. Commercially available  $C_{60}$  (99.98%) was used for the formation of the thin film channel layer. A  $C_{60}$  thin film of 150 nm thickness was formed using vacuum ( $<10^{-4}$  Pa) vapor deposition at the deposition rate of 0.1 nm/s. FETs fabricated by this procedure were exposed to air during the transfer from the deposition chamber to the measurement chamber. Before measurements, therefore, the samples were annealed at  $120 \,^{\circ}$ C under  $10^{-3}$  Pa for a few days in order to remove adsorbed  $O_2$  and/or  $H_2O$  molecules. Transport properties of  $C_{60}$  FETs were measured at room temperature under  $10^{-3}$  Pa without exposure to air after annealing. In this study, in order to reduce sample dependence due to the small number of adsorbed  $O_2$  and/or  $H_2O$  molecules, a series of FETs of dif-



FIG. 1. (Color online) (a) Optical photograph image of  $C_{60}$  thin film FET. (b) Cross sectional schematic of device. (c) Optical photograph image of a series of devices.

89, 173510-1

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TABLE I. Size and device parameters of all devices.

$L(\mu m)/W(\mu m)$	5/100	10/200	15/300	20/400
$\mu \text{ (cm}^2/\text{V s)} \\ \text{V}_T \text{ (V)} \\ \text{On-off ratio}$	$2.8 \times 10^{-1}$	$2.8 \times 10^{-1}$	$2.6 \times 10^{-1}$	$2.3 \times 10^{-1}$
	18	18	15	11
	7.3 × 10 <sup>6</sup>	$2.3 \times 10^{7}$	$2.4 \times 10^{7}$	$9.2 \times 10^{6}$

ferent sizes was fabricated in a single substrate [Fig. 1(c)], and the fabrication, annealing, and measurement were all performed under the same conditions.

Output characteristics,  $I_D$  vs  $V_{DS}$  plots, for C<sub>60</sub> FET with  $L=5 \ \mu m$  and  $W=100 \ \mu m$  are shown in Fig. 2(a).  $I_D$  increases almost linearly with  $V_{DS}$ , followed by saturation due to the pinch off of the accumulation layer; all FETs in this work show typical *n*-type normally off characteristics. Hysteresis of  $I_{\rm D}$ 's with  $V_{\rm DS}$  sweep was very small. Figure 2(b) shows  $I_{\rm D}^{1/2}$  vs  $V_{\rm G}$  plot at  $V_{\rm DS}$ =50 V for the same sample. The  $\mu$  and threshold voltage  $V_T$  were determined from the relation  $I_{\rm D} = (\mu W C_0 / 2L) (V_{\rm G} - V_T)^2$  at saturation regime and were found to be  $2.8 \times 10^{-1}$  cm<sup>2</sup>/V s and 18 V, respectively. Here, we use  $1.0 \times 10^{-8}$  F/cm<sup>2</sup> as the capacitance per area of gate insulator SiO<sub>2</sub> ( $C_0$ ) estimated from the dielectric constant and the thickness of SiO<sub>2</sub>, because this estimation is consistent with experimental results.<sup>13</sup> The current on-off ratio,  $I_{\rm D}(V_{\rm G}=50 \text{ V})/I_{\rm D}(V_{\rm G}=0 \text{ V})$ , is  $7.3 \times 10^6$ . Derived device parameters for all devices are summarized in Table I. All devices show qualitatively the same characteristics, and their device parameters are close to those of best ones.<sup>1</sup>

In this work, we estimated  $R_t$  from the steepest part of the slope near  $V_{DS}=15$  V in  $I_D$  vs  $V_{DS}$  plots [see Fig. 2(a)]. As in the case of *p*-type OFETs,<sup>5</sup> it is reasonable that  $R_t$  is expressed by the equation  $R_t=R_{ch}+R_c=(L/W)R_{sheet}+R_c$ , where  $R_{sheet}$  is the resistance per square of channel. When  $R_tW$  is plotted against *L*,  $R_{sheet}$  and  $R_cW$  can be extracted from the slope and the intercept of the ordinate, respectively. These plots for C<sub>60</sub> FETs with different device sizes for each  $V_G$  are shown in Fig. 3. At low  $V_G$ 's, it is difficult to estimate the value of  $R_t$  because of the small value of  $I_D$ , which results in data scattering in  $R_tW$  vs *L* plots. On the other hand, the linear relation between  $R_tW$  and *L* is clearly seen at



FIG. 3. Channel size (*L*) dependence of total device resistance ( $R_t$ ) for gate voltages ( $V_G$ ) of 30, 40, and 50 V. The channel resistance can be derived from slope of  $R_t$  vs *L* plots, and the contact resistance corresponds to the data extrapolated to  $L=0 \ \mu m$  for each gate voltage.

higher  $V_{\rm G}$  's. In these  $V_{\rm G}$ 's,  $R_{\rm sheet}$  and  $R_c W$ , namely,  $R_{\rm ch}$  and  $R_c$ , can be extracted from this relation. We estimated these values for  $V_{\rm G} > 30$  V, where  $I_{\rm D}$ 's are on the order of  $10^{-6}$  A and larger than those in the off state by more than five orders of magnitude. For this reason, we will discuss the transport properties of the device in the on state by using the extracted  $R_{\rm ch}$  and  $R_c$  hereafter.

 $V_{\rm G}$  dependence of extracted  $R_{\rm ch}$  and  $R_c$  for device with  $L=5 \ \mu m$  is shown in Fig. 4(a), and ratios of contact resistance to channel resistance  $(R_c/R_{ch})$  for each device size are summarized in Fig. 4(b).  $R_c/R_{ch}$ 's are order of 1 and decrease with increasing  $V_{\rm G}$  even in the on state. It was thought that the operation mechanism of OFETs is carrier accumulation, whereas that of carbon nanotube FET is Schottky barrier modulation.<sup>14</sup> However, it was found that the device operation is caused by both carrier accumulation and Schottky barrier modulation in *p*-type OFETs.<sup>4,5</sup> Now we have found that device operation in *n*-type OFETs is also caused by both effects. As a result, not only the carrier accumulation but also the reduction of contact resistance plays an important role in device operation independent of types of carrier, electron or hole, in OFETs. From the viewpoint of the application of OFETs to devices, reduction in the effect of contact resistance is an important and general issue for the improvement of device performance.

In conclusion, we reported the transport properties of the channel and the contact resistance between the channel and electrodes extracted from device-size dependence. Contact



FIG. 2. Typical example of (a)  $I_{\rm D}$  vs  $V_{\rm DS}$  plot and (b)  $I_{\rm D}^{1/2}$  vs  $V_{\rm G}$  plot for  $C_{60}$ FET with  $L=5 \ \mu \text{m}$  and  $W=100 \ \mu \text{m}$ . Gate voltages were applied from 0 to 50 V in 5 V steps.



FIG. 4. Gate voltage dependence of (a) contact resistance  $(R_c)$  and channel resistance  $(R_{ch})$  and (b) their ratio  $(R_c/R_{ch})$ .

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resistances are comparable to channel resistances, and the gate voltage dependence of contact resistance is greater than that of channel resistance, even in the on state. We found that the fact that both channel resistance and contact resistance affect device performance is a general characteristic in OFETs. Understanding the electronic structure and transport properties at the interface between an organic semiconductor and inorganic metals is an important factor in the development of organic electronics.

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