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Intrinsic transport and contact resistance effect in C_{60} field-effect transistors

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The autors report size dependence of characteristics of C_{60} field-effect transistors (FETs). The transport properties of the channel and the contact resistance between the channel and electrodes are extracted from size dependence. Contact resistances are comparable to those of channel resistances, and the gate voltage dependence of contact resistance is greater than that of channel resistance even at linear region. Results show that the Schottky barriers between the channel and the electrodes still affect device characteristics in the on state of C_{60} FETs. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2372596]

Organic field-effect transistors (OFETs) have great potential in the next-generation electronic devices, due to their inexpensive price, light weight, mechanical flexibility, and high shock resistance.[1] Performance of *p*-type OFETs has been dramatically improved, and mobility has become comparable to that of amorphous Si during recent years.[2,3] Systematic and detailed characterization of *p*-type OFETs has also been performed intensively because their transport properties are very stable in air.[4–6] On the other hand, the characteristics of *n*-type OFETs are very sensitive to chemically and physically adsorbed O_2 and/or H_2O molecules[7–9] and depend strongly on sample. This has resulted in difficulties in specifying these precise characteristics. For the application of OFETs to electronic devices, such as complementary metal-oxide semiconductors, detailed characterization and improvement of performance of *n*-type OFETs are required.

A report on a high performance C_{60} FET with field mobility (μ) of 0.6 $cm^2/V\,s$ and current on-off ratio larger than 10^8 as *n*-type OFETs(Ref. 10) has stimulated a number of investigations on fullerene FETs.[11,12] In the present study, in order to clarify transport properties of *n*-type OFETs by reducing strong sample dependence, we have fabricated a series of C_{60} FETs of different sizes in a chip. Properties of the intrinsic channel resistance and of the parasitic resistance between the organic semiconductor and inorganic metal electrodes are extracted from size dependence.

C_{60} FETs were fabricated with a bottom contact configuration as shown in Fig. 1(b). A heavily doped *n*-type silicon wafer, with a 400 nm thick layer of thermally oxidized SiO_2 on the surface, was used as substrate. The Au source and drain electrodes with thickness of 100 nm were patterned on the insulating SiO_2 layer, using the electron-beam lithography method. In order to extract the channel resistance (R_{ch}) and the contact resistance (R_c) from the total device resistance (R_t), a series of FETs with fixed channel resistance in different sizes was fabricated. The ratio of channel length L and channel width W (L/W) was fixed to be 0.05. Device dimensions are summarized in Table I. The doped silicon layer of the wafer was used as a gate electrode. Commercially available C_{60} (99.98%) was used for the formation of the thin film channel layer. A C_{60} thin film of 150 nm thickness was formed using vacuum ($<10^{-4}$ Pa) vapor deposition at the deposition rate of 0.1 nm/s. FETs fabricated by this procedure were exposed to air during the transfer from the deposition chamber to the measurement chamber. Before measurements, therefore, the samples were annealed at 120 °C under 10^{-3} Pa for a few days in order to remove adsorbed O_2 and/or H_2O molecules. Transport properties of C_{60} FETs were measured at room temperature under 10^{-3} Pa without exposure to air after annealing. In this study, in order to reduce sample dependence due to the small number of adsorbed O_2 and/or H_2O molecules, a series of FETs of dif-

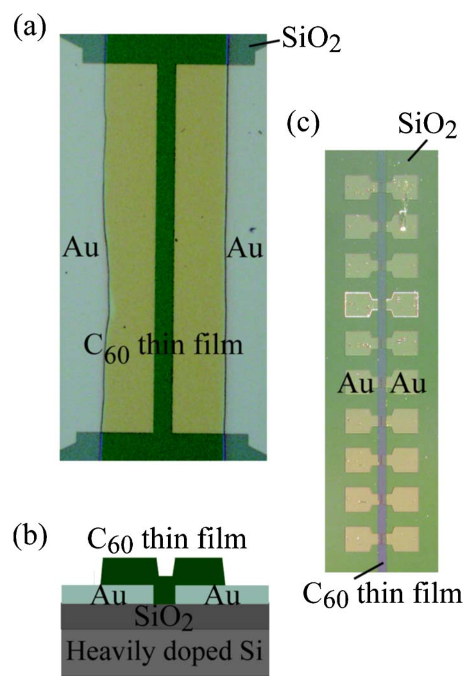

FIG. 1. (Color online) (a) Optical photograph image of C_{60} thin film FET. (b) Cross sectional schematic of device. (c) Optical photograph image of a series of devices.

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TABLE I. Size and device parameters of all devices.

$L(\mu m)/W(\mu m)$	5/100	10/200	15/300	20/400
μ (cm^2/V s)	2.8×10^{-1}	2.8×10^{-1}	2.6×10^{-1}	2.3×10^{-1}
V_T (V)	18	18	15	11
On-off ratio	7.3×10^{6}	2.3×10^{7}	2.4×10^{7}	9.2×10^{6}

ferent sizes was fabricated in a single substrate [Fig. 1(c)], and the fabrication, annealing, and measurement were all performed under the same conditions.

Output characteristics, I_D vs V_{DS} plots, for C_{60} FET with $L=5$ μm and $W=100$ μm are shown in Fig. 2(a). I_D increases almost linearly with V_{DS}, followed by saturation due to the pinch off of the accumulation layer; all FETs in this work show typical n-type normally off characteristics. Hysteresis of I_D's with V_{DS} sweep was very small. Figure 2(b) shows $I_D^{1/2}$ vs V_G plot at $V_{DS}=50$ V for the same sample. The μ and threshold voltage V_T were determined from the relation $I_D=(\mu W C_0/2L)(V_G-V_T)^2$ at saturation regime and were found to be 2.8×10^{-1}cm^2/V s and 18 V, respectively. Here, we use 1.0×10^{-8} F/cm^2 as the capacitance per area of gate insulator SiO_2 (C_0) estimated from the dielectric constant and the thickness of SiO_2, because this estimation is consistent with experimental results.[13] The current on-off ratio, $I_D(V_G=50\text{ V})/I_D(V_G=0\text{ V})$, is 7.3×10^6. Derived device parameters for all devices are summarized in Table I. All devices show qualitatively the same characteristics, and their device parameters are close to those of best ones.[10]

In this work, we estimated R_t from the steepest part of the slope near $V_{DS}=15$ V in I_D vs V_{DS} plots [see Fig. 2(a)]. As in the case of p-type OFETs,[5] it is reasonable that R_t is expressed by the equation $R_t=R_{ch}+R_c=(L/W)R_{sheet}+R_c$, where R_{sheet} is the resistance per square of channel. When R_tW is plotted against L, R_{sheet} and R_cW can be extracted from the slope and the intercept of the ordinate, respectively. These plots for C_{60} FETs with different device sizes for each V_G are shown in Fig. 3. At low V_G's, it is difficult to estimate the value of R_t because of the small value of I_D, which results in data scattering in R_tW vs L plots. On the other hand, the linear relation between R_tW and L is clearly seen at higher V_G 's. In these V_G's, R_{sheet} and R_cW, namely, R_{ch} and R_c, can be extracted from this relation. We estimated these values for $V_G>30$ V, where I_D's are on the order of 10^{-6} A and larger than those in the off state by more than five orders of magnitude. For this reason, we will discuss the transport properties of the device in the on state by using the extracted R_{ch} and R_c hereafter.

V_G dependence of extracted R_{ch} and R_c for device with $L=5$ μm is shown in Fig. 4(a), and ratios of contact resistance to channel resistance (R_c/R_{ch}) for each device size are summarized in Fig. 4(b). R_c/R_{ch}'s are order of 1 and decrease with increasing V_G even in the on state. It was thought that the operation mechanism of OFETs is carrier accumulation, whereas that of carbon nanotube FET is Schottky barrier modulation.[14] However, it was found that the device operation is caused by both carrier accumulation and Schottky barrier modulation in p-type OFETs.[4,5] Now we have found that device operation in n-type OFETs is also caused by both effects. As a result, not only the carrier accumulation but also the reduction of contact resistance plays an important role in device operation independent of types of carrier, electron or hole, in OFETs. From the viewpoint of the application of OFETs to devices, reduction in the effect of contact resistance is an important and general issue for the improvement of device performance.

In conclusion, we reported the transport properties of the channel and the contact resistance between the channel and electrodes extracted from device-size dependence. Contact

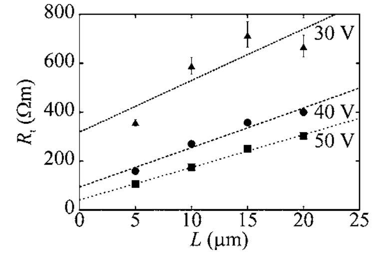

FIG. 3. Channel size (L) dependence of total device resistance (R_t) for gate voltages (V_G) of 30, 40, and 50 V. The channel resistance can be derived from slope of R_t vs L plots, and the contact resistance corresponds to the data extrapolated to $L=0$ μm for each gate voltage.

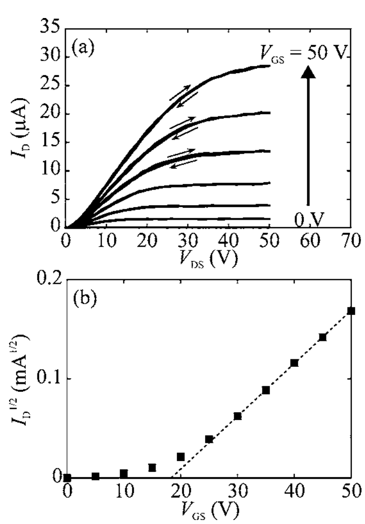

FIG. 2. Typical example of (a) I_D vs V_{DS} plot and (b) $I_D^{1/2}$ vs V_G plot for C_{60} FET with $L=5$ μm and $W=100$ μm. Gate voltages were applied from 0 to 50 V in 5 V steps.

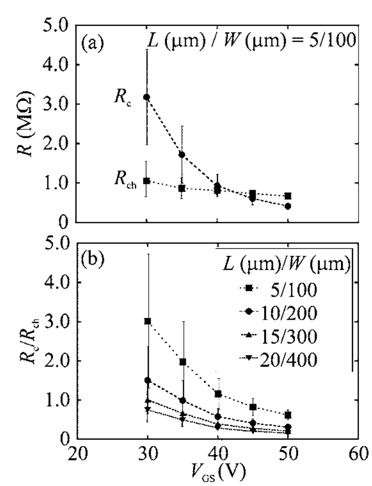

FIG. 4. Gate voltage dependence of (a) contact resistance (R_c) and channel resistance (R_{ch}) and (b) their ratio (R_c/R_{ch}).

resistances are comparable to channel resistances, and the gate voltage dependence of contact resistance is greater than that of channel resistance, even in the on state. We found that the fact that both channel resistance and contact resistance affect device performance is a general characteristic in OFETs. Understanding the electronic structure and transport properties at the interface between an organic semiconductor and inorganic metals is an important factor in the development of organic electronics.

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[1] C. D. Dimitrakopoulos and D. J. Mascaro, IBM J. Res. Dev. **45**, 11 (2004).
[2] V. Podzorov, S. E. Sysoev, E. Loginova, V. M. Pudalov, and M. E. Gershenson, Appl. Phys. Lett. **83**, 3504 (2003).
[3] P. R. L. Malenfant, C. D. Dimitrakopoulous, J. D. Gelorme, L. L. Kosbar, and T. O. Graham, Appl. Phys. Lett. **80**, 2517 (2002).
[4] I. Yagi, K. Tsukagoshi, and Y. Aoyagi, Appl. Phys. Lett. **84**, 813 (2004).
[5] B. H. Hamadani and D. Natelson, J. Appl. Phys. **95**, 1227 (2004).
[6] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie, J. Appl. Phys. **96**, 7312 (2004).
[7] A. Hamed, Y. Y. Sun, Y. K. Tao, R. L. Meng, and P. H. Hor, Phys. Rev. B **47**, 10873 (1993).
[8] B. Pevzner, A. F. Hebard, and M. S. Dresselhaus, Phys. Rev. B **55**, 16439 (1997).
[9] R. Konenkamp, G. Priebe, and B. Pietzak, Phys. Rev. B **60**, 11804 (1999).
[10] S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, and Y. Iwasa, Appl. Phys. Lett. **82**, 4581 (2003).
[11] K. Horiuchi, S. Uchino, S. Hashii, A. Hashimoto, T. Kato, T. Sasaki, N. Aoki, and Y. Ochiai, Appl. Phys. Lett. **85**, 1987 (2004).
[12] Y. Kubozono, T. Nagano, Y. Haruyama, E. Kuwahara, T. Takayanagi, K. Ochi, and A. Fujiwara, Appl. Phys. Lett. **87**, 143506 (2005).
[13] K. Shibata, Y. Kubozono, T. Kanbara, T. Hosokawa, A. Fujiwara, Y. Ito, and H. Shinohara, Appl. Phys. Lett. **84**, 2572 (2004).
[14] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, Phys. Rev. Lett. **89**, 106801 (2002).