

Title	Fabrication of C <sub>60</sub> field-effect transistors with polyimide and Ba <sub>0.4</sub> Sr <sub>0.6</sub> Ti <sub>0.96</sub> O <sub>3</sub> gate insulators
Author(s)	Kubozono, Y; Nagano, T; Haruyama, Y; Kuwahara, E; Takayanagi, T; Ochi, K; Fujiwara, A
Citation	Applied Physics Letters, 87(14): 143506-1-143506-3
Issue Date	2005-10
Type	Journal Article
Text version	publisher
URL	<a href="http://hdl.handle.net/10119/3374">http://hdl.handle.net/10119/3374</a>
Rights	Copyright 2005 American Institute of Physics. This article may be downloaded for personal use only. Any other use requires prior permission of the author and the American Institute of Physics. The following article appeared in Yoshihiro Kubozono, Takayuki Nagano, Yusuke Haruyama, Eiji Kuwahara, Toshio Takayanagi, Kenji Ochi and Akihiko Fujiwara, Applied Physics Letters 87(14), 143506 (2005) and may be found at <a href="http://link.aip.org/link/?apl/87/143506">http://link.aip.org/link/?apl/87/143506</a> .
Description	

## Fabrication of C<sub>60</sub> field-effect transistors with polyimide and Ba<sub>0.4</sub>Sr<sub>0.6</sub>Ti<sub>0.96</sub>O<sub>3</sub> gate insulators

Yoshihiro Kubozono,<sup>a)</sup> Takayuki Nagano, Yusuke Haruyama, Eiji Kuwahara, Toshio Takayanagi, and Kenji Ochi  
 Department of Chemistry, Okayama University, Okayama 700-8530, Japan and CREST, Japan Science and Technology Agency, Kawaguchi, 322-0012, Japan

Akihiko Fujiwara  
 Japan Advanced Institute of Science and Technology, Ishikawa 923-1292, and CREST, Japan Science and Technology Agency, Kawaguchi, 322-0012, Japan

(Received 21 June 2005; accepted 8 August 2005; published online 29 September 2005)

A flexible C<sub>60</sub> field-effect transistor (FET) device has been fabricated with a polyimide gate insulator on the poly(ethylene terephthalate) substrate, and *n*-channel normally off FET properties are observed in this FET device. The field-effect mobility,  $\mu$ , is estimated to be  $\sim 10^{-2}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> at 300 K. Furthermore, the C<sub>60</sub> FET has been fabricated with a high-dielectric Ba<sub>0.4</sub>Sr<sub>0.6</sub>Ti<sub>0.96</sub>O<sub>3</sub> (BST) gate insulator, showing *n*-channel properties; the  $\mu$  value is estimated to be  $\sim 10^{-4}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> at 300 K. The FET device operates at very low gate voltage,  $V_G$ , and low drain-source voltage,  $V_{DS}$ . Thus these C<sub>60</sub> FET devices possess flexibility and low-voltage operation characteristic of polyimide and BST gate insulators, respectively. © 2005 American Institute of Physics. [DOI: 10.1063/1.2081134]

Field-effect transistors (FETs) with thin films of fullerenes have been extensively studied during the past decades,<sup>1-12</sup> and the potential applications of fullerene FETs in next-generation electronic devices have been discussed based on their high values of field-effect mobility,  $\mu$ . The first fullerene FET device was fabricated with thin films of C<sub>60</sub> and a SiO<sub>2</sub> gate insulator by Haddon *et al.*<sup>1</sup> This device showed *n*-channel properties and a high  $\mu$  value of 0.08–0.30 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>. Subsequently, Haddon developed the C<sub>70</sub> FET device with the SiO<sub>2</sub> gate insulator which exhibited the *n*-channel performance with the  $\mu$  value of  $2 \times 10^{-3}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>.<sup>2</sup> The  $\mu$  value of the C<sub>60</sub> FET device reached 0.56 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> (Ref. 3), which was comparable to the highest  $\mu$  value realized so far in the *n*-channel FETs with thin films of organic molecules (OFETs) (Ref. 13).

The characteristics such as shock-resistance, structural flexibility, large-area coverage, and portability are the most important advantages expected for the OFETs. Therefore, it is necessary for the SiO<sub>2</sub>/Si substrate to be replaced by polymer gate insulators in a realization of the complete flexible OFET devices. In 2004, Someya *et al.* successfully fabricated the flexible and high-performance *p*-channel pentacene FET device with polyimide gate insulator.<sup>14</sup> The flexible and high-performance *n*-channel OFET device is required for a realization of the flexible complementary metal-oxide-semiconductor logic gate circuit, which has many advantages such as low-power consumption, good-noise margin, and ease of design.<sup>15</sup>

The C<sub>60</sub> FET device with a high-dielectric gate insulator such as Ba<sub>0.4</sub>Sr<sub>0.6</sub>Ti<sub>0.96</sub>O<sub>3</sub> (BST) attracts special attention for high-carrier injection into the channel region of C<sub>60</sub> thin films, because the doping of electrons and holes into C<sub>60</sub> is expected to yield new materials with novel physical properties, from the analogy with metal-intercalated C<sub>60</sub> exhibiting superconductivity and metallic behavior. Such novel physical

properties are produced by the electron filling to the lowest unoccupied molecular orbital (LUMO) of the C<sub>60</sub> molecule.<sup>16</sup> Currently, the number of electrons that can be injected into the C<sub>60</sub> molecules by field-effect doping is at most 0.1 per C<sub>60</sub> molecule even at the maximum gate voltage  $V_G^{\max}$ , because of the low-dielectric constant  $\epsilon_x$  ( $\sim 3.9$ ) of SiO<sub>2</sub> used as an insulating layer. Therefore, new techniques for high-carrier injection, i.e., injection of more than one electron or hole per C<sub>60</sub> molecule, are required to control the electronic structure of C<sub>60</sub>.

The maximum density of carriers,  $N_{\max}$ (cm<sup>-2</sup>), which can be induced on the dielectric insulating layer, is empirically given by  $N_{\max} \sim 1.1 \times 10^{13} \epsilon_x^{1/2}$  since  $V_G^{\max}$  (MV)  $\sim dE_{\max} \sim 20d/\epsilon_x^{1/2}$ ;  $d$  (cm) is the thickness of the insulating layer. The high-carrier injection into C<sub>60</sub> thin film in the FET device should be realized by using the high  $\epsilon_x$  gate insulator. Furthermore, the high-carrier injection into the active layer should achieve the low gate voltage ( $V_G$ ) and low drain-source voltage ( $V_{DS}$ ) operation in the FET device. The low-voltage operation is very important in a realizing the practical FET device, because the  $V_G$  and  $V_{DS}$  required for operation of the OFET device are currently as high as 10–100 V. In the present study, the C<sub>60</sub> thin-film FET devices with polyimide and BST gate insulators have been fabricated on the poly(ethylene terephthalate) (PET) and the Si substrates, respectively. The fabrication of these FET devices should open a way to the structural flexibility and the low  $V_G$  and  $V_{DS}$  operation in the OFET device.

Schematic representations of cross-sectional views of the C<sub>60</sub> FET devices with polyimide and BST gate insulators are shown in Figs. 1(a) and 1(b), respectively. Commercially available PET substrate was cleaned by washing with acetone, 2-propanol, and ultrapure water, and was dried at 190 °C. The Au gate electrodes with thickness of 50 nm were formed on the PET substrate by a thermal deposition under vacuum of 10<sup>-8</sup> Torr. The films of the polyimide gate insulator were formed by a spin coating of a high-purity

<sup>a)</sup>Electronic mail: kubozono@cc.okayama-u.ac.jp

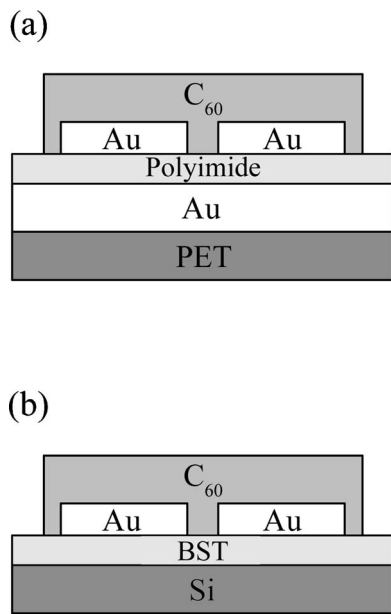


FIG. 1. Schematic representations of cross-sectional view of  $C_{60}$  FET devices with a (a) polyimide gate insulator and (b) BST gate insulator.

polyimide precursor (KEMITITE CT4112, Kyocera Chemical) on the Au/PET substrate at 2000 rpm for 5 s and 4000 rpm for 20 s. The films were heated at 100 °C for 10 min and at 180 °C for 1 h. The surface of polyimide films was treated to be hydrophobic with hexamethyldisilazane (HMDS). Fifty (50) nm thickness of Au source-drain electrodes and 150 nm thickness of  $C_{60}$  thin films were formed on the substrate by the thermal deposition under  $10^{-8}$  Torr. The channel length  $L$  and the channel width  $W$  of the  $C_{60}$  FET device with a polyimide gate insulator were 30 and 2000  $\mu\text{m}$ , respectively.

The BST layer of the chemical composition  $\text{Ba}_{0.4}\text{Sr}_{0.6}\text{Ti}_{0.96}\text{O}_3$  was fabricated on the As-doped Si (100) wafer ( $\rho=0.001\text{--}0.004\ \Omega\ \text{cm}$ ) by the sol-gel method; the isoamyl acetate-amyl alcohol solution of 7 wt %  $\text{Ba}_{0.4}\text{Sr}_{0.6}\text{Ti}_{0.96}\text{O}_3$  was purchased from Mitsubishi Materials Corporation. The Si wafer was cleaned by washing with acetone, methanol, and  $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$  (4:1 in volume), and native  $\text{SiO}_2$  on the Si wafer was removed by immersing it in dilute HF solution. The wafer was finally washed by ultra-pure water. The precursor film of BST was prepared by a spin coating of the  $\text{Ba}_{0.4}\text{Sr}_{0.6}\text{Ti}_{0.96}\text{O}_3$  solution on the Si substrate at 500 rpm for 3 s and at 2000 rpm for 20 s. The substrate was prebaked at 300–400 °C for 10 min. The spin coating and prebaking were repeated four times before the annealing. The substrate was annealed at 700 °C for 1 h under 100 ml  $\text{min}^{-1}$  flow of  $\text{O}_2$ . Fifty (50) nm thickness of source/drain Au electrodes and 150 nm thickness of  $C_{60}$  thin films were formed on the BST/Si substrate by thermal deposition under  $10^{-8}$  Torr; the  $C_{60}$  FET device with the BST layer treated by HMDS has also been fabricated. The  $L$  and  $W$  of the  $C_{60}$  FET device with a BST gate insulator were 30 and 1000  $\mu\text{m}$ , respectively. The FET properties for all FET devices fabricated in the present study were measured after an annealing at 100–140 °C for 24 h under  $10^{-6}$  Torr.

The drain current  $I_D$  versus  $V_{DS}$  plots for the  $C_{60}$  thin-film FET with a polyimide gate insulator at 300 K are shown in Fig. 2(a). The plots show  $n$ -channel normally off FET properties. The plot of  $I_D$  versus  $V_G$  at  $V_{DS}=20\ \text{V}$  is shown in

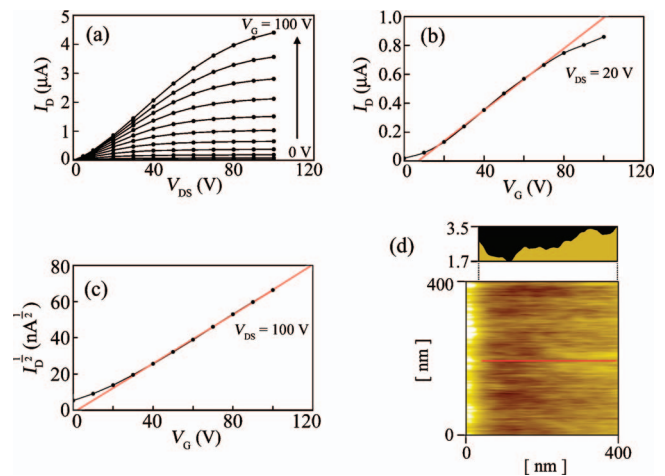


FIG. 2. (Color) (a)  $I_D$ - $V_{DS}$  plots, (b)  $I_D$ - $V_G$  plot at  $V_{DS}=20\ \text{V}$ , and (c)  $(I_D)^{1/2}$ - $V_G$  plot at  $V_{DS}=100\ \text{V}$  for the  $C_{60}$  FET with polyimide gate insulator. (d) AFM image of the polyimide surface (bottom); the cross-sectional AFM image (top) observed along the red line. The brightness in the AFM image (bottom) refers to the unevenness of the surface. As the color brightens, the part is closer to the surface.

Fig. 2(b). The  $I_D$  increases with increasing  $V_G$  to positive up to 100 V. The  $\mu$  and the threshold voltage,  $V_T$ , were determined to be  $7.1 \times 10^{-3}\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  and 7 V, respectively, from the  $I_D$ - $V_G$  plot with the relation,  $I_D = (\mu WC_0/L)(V_G - V_T)V_{DS}$ , where  $C_0$  is the capacitance per area.<sup>17</sup> The  $C_0$  value was determined to be  $1.1 \times 10^{-9}\ \text{F}\ \text{cm}^{-2}$  from the experimental capacitance,  $C = C_0 S$  measured with an LCR meter, where  $S$  is the area of electrode. Further, the  $\mu$  and  $V_T$  values of the  $C_{60}$  FET with the polyimide gate insulator were estimated to be  $1.2 \times 10^{-2}\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  and 2 V, respectively, from the  $(I_D^{\text{sat}})^{1/2}$ - $V_G$  plot [Fig. 2(c)] with the relation  $(I_D^{\text{sat}})^{1/2} = (\mu WC_0/2L)^{1/2}(V_G - V_T)$  (Ref. 17); the saturation of  $I_D$  is clearly observed in Fig. 2(a). The  $(I_D^{\text{sat}})^{1/2}$ - $V_G$  plot was obtained at  $V_{DS}$  of 100 V, and the current on-off ratio,  $I_D(V_G=100\ \text{V})/I_D(V_G=0\ \text{V})$ , was 160.

The atomic force microscope (AFM) image of the polyimide surface is shown in Fig. 2(d). The maximum depth,  $D_{\text{max}}$ , from the surface of the polyimide layer was 5.5 nm. The thickness,  $d$ , of polyimide was estimated to be 3.0  $\mu\text{m}$  from the  $C_0$  value of  $1.1 \times 10^{-9}\ \text{F}\ \text{cm}^{-2}$  with the relation  $C_0 = \epsilon_0 \epsilon_x / d$  by assuming  $\epsilon_x$  of 3.8 (Ref. 14), where  $\epsilon_0$  is permittivity in vacuum. The  $d$  value of the polyimide layer in this device is larger by 7 times than that, 420 nm, of the  $\text{SiO}_2$  layer used by our group in the fullerene FET devices.<sup>9–12</sup> The value of  $C_0$  in the  $C_{60}$  FET with 420 nm of  $\text{SiO}_2$  layer can be estimated to be  $\sim 8.2 \times 10^{-9}\ \text{F}\ \text{cm}^{-2}$  with  $C_0 = \epsilon_0 \epsilon_x / d$  as  $\epsilon_x$  of the  $\text{SiO}_2$  layer is 3.9. Therefore, the  $C_0$  value of the polyimide,  $1.1 \times 10^{-9}\ \text{F}\ \text{cm}^{-2}$ , is smaller than that of  $\text{SiO}_2$ ,  $8.2 \times 10^{-9}\ \text{F}\ \text{cm}^{-2}$ . This implies that the carrier density  $N (= C_0 V_G / e)$ , which can be induced at the same  $V_G$ , is smaller in the  $C_{60}$  FET with a polyimide gate insulator than that with a  $\text{SiO}_2$  layer. This problem can be solved by fabricating the  $C_{60}$  FET device with a thinner polyimide layer with high quality.

The plots of  $I_D$  versus  $V_{DS}$  for the  $C_{60}$  FET device fabricated with the crystalline BST layer are shown in Fig. 3(a). The plots show substantially  $n$ -channel normally off enhancement-type properties. The  $I_D$  increased with increasing the  $V_G$ , while at  $V_G=0\ \text{V}$  the  $I_D$  was extremely small. When decreasing  $V_G$  to the negative value, the small  $I_D$  was

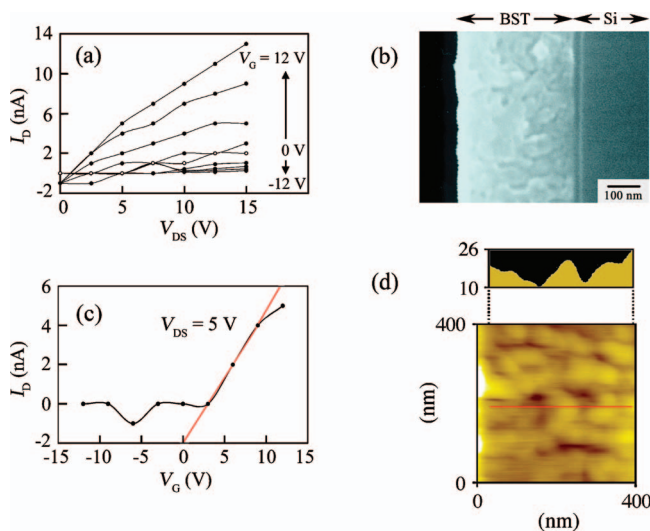


FIG. 3. (Color) (a)  $I_D$ - $V_{DS}$  plots, (b) cross-sectional SEM image, (c)  $I_D$ - $V_G$  plot at  $V_{DS}=5$  V for the  $C_{60}$  FET device with BST gate insulator. (d) AFM image of the BST surface (bottom); the cross-sectional AFM image (top) observed along the red line. In (a), the open circles refer to the  $I_D$ - $V_{DS}$  plots at  $V_G=0$  V. The brightness in the AFM image (bottom) refers to the unevenness of the surface. As the color brightens, the part is closer to the surface.

further reduced owing to the depletion of electrons in the channel region. The value of  $d$  for the layer was estimated to be 380 nm from the cross-sectional image of the scanning electron microscope (SEM) [Fig. 3(b)]. The  $\mu$  and  $V_T$  values of the FET device were determined to be  $4.1 \times 10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and 3 V, respectively, from the  $I_D$ - $V_G$  plots [Fig. 3(c)] at  $V_{DS}=5$  V with the relation,  $I_D = (\mu WC_0/L)(V_G - V_T)V_{DS}$  (Ref. 17). The  $C_0$  value was estimated to be  $8.3 \times 10^{-8} \text{ F cm}^{-2}$  from the experimental  $C$ . The  $\mu$  value estimated for the FET device is much lower than those,  $0.08$ – $0.56 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , of the  $C_{60}$  FETs with the  $\text{SiO}_2$  insulating layer.<sup>1,3,4</sup> Nevertheless, it should be noted that the  $V_{DS}$  and  $V_G$  values for the FET operation are smaller by one order of magnitude than those for the  $C_{60}$  FET with the  $\text{SiO}_2$  gate insulator. This result is based on the fact that the high concentration of carriers can be injected even at low  $V_G$  owing to the high  $\epsilon_x$  gate insulator; the  $N$  in the  $C_{60}/\text{BST}$  FET is  $5.2 \times 10^{12} \text{ cm}^{-2}$  at  $V_G=10$  V, which is comparable to that in the  $C_{60}/\text{SiO}_2$  FET at  $V_G=100$  V,  $5.1 \times 10^{12} \text{ cm}^{-2}$ . The low  $\mu$  value can be attributed to a large roughness in the surface of the BST layer. The value of  $D_{\text{max}}$  for the BST surface can be estimated to be  $\sim 35$  nm from the AFM image shown in Fig. 3(d); the BST layer was prepared by one-time annealing. Such a large roughness should suppress the carrier transport. The size of crystallite of the BST was estimated to be 20 nm from the x-ray diffraction peak ascribable to 100 reflection, and the size increased with an increase in annealing time at 700 °C. As the  $D_{\text{max}}$  decreased with an increase in annealing time, the increase in the annealing time may have caused the improvement of carrier transport.

The hydrophobic treatments of the BST thin films were carried out by immersing those into HMDS for 24 h at

300 K. The AFM showed the  $D_{\text{max}}$  of 10 nm for the HMDS-treated BST surface. The water contact angle increased from  $15^\circ$  to  $60^\circ$  by the HMDS treatment, showing that the BST surface changed to a hydrophobic situation. The  $I_D$ - $V_{DS}$  plots showed the  $n$ -channel properties with the  $\mu$  and  $V_T$  values of  $1.1 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $-5$  V, respectively. This shows clearly that the hydrophobic BST surface can increase the  $\mu$  value, although the origin remains to be clarified.

In summary, the flexible  $C_{60}$  FET device, which exhibits  $n$ -channel normally off properties, has been fabricated with a polyimide gate insulator on the PET substrate. Furthermore, the  $C_{60}$  FET device, which operates at low  $V_G$  and  $V_{DS}$ , has been fabricated with the high  $\epsilon_x$  gate insulator, BST. The FET device also showed  $n$ -channel FET properties. These should open a way towards high-performance fullerene FET devices exhibiting flexibility, portability, and low-voltage operation, and a way towards modification of electronic structure of  $C_{60}$  by high-carrier injection, i.e., a realization of novel physical properties.

This work was partly supported by the Mitsubishi Foundation and a Grant-in-Aid (No. 15350089) from the Ministry of Education, Culture, Sports, Science and Technology, Japan.

- <sup>1</sup>R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming, *Appl. Phys. Lett.* **67**, 121 (1995).
- <sup>2</sup>R. C. Haddon, *J. Am. Chem. Soc.* **118**, 3041 (1996).
- <sup>3</sup>S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, and Y. Iwasa, *Appl. Phys. Lett.* **82**, 4581 (2003).
- <sup>4</sup>T. Kanbara, K. Shibata, S. Fujiki, Y. Kubozono, S. Kashino, T. Urisu, M. Sakai, A. Fujiwara, R. Kumashiro, and K. Tanigaki, *Chem. Phys. Lett.* **379**, 223 (2003).
- <sup>5</sup>E. Kuwahara, Y. Kubozono, T. Hosokawa, T. Nagano, K. Masunari, and A. Fujiwara, *Appl. Phys. Lett.* **85**, 4765 (2004).
- <sup>6</sup>A. Dodabalapur, H. E. Katz, L. Torsi, and R. C. Haddon, *Science* **269**, 1560 (1995).
- <sup>7</sup>E. J. Meijer, D. M. De Leeuw, S. Setayesh, E. van Veenendaal, B.-H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, *Nat. Mater.* **2**, 678 (2003).
- <sup>8</sup>S. Kobayashi, S. Mori, S. Iida, H. Ando, T. Takenobu, Y. Taguchi, A. Fujiwara, A. Taninaka, H. Shinohara, and Y. Iwasa, *J. Am. Chem. Soc.* **125**, 8116 (2003).
- <sup>9</sup>Y. Kubozono, Y. Rikiishi, K. Shibata, T. Hosokawa, S. Fujiki, and H. Kiatagawa, *Phys. Rev. B* **69**, 165412 (2004).
- <sup>10</sup>K. Shibata, Y. Kubozono, T. Kanbara, T. Hosokawa, A. Fujiwara, Y. Ito, and H. Shinohara, *Appl. Phys. Lett.* **84**, 2572 (2004).
- <sup>11</sup>T. Nagano, H. Sugiyama, E. Kuwahara, R. Watanabe, H. Kusai, Y. Kashino, and Y. Kubozono, *Appl. Phys. Lett.* **87**, 023501 (2005).
- <sup>12</sup>T. Nagano, E. Kuwahara, T. Takayanagi, Y. Kubozono, and A. Fujiwara, *Chem. Phys. Lett.* **409**, 187 (2005).
- <sup>13</sup>P. R. L. Malenfant, C. D. Dimitrakopoulos, J. D. Gelorme, L. L. Kosbar, T. O. Grahama, A. Curioni, and W. Andreoni, *Appl. Phys. Lett.* **80**, 2517 (2002).
- <sup>14</sup>Y. Kato, S. Iba, R. Teramoto, T. Sekitani, T. Someya, H. Kawaguchi, and T. Sakurai, *Appl. Phys. Lett.* **84**, 3789 (2004).
- <sup>15</sup>S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits, Analysis and Design* (McGraw Hill, New York, 2003).
- <sup>16</sup>M. S. Dresselhaus, G. Dresselhaus, and R. C. Eklund, *Science of Fullerenes and Carbon Nanotubes* (Academic, San Diego, 1996).
- <sup>17</sup>S. M. Sze, *Semiconductor Devices, Physics and Technology* (Wiley, New York, 2002).