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Description	

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Transport properties of C_{60} thin film FETs with a channel of several-hundred nanometers

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Abstract

We report the transport properties of C_{60} thin film field-effect transistors (FETs) with a channel of several-hundred nanometers. Asymmetrical drain current I_D versus source-drain voltage V_{DS} characteristics were observed. This phenomenon could be explained in terms of the high contact-resistance between the C_{60} thin film and the source/drain electrodes. This device showed a current on/off ratio > 10^5.

Keywords: fullerene, C_{60}, transport property, field-effect transistor

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1. Introduction

The miniaturization of transistors enables us to put a billion transistors on a chip operating with the clock periods of a billionth of a second. However, as transistors get smaller in size, there are many undesirable effects, such as short-channel effects and the increase of off-current, *etc.*; moreover, quantum effects will become significant. To overcome these effects, a device based on a new principle of operation is required, such as a single-electron transistor (SET) [1]. In recent years, C_{60} has attracted considerable attention as the material for an island of SET because it can be regarded as an ideal quantum dot by itself.

C_{60} is a closed cage, nearly spherical molecule consisting of 60 carbon atoms with a diameter of about one nanometer. Its high symmetry results in a unique electronic structure, such as the three-fold degenerated lowest-unoccupied-molecular orbital (LUMO) and the five-fold degenerated highest-occupied-molecular orbital (HOMO) [2]. In addition, the electronic structure of a crystalline C_{60} is closely related to that of a free C_{60} molecule, because a crystalline C_{60} is a nearly ideal molecular crystal with van der Waals interaction. The quantized electronic levels are conserved even when C_{60} is in a cluster or a crystalline state.

An FET is a macroscopic system with dominant classic-mechanical effects, whereas an SET is a nano-scale system with dominant quantum-mechanical effects. The transport properties of C_{60} thin film FETs with a channel of several-decades micrometers [3,4] and of the C_{60} SET with an island of several nanometers [5] have been reported. In the marginal area between these systems, the mixed electronic state of a macroscopic system and a nano-scale one is expected. In this work, to clarify the C_{60} device properties in this marginal area, we have investigated the transport properties of C_{60} thin film FETs with a

channel of several-hundred nanometers.

2. Experimental details

Figure 1 shows the schematic cross section of the fabricated C_{60} thin film FET with a diagram of the measurement setup. The 34/26 nm Ti/Au source and drain electrodes were fabricated on the 100 nm SiO_2 layer that was made on the surface of a heavily doped *n*-type silicon wafer, using an electron-beam lithography system and a lift-off technique. The doped silicon layer of the wafer was used for a gate electrode. The distance between source and drain electrodes, *i.e.* the channel length, of the fabricated C_{60} thin film FETs was approximately 700 nm. Commercially available C_{60} (99.98 %) was used for the formation of the thin films. A C_{60} thin film of 12 nm thickness was formed on the SiO_2 layer using vacuum (< 10^{-4} Pa) vapor deposition at the normal deposition rate of 0.01 nm/s. The samples were annealed at 100 ºC for 40 h, then at 120 ºC for 12 h.

The drain and gate electrodes were biased with dc voltage sources and the source electrode was grounded. The transport properties of the samples were measured at room temperature under 10^{-3} Pa before and after annealing.

3. Results and discussion

Figure 2 shows the drain current I_D versus the source-drain voltage V_{DS} plots for various gate voltages V_G measured before annealing. The $/I_D/$ increases with increasing V_G. This result is consistent with the fact that a C_{60} molecule exhibits *n*-type semiconducting behavior [6]. These I_D versus V_{DS} plots show asymmetry characteristics, that is, the $/I_D/$s drastically increase only for the $V_{DS} < 0$. This phenomenon can be understood in terms of the high contact-resistance (HCR) between the C_{60} channel and the

source/drain electrodes. Figure 3(a) shows the model of the device circuit with the HCR; the series of HCR and relatively low resistance of the C_{60} channel are assumed. Figure 3(b) shows the model of the electric potential profile at the C_{60} thin film FET for $V_{DS} > 0$ V at $V_G = 0$ V. The vertical dotted lines demarcate the geometrical edges of the source and drain electrodes. The electric potential at the C_{60} channel becomes positive because the voltage significantly drops at the contacts with high resistance. Since the electric potential at the gate electrode becomes relatively negative compared to the electric potential at the C_{60} channel, a negative-gate-voltage, V_{G0} is effectively biased. (Here after, V_{G0} is defined as the effective voltage at the channel caused by the V_{DS}.) The $/I_D/$ tends to be suppressed because of the V_{G0} as the V_{DS} becomes positive. When a V_G ($\neq 0$) is biased, the effective-gate-voltage V_{Geff} at C_{60} channel is given by

$$V_{Geff} = V_{G0} + V_G \sim -\frac{V_{DS}}{2} + V_G . \quad (1)$$

Figure 3(c) shows the model of the electric potential profile at the C_{60} thin film FET for $V_{DS} < 0$ V at $V_G = 0$ V. The electric potential at the gate electrode is relatively positive to the electric potential at the C_{60} channel, where the V_{G0} becomes positive. The $/I_D/$ tends to be enhanced because of the effective positive-gate-voltage as the V_{DS} becomes negative. When a V_G ($\neq 0$) is biased, the electric potential at the C_{60} channel is also represented by equation (1).

Figure 4 shows the I_D versus V_{DS} plots for the gate voltage V_G varying between 10 and -10 V measured after annealing. The $/I_D/$s increase in contrast with those measured before annealing. In general, the *n*-type behavior of organic semiconductor is very sensitive to chemically and physically adsorbed O_2 and/or H_2O molecules, which can generate traps of electrons and suppress carrier transport [7-9]. Removing these molecules from the C_{60} channel by an annealing would cause the increase of $/I_D/$. In the region of $V_{DS} > 0$ V, for a

given V_G the I_Ds first increases linearly with increasing V_{DS}, then gradually levels off, and finally approaches a saturated value. This trend is different from that for $V_{DS} < 0$ V, but similar to that observed in conventional FETs. In this device, it is expected that the relative electric-potential-variation for $V_{DS} = -10$ V at $V_G = 0$ V will be the same as that for $V_{DS} = 10$ V at $V_G = 10$. The $/I_D/$s at these electric-potentials are in the range of 10^{-8} A for the former case and of 10^{-11} A for the latter case, whereas these values should be the same in our simple model. More factors in addition to the HCR would have to be considered. Figure 5 shows the $/I_D/$ versus V_G plot at $V_{DS} = -10$ V and $V_{DS} = 10$ V measured after annealing. The obtained current on/off ratios are larger than 10^5 at $V_{DS} = -10$ V and 10^2 at $V_{DS} = 10$ V, respectively. This difference cannot be explained only the model with HCR, because it may be resulted from additional effects. More detailed studies such as profiling the electric potential [10] and control of the contact resistance [11] will clarify these veiled characteristics in the crossover region in the channel between a macroscopic and a quantum size.

4. Conclusion

We have investigated the transport properties in short-channel C_{60} thin film FETs. The I_D versus V_{DS} plots showed asymmetry characteristics, that is, the $/I_D/$ drastically increased only for the $V_{DS} < 0$. The current on/off ratios, $> 10^5$ at $V_{DS} = -10$ V and $> 10^2$ at $V_{DS} = 10$ V, were estimated from the $/I_D/$ versus V_G plots. Clarifying these properties will open a way to fabricate practical devices of a size between macroscopic and nano-scale.

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Figure Captions

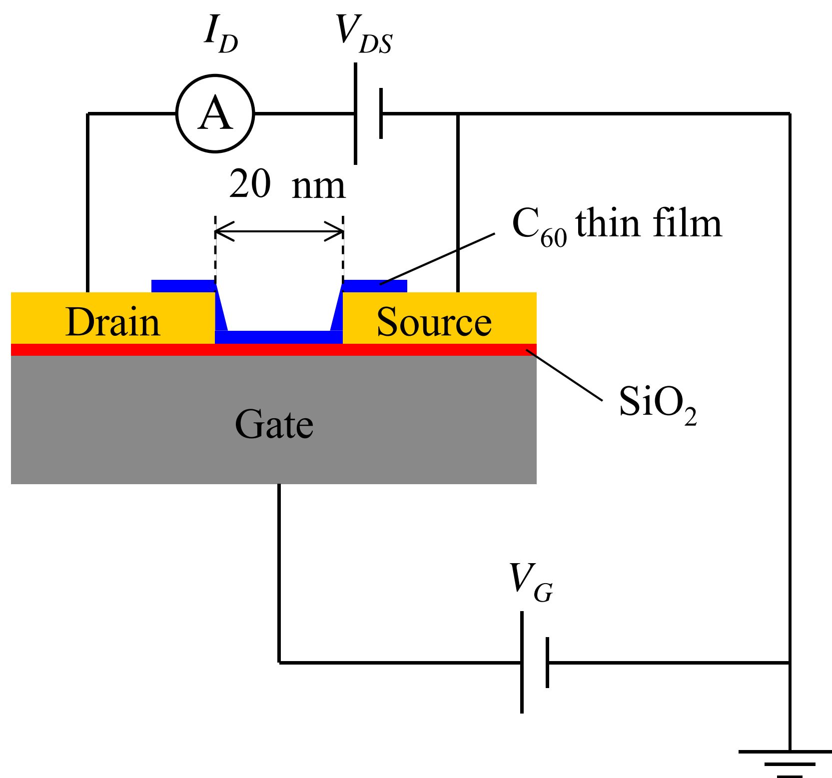
Figure. 1 Schematic cross section of the fabricated C_{60} thin film FET (700 nm channel length) with a diagram of the measurement setup.

Figure. 2 I_D versus V_{DS} plots for various V_G measured before annealing.

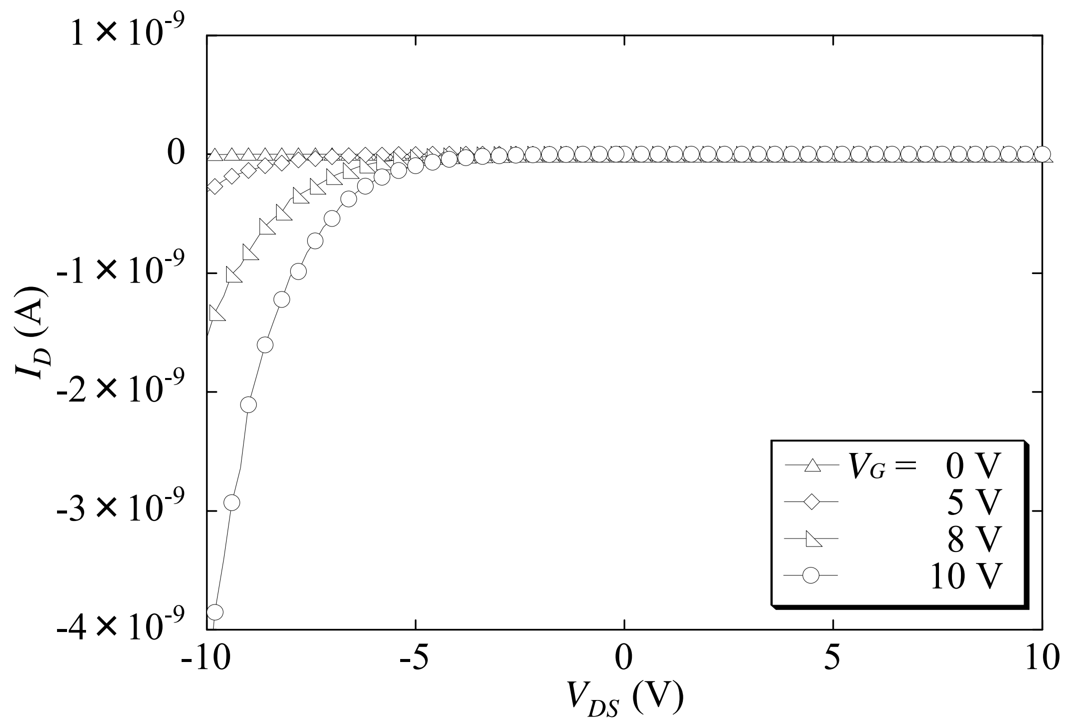
Figure. 3 Model of the V_{G0} because of the high-contact resistance (HCR). Here, we assume HCRs and relatively low resistance of the channel to be connected in series. (a) Schematic cross section of the C_{60} thin film FET with HCR and resistance of the channel. (b) Model of the electric potential profile for $V_{DS} > 0$ at $V_G = 0$. (c) Model of the electric potential profile for $V_{DS} < 0$ at $V_G = 0$. The vertical dotted lines indicate the edges of the source and drain electrodes.

Figure. 4 I_D versus V_{DS} plots for the V_G varying between 10 and -10 V measured after annealing. The I_Ds for $V_{DS} < 0$ and for $V_{DS} > 0$ are shown on the left vertical axis and the right vertical axis, respectively.

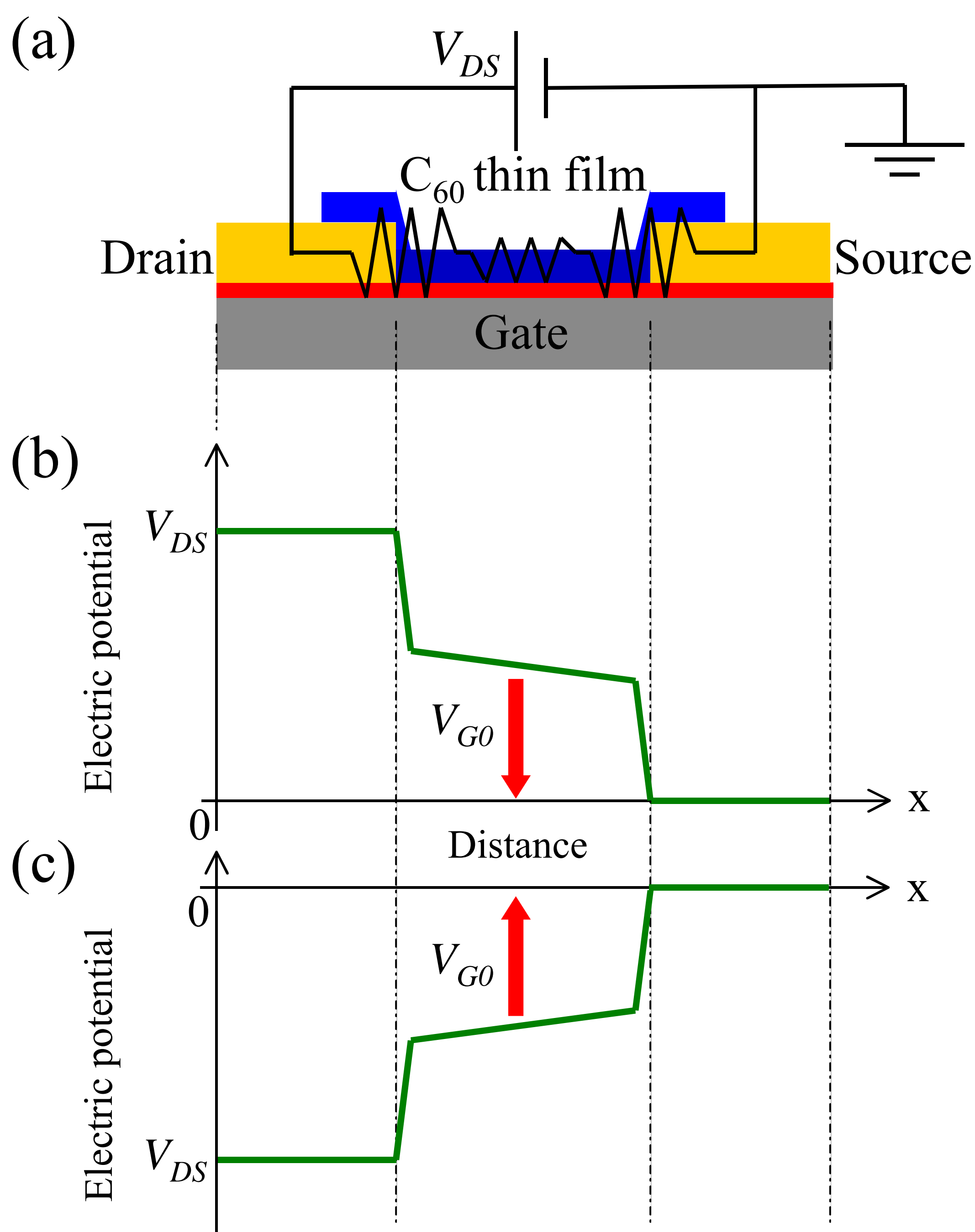
Figure. 5 $|I_D|$ versus V_G plots at V_{DS} = -10 V and V_{DS} = 10 V measured after annealing.



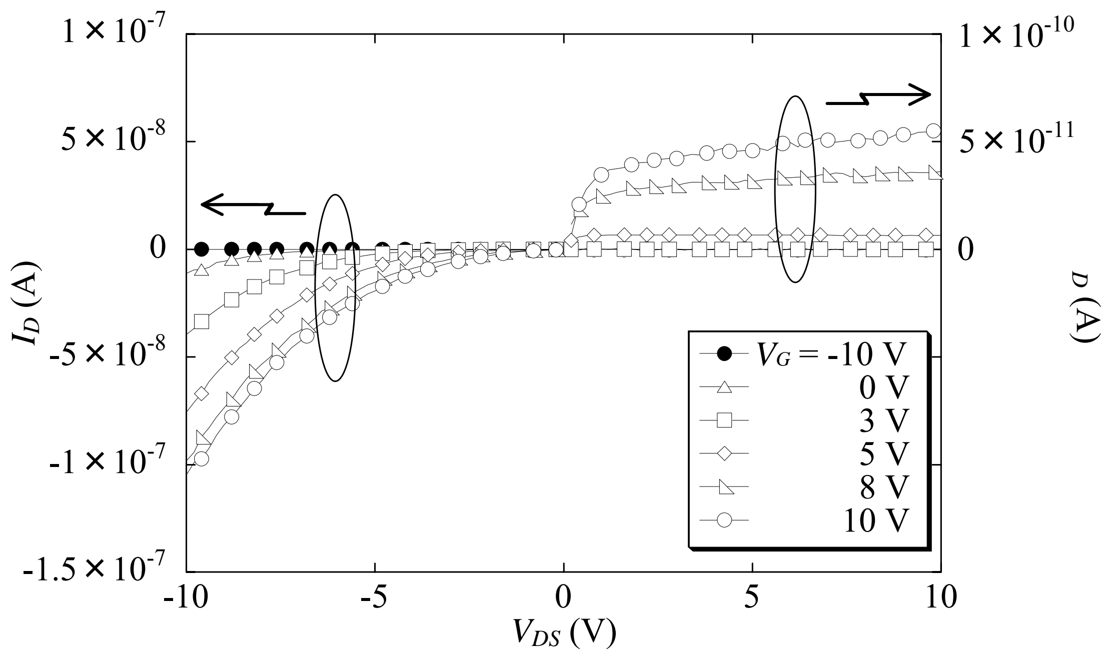
Y. Matsuoka et al. Figure 1.



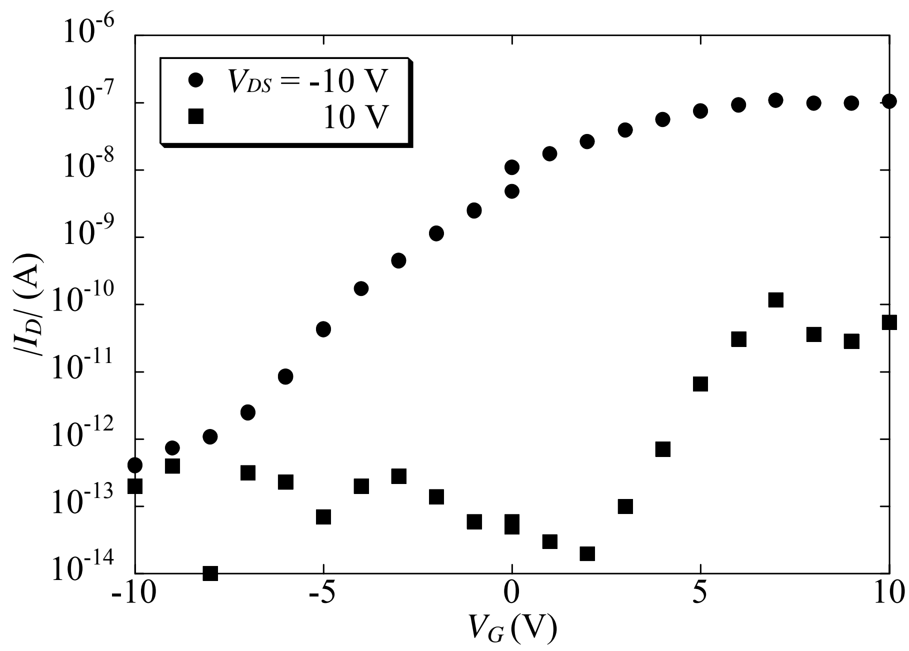
Y. Matsuoka et al. Figure 2.



Y. Matsuoka et al. Figure 3.



Y. Matsuoka et al. Figure 4.



Y. Matsuoka et al. Figure 5.