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Research on Low Power Consumption of Cache Memory by Self-Invalidation

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1 Introduction

Recently, semiconductor process technique is improving and transistors are shrinking in size. Therefore, processor's speeds are dramatically upgraded. On the other hand, since leakage currents of a transistor are becoming too larger to ignore, the power consumption of a processor is increasing. This affects battery life of mobile devices. Recent mobile devices are required to have high-performance and long battery life. Consequently, it is important to reduce power consumption of a processor while maintaining its high-performance.

Today, a cache memory accounts for a large area of a processor. Also recently, chip multiprocessors that have multiple processors in a single-chip are becoming mainstream. For these reasons, I propose a technique for reducing power that the cache memory of a chip multiprocessor consumes without the overhead of program execution in this research.

2 Related Works

Many researchers are interested in the power consumption of a processor, and it's an object of many researches to reduce the leakage currents

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of a cache memory.In this chapter, I introduce some researches on low power consumption of a cache memory. I also explain cache coherency for multiprocessor environment. And, I introduce established techniques of self-invalidation that aimed at reduction of the overhead to keep cache coherency.

3 Proposal Technique

In this research, I propose a software self-invalidation technique to reduce power consumed by a cache memory. The conventional techniques of self-invalidation is the means by hardware. Therefore, they are not appropriate for reduction of power consumption, because additional hardware is required for the techniques. The software self-invalidation I propose is implemented with last-touch memory reference instructions which invalidate the cache block immediately after the memory reference. Of all normal memory reference instructions, ones that satisfy either of the following conditions are replaced to the last-touch memory reference instructions.

condition 1 referred address makes sure to receive an invalidate message

condition 2 referred address will be never accessed by the same processor

Also, last-touch memory reference instructions are classified into the following two kinds of instructions.

last-touch block (ltb ld/st) This instruction performs normal read from (writes to) memory, and invalidates the accessed cache block.

last-touch word (ltw ld/st) This instruction performs normal read from (writes to) memory, and marks an accessed word in the cache block. When all words in the cache block are last-touched, the block becomes invalid state.

To implement the last-touch word instruction, we tack on necessary infomation to the cache tag.

I use gated-Vdd as a mechanism to reduce power consumption of a cache, and a valid bit of a cache tag as its control signal.

4 Evaluation

I evaluate the proposal technique by simulation. The target to evaluate is a 2-core chip multiprocessor that has private L1 data and instruction cache per processor core. Benchmark programs are FFT, LU, RADIX and CHOLESKY in SPLASH-2. I mainly evaluate the reduction rate of power consumed by the L1 data cache when applying the proposal technique to each program.

To choose instructions to be replaced by the last-touch memory reference instructions, I employ an algorithm based on traces of memory accesses. I replace only instructions that certainly have last-touched reference address.

From results of simulation, the technique could reduce power consumption of L1 data cache by up to 46%. The power reduction rate is roughly proportional to the number of invalidations from other processor and software self-invalidations. In addition, program execution with the proposed technique could decrease cache misses, and reduce execution time.

5 Conclusions

In this thesis, I examined a technique to reduce power consumption for cache memory of a chip multiprocessor. I proposed the system using cache's valid bit to control gated-Vdd. I also proposed software self-invalidation to increase the number of invalid cache blocks. From results of evaluation, I obtained an effect of power reduction for all benchmark programs I had executed.