JAIST Repository
https://dspace.jaist.ac.jp/

Title	Study on Integrated Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode
Author(s)	Trinh, Bui Nguyen Quoc
Citation	
Issue Date	2007-09
Type	Thesis or Dissertation
Text version	none
URL	http://hdl.handle.net/10119/3758
Rights	
Description	Supervisor:Susumu Horita, 材料科学研究科, 博士

JAIST
JAPAN
ADVANCED INSTITUTE OF
SCIENCE AND TECHNOLOGY

Japan Advanced Institute of Science and Technology

Study on Integrated Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode

Laboratory of Semiconductor Materials
Bui Nguyen Quoc Trinh
Student Number: 440209

Introduction

Ferroelectric gate field-effect transistors (FeFETs) are well known as field-effect transistor (FET) type memory, in which the gate insulator is a ferroelectric material. This FeFET memory has attracted much attention because it has prominent advantages such as nonvolatile, nondestructive readout, low writing voltage, fast writing speed, high endurance and high packing density. However, it is very difficult to fabricate an FeFET with perfect memory ability. If a ferroelectric film is directly deposited on a Si substrate, the constituent atoms from the deposited ferroelectric film, such as Pb and Bi, easily diffuse into the Si substrate, and thus, the interfacial electrical properties become very poor. Generally, a buffer layer with a high dielectric constant is inserted between the ferroelectric film and Si substrate, forming a metal–ferroelectric–insulator–semiconductor structure (MFIS). Many researchers reported that, using this MFIS structure, the retention time has a tendency to be very short because the generation of leakage current to/from the Si and a reduction in the remnant polarization are caused by the essentially preserved charge on the insulator layer. Furthermore, a high writing voltage is needed because of the voltage drop at the insulator and transistor layers. In order to solve these issues of the conventional FeFET memories, a FeFET memory with an intermediate electrode for data writing (called as IF-FET) was investigated. With the intermediate electrode of IF-FET memory, a writing voltage is lowered because it is applied only to the ferroelectric capacitor, and a long retention time is expected by keeping the remnant polarization state under zero bias condition without preserving charge on the gate of MOSFET.

The main goal of this study is to fabricate a well-operative IF-FET memory integrated on Si substrate, and to find new writing and reading methods for improvement in the nondestructive readout of IF-FET.

Operational Principle of IF-FET Memory

Figure 1 shows the schematic basic circuit of IF-FET memory which consists of a ferroelectric capacitor C_f connected serially to an n-channel reading MOSFET transistor (R-FET). For data-writing, we apply a writing pulse voltage V_W only to the C_f directly using the intermediate electrode. Then, the polarization state of the C_f is

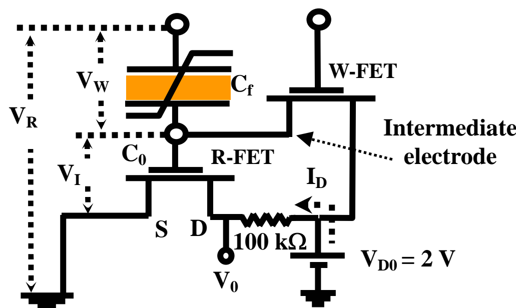

Fig. 1: Schematic basic circuit of IF-FET memory for investigating the memory operation.

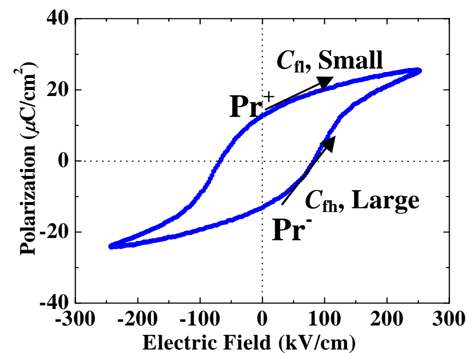

Fig. 2: A typical polarization-electric field (P-E) hysteresis loop of the ferroelectric capacitor with 200-nm-thick poly-PZT film.

set positive (P_r^+) for $V_W > 0$ or negative (P_r^-) for $V_W < 0$. Although the W-FET for data-writing is connected to the R-FET, we did not use it in this study.

For data-reading, a positive reading voltage V_R is applied between the top electrode and the source of R-FET. Because the C_f for Pr^+ (C_{fl}) is much smaller than that for Pr^- (C_{fh}) when $V_R > 0$ (see Fig. 2), the drain current I_D for the P_r^- state is larger than that for the P_r^+ state owning to intermediate voltage $V_I = C_f V_R/(C_f + C_0)$, where C_0 is the input capacitor of the MOSFET. Thus, by detecting the I_D the memory state can be read.

Experimental Method

For fabrication of the IF-FET memory, a 6-nm-thick SiO_2 was used as a buffer layer at the gate of MOSFET because the interface between SiO_2 and Si is the most ideal. Then, on the SiO_2, a double-layer structure consisting of a 700-nm-thick Pt film and a 60-nm-thick RuO_x film was formed as the bottom electrode by sputtering, in order to suppress the fatigue properties of the memory because oxygen in RuO_x can supply to the PZT film. Since SiO_2 is amorphous without crystallographic information, 200-nm-thick $Pb(Zr_{0.52}Ti_{0.48})O_3$ (poly-PZT) films prepared by sputtering as ferroelectric layers of the IF-FET memory were polycrystalline, which is favorable for industry aspect because of the easy and low cost technique of mass production. Actually, for PZT film deposition, a thin PZT seed layer was deposited at 600°C for a short time of 2 min, followed by an amorphous PZT layer deposited at 300°C for 28 min, and then it was crystallized at around 600°C for 15 min in air.

To evaluate nondestructive characteristics, after only one data writing, the memory state was readout 10 times with an interval of 1 min after each readout. During retention, the top electrode was grounded together with the source and drain of the R-FET transistor, the intermediate electrode was floated, and the gate of W-FET is grounded.

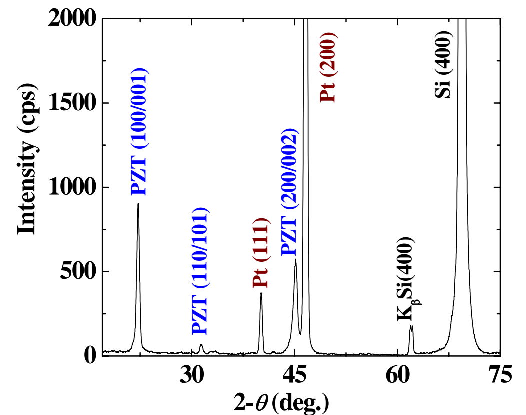

Fig. 3: XRD patterns of the normal PZT film deposited on (a) the highly (100)-oriented Pt films on the $RuO_x/SiO_2/Si$ substrate.

Results and Discussion

It was found that the preferential orientation of Pt films deposited on the $RuO_x/SiO_2/Si$ substrates depends on the sputtering power, pressure and deposition time. The preferential orientation of the Pt film can be explained by considering surface energy and strain energy in the Pt film. If the contribution of surface energy to the difference in overall energy is predominant, the preferential orientation tends toward Pt(111), but if that of strain energy is predominant, the preferential orientation tends toward Pt(100). In fact, the highly (100)-oriented Pt films were successfully prepared, as seen from the high (200) Pt peak in Fig. 3. As a result, the (100/001)-oriented PZT film was successfully grown on the highly (100)-oriented Pt film on $RuO_x/SiO_2/Si$ substrate by sputtering as shown in Fig. 3. Also, PtO_x/RuO_x double layer as a top electrode was used in order to reduce leakage current. By using the PtO_x/RuO_x

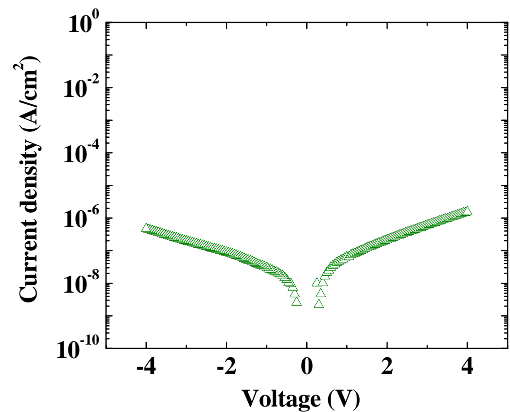

Fig. 4: I-V characteristics of the A-PZT film crystallized at 600°C after the RuO_x/PtO_x double top electrodes annealed at 450°C.

double top electrode the leakage current density is about 10^{-6} A/cm^2 at ± 4 V as shown in Fig. 4, whereas it is about 10^{-5} A/cm^2 by using the RuO_x single top electrode.

Figure 5 shows the photograph of the integrated IF-FET memory cell fabricated on a p-type Si substrate (a) and the schematic drawing of one cell (b). Threshold voltage of the R-FET is determined to be about 1.2 V.

For conventional data-writing, two positive and negative square pulses of 3.5 V induced the Pr^+ and the Pr^- memory states as shown in Fig. 6 (a), respectively. For conventional data-reading, a unipolar square pulse train of 3.5 V was applied as shown in Fig. 6 (b). Ideally, the readout operation of IF-FET memory should be nondestructive as an ultimate FeFET memory. However, actually, it was found that the IF-FET memory showed destructive readout, especially for the Pr^- memory state. In fact, although the initial difference in output voltage between Pr^+ and Pr^-, ΔV_0 was 0.98 V, the differences decreased with number of reading. This poor nondestructive readout for the Pr^- was resulted from large amount of nonreturned domain from negatively polarized domains.

Therefore, we proposed new data writing and reading methods. For the new data-writing, we used the Pr^+ state and the Pr^0 state instead of the Pr^- state. The new Pr^0 was used to reduce the amount of negatively polarized domains in data writing. The Pr^0 was induced by a combined pulse with a positive voltage (V_W^+) and a negative voltage (V_W^-). The degree of polarization can be controlled by adjusting the V_W^-. For the new data-reading, a negative voltage V_R^- was applied, following a positive voltage V_R^+ in order to reduce amount of nonreturned domains. By increasing the V_R^-, the switched positive domains due to V_R^+ can be reswitched to the initial states, and the memory state can be recovered after each reading, which means that the nondestructive readout can be improved. However, because the small V_W^- makes the ΔV_0 between Pr^+ and Pr^0 reduce and the large V_R^- makes the nondestructive readout for the Pr^+ degrade, we optimized the amplitude of V_W^- and V_R^-.

The V_W^+ was determined from the polarization-voltage *P-V* hysteresis loop of the C_f, at which the saturation of polarization begins. The V_W^- was adjusted around $-V_W^+/2$ from viewpoints of output voltage and

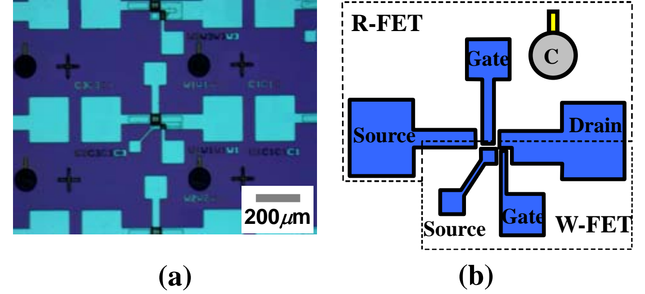

Fig. 5: (a) Photograph and (b) schematic drawing of the integrated IF-FET memory cell. F-FET consists of a ferroelectric capacitor C_f connected serially to an n-channel MOSFET (R-FET). W-FET is used as a switch for data writing, and C has the same structure with the C_f for checking ferroelectric properties.

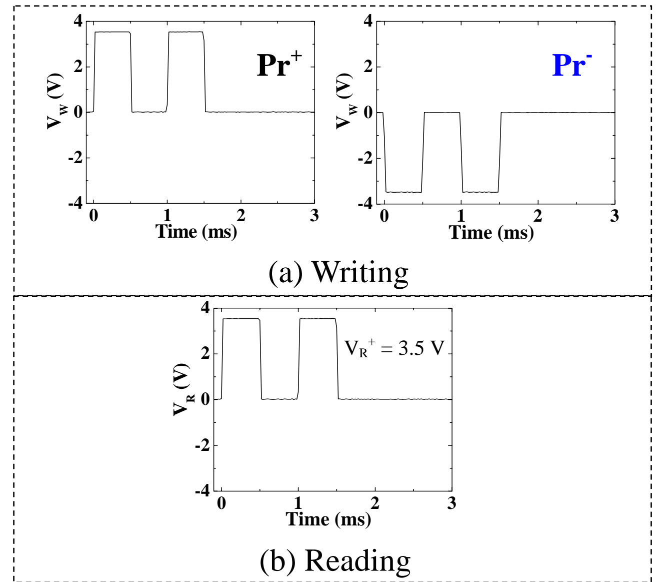

Fig. 6: Conventional method: (a) writing pulses for Pr^+ and Pr^- and (b) reading pulse.

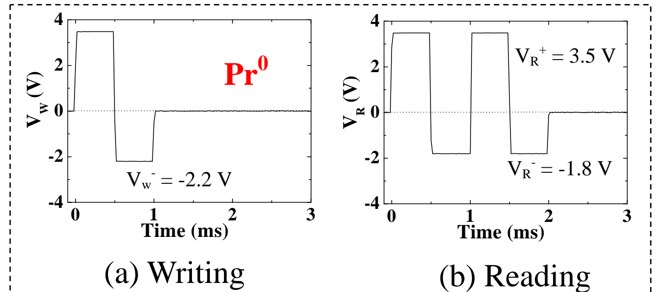

Fig. 7: New method: (a) writing pulse for Pr^0 instead of Pr^- and (b) reading pulse.

nondestructive characteristics. The V_R^+ was determined from analyzing the memory operation, and the V_R^- was optimized from a viewpoint of the nondestructive characteristics. The actual values are shown in Fig. 7. As a result, when the Pr^0 was induced by a combined pulse with $V_W^+ = 3.5$ V and $V_W^- = -2.2$ V, and a new reading voltage with $V_R^+ = 3.5$ V and $V_R^- = -1.8$ V was applied, the nondestructive readout characteristics were further improved although the ΔV_0 was reduced by 21%, compared with the conventional method.

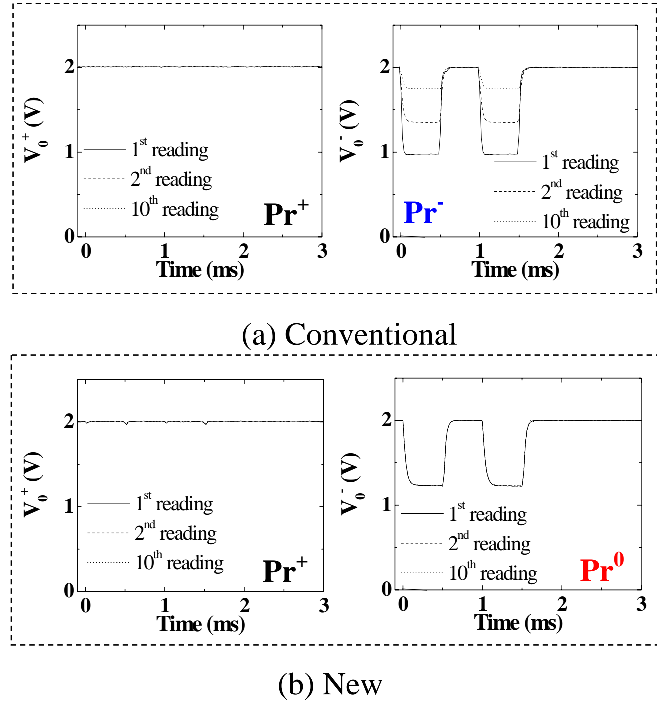

Fig. 8: Nondestructive readout characteristics: (a) previous writing and reading method and (b) new method.

Conclusions

A highly (100)-oriented Pt film prepared by sputtering plays a role as a seed layer so that a mainly (100/001)-oriented PZT film was successfully grown on it.

An integrated IF-FET was successfully fabricated on Si wafer. The nondestructive readout characteristics of the integrated IF-FET were obtained by using the new writing and reading methods. Therefore, it is expected that the new method will promote commercialization of IF-FET in future as a proper substitute for conventional FeFET.

Table of Contents

Chapter 1 Introduction………………………………………………………………………. 1
Chapter 2 Experimental Procedures and Film Characterization…………………………………..... 22
Chapter 3 Control of Preferred Orientation of Pt Film ……………………………………………. ..44
Chapter 4 Crystalline and Electric Properties of PZT Film……………………………………… 57
Chapter 5 Discrete Circuit of IF-FET Memory…………………………………………………….. 71
Chapter 6 Fabrication of Integrated IF-FET Memory…………………………………………… 92
Chapter 7 Conclusions and Future Work ………………………………………………………….. 105

List of Publications

1. **Bui Nguyen Quoc Trinh** and Susumu Horita, *Operation of Ferroelectric Gate Field-Effect Transistor Memory with Intermediate Electrode using Polycrystalline Capacitor and Metal–Oxide–Semiconductor Field-Effect Transistor*, Japanese Journal of Applied Physics, Vol. 45, 7341–7344 (2006).
2. **Bui Nguyen Quoc Trinh** and Susumu Horita, *Control of Preferential Orientation of Platinum Films on $RuO_2/SiO_2/Si$ Substrates by Sputtering*, Japanese Journal of Applied Physics, Vol. 45, 8810-8816 (2006).