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Lattice-mismatched heteroepitaxy and epitaxial lift-off of metamorphic In(Ga,Al)As materials

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I. Introduction

III-V compound semiconductor materials are promising for applications in the higher speed devices demanded for wireless communications of today. In particular, devices on InP substrates exhibited excellent speed performance [1]. However, InP substrates have many practical problems in comparison with GaAs substrates. On the other hand, In(Ga,Al)As metamorphic devices on GaAs substrates have been extensively developed, and exhibited performance equivalent to that of the InP devices [2]. The In(Ga,Al)As metamorphic devices can be alternatives to devices on InP substrates. Moreover, they can offer a freedom of choice of indium content, which should be optimized as a device parameter considering trade-off between speed and power performance [3]. Importance of the In(Ga,Al)As metamorphic devices is a rising trend in high speed analog electronics.

An important issue of the metamorphic devices is the reduction of crystalline defects, such as dislocations and stacking faults. InAlAs graded buffers with the intermediate contents have been widely employed to reduce the defects in the device layer. However, understanding of dislocation density reduction by using graded buffers is still insufficient. Therefore, one of the purposes of this work is to obtain an insight into the mechanism of dislocation density reduction in metamorphic lattice-mismatched growth, through the lattice-mismatched growth and characterizations of In(Ga,Al)As materials on GaAs.

The thicker buffers should be employed to obtain lower defect density in the device layer. However, the thicker buffers containing a high density of defects often cause unfavorable influences on the device layer. In addition, material choice for the buffer layers is strongly restricted to reduce the leakage current or parasitic capacitance. To solve these problems, we propose a new application of the epitaxial lift-off (ELO) process to the metamorphic lattice-mismatched growth. The ELO process has been recognized to be important as the basis for heterogeneous integration technology [4-6]. Although lattice-matched ELO has been extensively investigated, lattice-mismatched ELO has hardly been investigated and reported at all. Therefore, another purpose of this work is to realize the proposed new application of ELO to lattice-mismatched growth, using ELO of highly lattice-mismatched InAs thin films and ELO of InGaAs/InAlAs metamorphic high electron mobility transistor (MHEMT) structures on the GaAs substrates.

II. Experimental details and discussion

Chapter 2. Lattice-mismatched growth of In(Ga,Al)As

Several InAs samples were grown on semi-insulating GaAs (001) substrates using direct growth (DG) and graded-buffer growth (GBG). In the GBG, InAlAs step GBs with 17 steps (1.7 μm) were employed, where each step thickness was 100 nm and the indium content was increased from 0.15 to 0.95 by increments of 0.05. As shown in Figure 1(b), we observe for the 1 μm thickness, the GBG of $In_{0.5}(Ga,Al)_{0.5}As$ is strongly effective in comparison with the DG for the TD density, D, reduction. For the DG of InAs samples, the obtained D is inversely proportional to epilayer thickness, l, due to the pair-annihilation mechanism [7]. The GBG of InAs exhibits almost same TD densities with the DG of InAs. The GBG of InAs is not effective in reducing the TD density under a comparison using the same total grown layer thickness. These can be attributed to alloy hardening by solid solution. Increased alloy may cause higher pinning force, which eventually causes lower mobility and pair-annihilation probability of dislocations. The high TD density in DG of $In_{0.5}(Ga,Al)_{0.5}As$ on GaAs may be due to a possibility of this alloy hardening in crystals. On the other hand, there is a difference in the GBG for $In_{0.5}(Ga,Al)_{0.5}As$ on GaAs and InAs on GaAs. In the case of the $In_{0.5}(Ga,Al)_{0.5}As$ on GaAs, the dislocations have a tendency to be confined in the lower indium contents region by the alloy-hardening gradient. In the case of the InAs on GaAs, above the intermediate contents, the alloy-hardening gradient becomes inverted. Thus, the confinement of dislocations will become relatively weak. The effectiveness of the GB below the intermediate indium contents would be faded away by the influence from the region above the intermediate contents according to the alloy-hardening gradient.

Chapter 3. Epitaxial lift-off of lattice-mismatched InAs

Figure 2 exhibits a proposed new application of ELO process to metamorphic lattice-mismatched growth. For

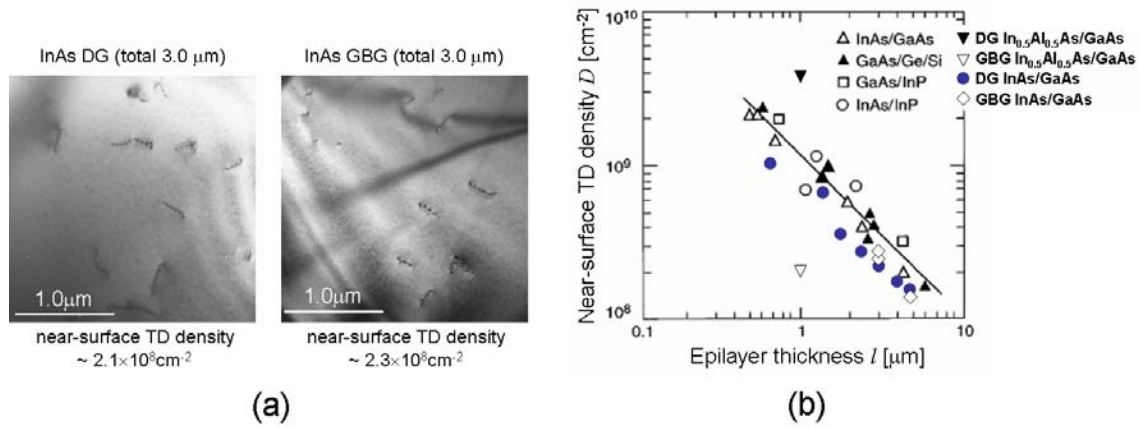

Fig. 1: (a) One each of the obtained plane-view transmission electron microscope (TEM) images for the InAs DG samples and for the InAs GBG samples, and (b) TD density as a function of epilayer thickness; addition of the obtained TD densities to data of reference [8].

the new application, we have grown the following heterostructures: InAs(1.7 μm)/AlAs/InAs(2.3 μm)/GaAs, where the thin AlAs sacrificial layers were employed, with thicknesses of 1.5 nm, 4.0 nm, and 5.0 nm (Figure 3(a)). On the other hand, the ELO process was successfully realized only for the heterostructure with the AlAs 5.0 nm. The AlAs 5.0 nm seems to be suitable for the lattice-mismatched sacrificial layer considering the trade-off between the crystal qualities of the InAs top layer and easiness of the ELO process. The InAs top layer is separated by the ELO process using selective etching of the AlAs sacrificial layer with the 12.5 % HF diluted solution. The separated InAs top layer is bonded on SiO_2/Si substrate using van der Waals bonding (VWB) (Figure 3(b)). The electron transport property of an obtained ELO InAs layer on the SiO_2/Si was characterized by Hall measurements with a van der Pauw sample of $\sim$5$\times$5 mm^2. As shown in Figure 3(c), the ELO InAs sample exhibits higher electron mobility, indicating better crystal quality than that of the reference sample. The room temperature mobility of 11600 cm^2/V-s is the highest electron mobility ever reported for ELO thin films.

Chapter 4. Epitaxial lift-off device fabrication using lattice-mismatched In(Ga,Al)As heterostructures

For the new application, we have grown several InGaAs/InAlAs MHEMT structures with thin sacrificial layers. A suitable structure for ELO as shown in Figure 4(a) is following: we have grown the buffers consisting of an $In_xGa_{1-x}As$ step GB and an $In_{0.56}Al_{0.44}As$ buffers. The InGaAs step GB has x=0.19$\rightarrow$0.62 with Δx=0.054 and 100 nm each step thickness and $In_{0.56}Al_{0.44}As$ buffer has 100 nm thickness. After the growth of the buffer, a very thin AlAs sacrificial layer of 3.0 nm thickness was grown. Finally, we have grown a modulation-doped InGaAs/InAlAs metamorphic device layer consisting of an $In_{0.56}Al_{0.44}As$ (1.9 μm), an $In_{0.57}Ga_{0.43}As$ channel (30 nm), an $In_{0.56}Al_{0.44}As$ spacer (20 nm), a Si δ-doping (5$\times$10^{12} cm^{-2}), an $In_{0.56}Al_{0.44}As$ barrier (40 nm), an $In_{0.57}Ga_{0.43}As$ (10 nm). The indium contents were precisely confirmed by symmetric and asymmetric X-ray diffraction measurements. We have employed slightly higher indium contents than the InP lattice-matched system, according to the freedom of choice regarding the indium contents. Hall-bar samples as shown in Figure 4(b)

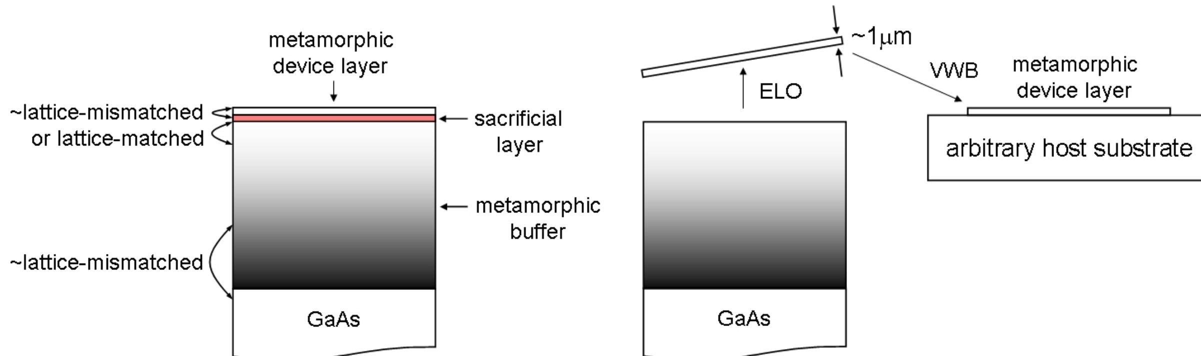

Fig. 2: A proposed new application of ELO process to metamorphic lattice-mismatched growth.

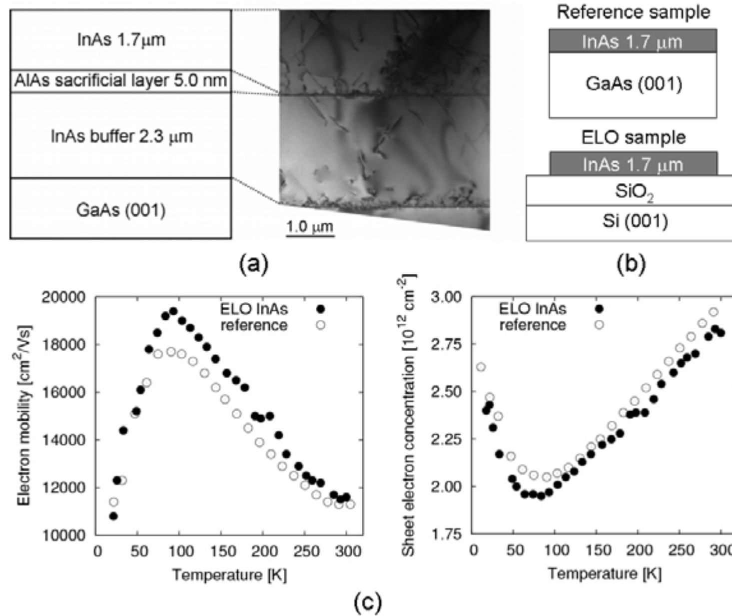

Fig. 3: (a) A cross-sectional TEM (XTEM) image of the heterostructure with the AlAs 5.0 nm, (b) A schematic of the reference and the ELO InAs sample bonded on SiO_2/Si, and (c) temperature dependence of electron mobilities and sheet electron concentrations of the reference and the ELO InAs sample bonded on SiO_2/Si.

for electrical characterization were fabricated as follows. After mesa-etching using the resist, the sacrificial layer etching of the sample with the resist was carried out with the 12.5 % HF diluted solution. The sample with the substrate is moved from the HF solution into deionized water, in which the sample with the resist in deionized water as shown in Figure 4(c)-top is transferred onto the AlN substrate. After drying, the resist is removed by O_2 plasma ashing. By dropping a small amount of water near the interface between the sample and the AlN, and subsequent drying, we can obtain a sufficiently firm VWB for the following electrode formation process. Figure

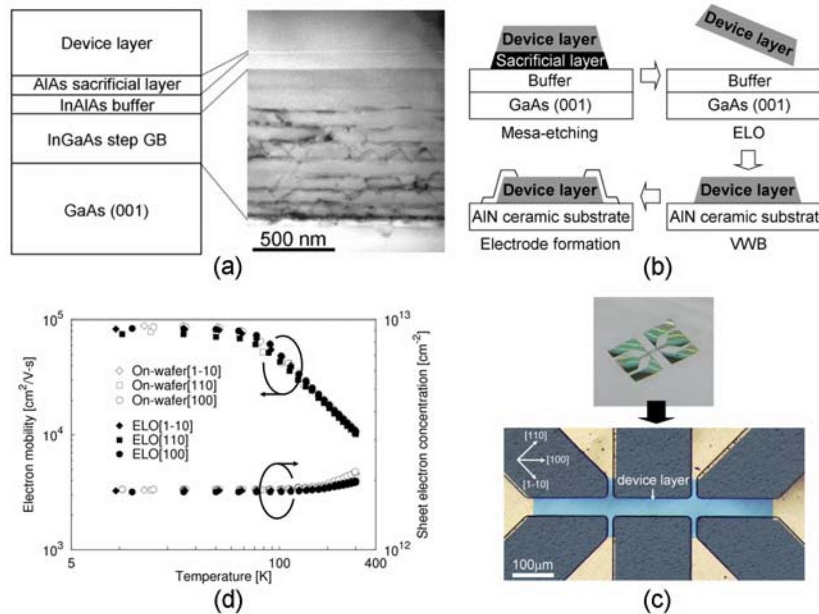

Fig. 4: (a) An XTEM image of the MHEMT structure for ELO, (b) A schematic of device fabrication process, (c) A separated device layer in deionized water during the process (top) and a successfully fabricated Hall-bar device on AlN ceramic substrates (bottom), and (d) temperature dependence of electron mobilities and sheet electron concentrations of the ELO and the on-wafer Hall-bar devices for several crystal directions.

4(c)-bottom image exhibits a successfully fabricated Hall-bar device on AlN ceramic substrates. As shown in Figure 4(d), we obtained very high electron mobilities for the ELO Hall-bar devices, such as 11000 cm^2/V-s at room temperature, and 84000 cm^2/V-s at 12 K, owing to the high indium content and the successful ELO and VWB processes. The room temperature mobility of 11000 cm^2/V-s is the highest ever reported for ELO devices.

III. Conclusions and Perspectives to future work

The GBG of InAs on GaAs is not effective in reducing the InAs near-surface TD density in comparison with the DG, despite its effectiveness for In(Ga,Al)As below the intermediate indium contents. This may be attributed to the fact that the effectiveness of the GB below the intermediate indium contents would be faded away by the influence from the region above the intermediate contents according to the alloy-hardening gradient.

Using the InAs sample with AlAs 5.0 nm sacrificial layer, we successfully realized the ELO of InAs thin films and the VWB on SiO_2/Si substrates, and the obtained ELO InAs films exhibited good electron transport properties. In addition, using a suitable MHEMT structure with AlAs 3.0 nm sacrificial layer for ELO, we have fabricated the ELO Hall-bar devices on the AlN ceramic substrates, and the obtained ELO Hall-bar devices exhibited excellent electron transport properties due to successful ELO and VWB.

We consider that lattice-mismatched ELO technology will be useful for future analog and digital electronic, and optical device applications, in addition to photovoltaic device applications.

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Publications

1. **Y. Jeong**, M. Shindo, H. Takita, M. Akabori, and T. Suzuki: "Structural, optical, and electrical characterizations of epitaxial lifted-off InGaAs/InAlAs metamorphic heterostructures bonded on AlN ceramic substrates" Phys. Stat. Sol. (c), *to be published.*

2. **Y. Jeong**, M. Shindo, M. Akabori, and T. Suzuki: "Epitaxial lift-off of InGaAs/InAlAs metamorphic high electron mobility heterostructures and their van der Waals bonding on AlN ceramic substrates" Appl. Phys. Express **1**, 021201 (2008).

3. **Y. Jeong**, H. Choi, and T. Suzuki: "Invalidity of graded buffers for InAs grown on GaAs(001) —A comparison between direct and graded-buffer growth" J. Crystal Growth **301-302**, 235 (2007).

4. H. Choi, Y. Kitta, T. Kakegawa, **Y. Jeong**, M. Akabori, T. Suzuki, and S. Yamada: "Spin-orbit Interactions in High In-content InGaAs/InAlAs Inverted Heterojunctions for Rashba spintronics Devices" AIP Conference Proceedings **893**, 1373 (2007).