A Constitution Method of the Three Valued Logic Memory System with CMOS Operation

Tatsuhiko Shiota(610702)
School of Information Science,
Japan Advanced Institute of Science Technology

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1 Introduction

The embedded systems such as communication equipments support our convenient life.The core technology is very large scale integration, called VLSI or ULSI. Although these technologies accomplish remarkable high density, people pursue further convenience for those equipments and require higher density integration with more functions.

However, current two valued digital system constitution cannot avoid problems such as increase of inside wiring area or lack of input or output pins. It is said that the wiring area, in particular, occupies 70 per cents of the integrated circuit active area.

Multiple valued signal lines can be expected to accomplish higher density integration by increasing information per line, that is, reducing inside wiring area and number of input or output pins.

In this paper, the author adopts the three valued logic that is expected that more efficient information per line than the two valued logic and the most efficient simplification of logic circuit constitution in other multiple value logics, and proposes a constitute-on method of three valued logic memory system that is the most significant component of the digital systems.

There were no three valued logic memory element without power consumption in the stable state. The memory element that the author proposes in this paper operates on the perfect CMOS principle.

In addition, the author suggests the design flows from three valued logic circuits to realization of the memory system.

2 Three Valued Logic

Various investigations on the multiple valued logic are conducted up to today, because the idea of the multiple valued logic seems that it have ability of human-like processing includes ambiguity that the two valued logic cannot express.

In recent years, especially expectation to the multiple valued logic integrated circuits which realize high density integration.

Also, the three valued logic is applied to calculation of the field with characteristic 3 and reported improvement of calculation efficiency and simplification of constitution of Public Key Cryptography Hardware.

3 CMOS Operation

The three valued logic circuit constitution premises on CMOS operation of the two valued logic circuit constitution.

The term CMOS operation here is that, since MOS transistors act on the threshold voltage of gates, two kinds of MOS transistors, pMOS and nMOS, act complementarity symmetry. In the case of the three valued logical circuit constitution, the constitution is same as conventional two valued logical circuit constitution, that is, the current flows only the time when the transistors are switching.

Therefore, the low power consumption and very large scale three valued integrated circuit can be feasible and be applicable conventional CMOS fabrication process.

4 Procedure to realize Three Valued Memory System

The three valued logic memory system will be realized in the following procedure.

1)Implement three valued inverter circuit (NOT circuit).

2)Next, compose a three valued latch circuit using three valued inverter circuit

above mentioned.

3)After that, compose a three valued SRAM memory cell using the three valued latch circuit obtained in the previous step.

4)Finally, construct a three valued SRAM memory system arranging the tree valued SRAM memory cells.

5 Three Valued Logic Circuit

A three valued inverter circuit (NOT circuit) is a typical the single input variable three valued logic circuit. The implementation method is given by Olson Edgar Danny. (This method is called Olson Method.)

The author also uses this method.

A three valued latch circuit is composed in the manner of the conventional master slave constitution that acts with operational stability.

A master slave latch is composed with two half latchs. A half latch is constituted with a loop circuit combined with two three valued inverter circuit and a transfer gate.

6 Three Valued Logic Memory System

There is little modification between the three valued logic SRAM memory cell constitution and the two valued constitution.

A three valued SRAM cell consists of a loop of two three value inverter circuit (NOT circuit) and one or two pass transistors. However, the pass transistors of three valued SRAM cell are different from two valued constitution. We must use back to back connected p and n channel MOS transistors as a three valued transfer date.

Design of three valued SRAM memory system is completed with laying out SRAM cells as an array and appending an address decoder.

7 Experiment Result

The operation of the three valued logic circuits are confirmed by SPICE simulation. Gate length of MOS transistors is 90nm. The author has confirmed finally operation capabilities of three valued SRAM memory cell adjusting threshold voltage of MOS transistors.

It is confirmed that the SRAM memory cell is able to be periodically written in 10n second and to hold data stable.

8 Conclusion

Some positive results have been achieved for practical use of the three valued logic circuit and the three valued logic memory, although some problems have been left. Reduction of leak current in stable states and acceleration of operating speed should be investigated.

The author has also realized the systematic flow of design for the three value logical circuit through constitution of the three valued memory system.

He also has obtained perspective of design automation for three valued LSIs and is convinced with reality of practical use of three valued logic.