Research of logic synthesis algorithm suitable for wave pipeline processor

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1 Introduction

Recent years, the microprocessor architecture is shifting from the single core configuration to the multiple core configuration. Processing speed improvement of single core processors is not allow, because operating clock frequency is proportional to maximum delay of processor's pipeline stages, and shortening a clock cycle time by dividing a pipeline stage faces to limit.

Meanwhile, there is an operating principle called the wave pipeline that it operates within the clock cycle time of the difference between maximum delay time and minimum delay time of a pipeline stage.

Operating frequency limitation of single core processor is expected to be overcome by this operating principle. There are, however, problems of design difficulties, because no suitable CAD system for the wave pipeline processor design exists currently.

Most important issue of the wave pipeline operation is to achieve cut-down of delay difference time between maximum delay time and minimum delay time. In this paper, the author suggests a new logic synthesis algorithm to coordinate number of logic stages of and to align the delay time of a logic circuit form input nodes to output nodes.

And the author develops the prototype CAD system that the proposed logic synthesis algorithm is embedded and shows the validity and effectiveness of the system.

2 Wave pipelining

The pipelining is a mode of processing that is moved two or more instructions little by little, temporally-overlaps, and executed concurrently. The pipeline processing becomes the general technology in the processor currently. A conventional pipeline is processed synchronizing with the clock. Therefore, The maximum delay will decide the operation clock frequency in a conventional pipeline.

In the wave pipeline, the operation clock frequency is decided by the differential delay. Thus, if the differential delays are smaller than maximums, the wave pipeline operation can set the operation clock frequency high. At the same time, CAD to which a usual pipeline is required is unsuitable for the design of the wave pipeline where the differential delay should be considered, because only the maximum delay is considered. Consequently, development of the special CAD is essential to apply a wave pipeline.

3 A theory of the MOSFET and delay characteristic of the CMOS

The current microprocessor makes ends meet by CMOS technology. CMOS is a device of the complementary type composed by PMOS and NMOS. The MOS transistor is a kind of field-effect transistor (FET). It is a semiconductor element that tries to change the electric conductivity of the current passage in static electricity by the third electrode, and to control the current. A basic principle of operation of the MOS transistor, it is in the control of the amount of the negative electric charge that flows in the channel between the source and drains by the action of the charge on the gate electrode and the flow. PMOS is a transistor that operates the hole as a career, and NMOS is a transistor that operates the electron as a career. Therefore, PMOS enters the state of the cutoff when the gate

voltage is high, and enters the state of conduction state is low. NMOS does working opposite to PMOS because the electron is a career. As for PMOS and NMOS, the mibility of the career is also different, because the career is different. For that reason, in PMOS and NMOS, ON resistance is different. But, PMOS can be matched to on resistance of NMOS by adjusting length L of the gate, width W of the gate, and thickness D of the oxide film .

4 Existing algorithm of cut down the differential delay

The technique of bringing a minimum delay close to the maximum delay is used by the algorithm that inserts the delay buffer designed by Ikeda as the technique for achieving the delay difference cut down the past. Operating by making to the wave by the frequency four times the operation clock frequency of a usual pipeline becomes possible in this technique. but the area of the circuit increases by about 2.8 times, and the performance improvement doesn't correspond to the cost of an area increase.

5 Logical synthesis method for delay difference cut-down

The logical, synthetic algorithm proposes by this research is processed by the following procedures. First of all, the logical expression is optimized by the Quine-McCluskey algorithm. Next, the circuit is converted into the NAND expression, and logic is made a multistage by the input limitation of the logic element. Finally, The number of logical circuits of logical stage at the end to each output adjust the circuit which is multistage most .

6 Mounting proposal technique and the evaluation

It explains the method of mounting the proposal technique and evaluates it according to the cell model for the evaluation. An ideal cell model to whom the maximum delay and a minimum delay of the logic element were almost

equal and the cell models by whom the differential delay in a realistic logic element was assumed were designed. For an ideal cell model, it was shown that the proposal technique had acted effectively. In the evaluation by a realistic cell model, it became a result that the improvement of about three times the operation clock frequency was able to be expected by making to the wave by replacing a tedious logic element with the best element. An area increase of the logical circuit showed suppression to about 1.7 times increased by optimizing the logic element.

7 Conclusion

It was a result that the improvement of three times of the operation clock frequency, and the increase of 1.7 times of the area was able to be expected for the multistage logic in the evaluation of the proposal technique. An increase in the area of the circuit was suppressed from a past technique by arranging the number of logical stage. From this conclusion, A logical, synthetic algorithm to which the number of logical stage is arranged can say that it can suppress an increase in the logic area, and can equalize the differential delay. Consequently, It is thought that the proposal technique is useful.

As future tasks, The selection of the best logic element to compose the logical circuit is included. And from the result of this research, It was shown to cause the limit by the delay of the logic element in cut-down the differential delay even if the number of logical stage was arranged. From here onwards, It is very important to suppress the differential delay in the logic element to the minimum. It is thought that the differential delay can be shortened further by the proposal technique considering the above.