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Description	

Potential barriers to electron carriers in C_{60} field-effect transistors

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Transport properties of C_{60} field-effect transistors (FETs) have been investigated in the temperature range between 160 and 300 K. Activation energy was estimated from temperature dependence of resistance at the linear region and of current at the saturation region for various channel lengths. Variation of activation energy values is attributed to carrier injection barrier at contact between source electrode and C_{60} channel, and barriers to carrier hopping between trap states in the channel of C_{60}. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2917469]

Organic field-effect transistors (OFETs) have great potential for next-generation electronic devices because of their inexpensive price, light weight, mechanical flexibility, and high shock resistance.[1] Performance of both *n*-type and *p*-type OFETs has been dramatically improved, and field-effect mobility μ_{FE} has become comparable to that of amorphous Si (*a*-Si) over the past decade.[2–5] Characterization, namely, estimation of device parameters for OFETs, has been performed in the same way as for Si metal-oxide-semiconductor (MOS) FETs so far, because of similarity of device characteristics of OFETs and Si-MOS FETs. This characterization is very convenient for the comparison of their performance from the viewpoint of device application. Understanding the detailed transport mechanism of OFETs is expected to greatly improve device performance.

From the systematic and detailed characterization of OFETs,[6–12] it has been clarified that the device performance of both *n*-type and *p*-type OFETs strongly depends on parasitic resistance at the interface between the (source/drain) electrodes (inorganic metal) and the channel (organic semiconductor). The effect of parasitic resistance is significant for the low gate voltage V_G region.[6,11] A main cause of the parasitic resistance is thought to be the Schottky barrier at the interface between electrodes and the channel. We proposed a semiquantitative model for operation of OFETs, where double Schottky barriers govern the device characteristics in the low drain-source voltage V_{DS} region.[13,14] However, in the saturation region, device characteristics strongly depend on properties of trap states in the channel region. Actually, density of states of charge carrier traps can be estimated from the temperature dependence of saturation current I_D^{sat}.[15,16] In linear and saturation regions, transport properties are strongly affected by Schottky barriers and/or potential barriers between traps.

In this letter, we have investigated temperature dependence of C_{60} FET device characteristics for various V_G and channel lengths L. Estimated values of potential barrier heights are discussed in terms of carrier injection at the contact between source electrode and C_{60} channel and carrier hopping between trap states in the channel of C_{60}.

C_{60} FETs were fabricated with a bottom contact configuration, as shown in Fig. 1(a). A heavily doped *n*-type silicon wafer with a 400 nm thick layer of thermally oxidized SiO_2 was used as substrate. The source and drain electrodes were patterned on insulating SiO_2 layer, using a photolithography method. In order to estimate contributions of the resistance at source electrode (R_S), drain electrode (R_D), and channel (R_{ch}) to the total resistance (R_t), a series of FETs with various channel lengths L, from 2.5 to 25 μm, and fixed channel width W of 500 μm, was fabricated. The adhesion layer of Ti

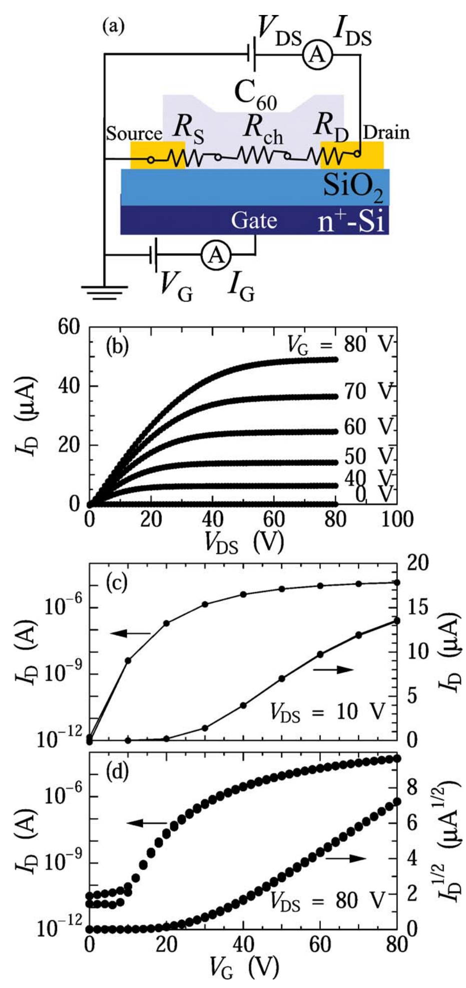

FIG. 1. (Color online) (a) Device structure of C_{60} thin-film FET. (b) Output characteristics, (c) transfer characteristics at V_{DS}=10 V (linear region), and (d) transfer characteristics at V_{DS}=80 V (saturation region), for C_{60} FET with L=25 μm at 300 K.

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TABLE I. Size and device parameters of all devices. Values at upper and lower lines were estimated from linear and saturation regions, respectively, with formulas in the text.

L (μm)	2.5[a]	5	10	15	20	25
μ_{FE} (cm^2/V s)	0.10	0.10	0.12	0.10	0.14	0.13
	⋯	0.26	0.20	0.20	0.20	0.20
V_T (V)	32.4	32.4	33.7	33.0	33.0	24.4
	⋯	32.9	32.8	30.9	30.6	28.8
On-off ratio	1.6×10^6	2.3×10^7	4.4×10^7	2.9×10^7	2.9×10^7	9.7×10^6
	3.3×10^6	1.0×10^7	2.6×10^7	8.4×10^7	2.5×10^7	5.3×10^7
S (V/decade)	5.5	5.6	4.4	3.8	3.8	5.9
	5.2	3.9	2.7	4.2	4.0	3.7

[a]No saturation characteristics were observed for the device with $L=2.5$ μm. The μ_{FE} and V_T were not estimated for saturation regime, and on-off ratio and S were estimated from data measured at $V_G=80$ V.

(thickness of 5 nm), and the Au source and drain electrodes (thickness of 95 nm) were deposited using electron-beam deposition at a deposition rate of about 0.1 nm/s. The doped silicon layer of the wafer was used as a gate electrode. Commercially available C_{60} (99.98%) was used for the formation of the thin-film channel layer. A C_{60} thin film of 150 nm thickness was formed using vacuum ($<10^{-5}$ Pa) vapor deposition at the deposition rate of 0.01 nm/s. The FETs fabricated by this procedure were exposed to air during the transfer from the deposition chamber to a measurement chamber. Therefore, before measurements, the samples were annealed at 120 °C under 10^{-3} Pa for 24 h in order to eliminate O_2 and/or H_2O molecules adsorbed in the C_{60} thin films. Transport properties of C_{60} FETs were measured under 10^{-3} Pa, using cryogenic prober system (Desert TT-prober, Keithley 4200-SCS). Output characteristics (drain current I_D versus V_{DS}) and transfer characteristics (I_D versus V_G) were measured. Low temperature measurements were performed by flowing liquid nitrogen into the cryogenic prober.

Figure 1(b) shows output characteristics of a device with $L=25$ μm at 300 K. I_D almost linearly increases with increasing V_{DS}, followed by saturation due to the pinch off of the accumulation layer. Hysteresis of I_D with V_{DS} sweep was very small. Transfer characteristics at linear region ($V_{DS}=10$ V) and saturation region ($V_{DS}=80$ V) at 300 K are shown in Figs. 1(c) and 1(d), respectively. The μ_{FE} and threshold voltage V_T were determined from the relations, $I_D=(\mu_{FE}WC_0/L)(V_G-V_T)V_{DS}$, at linear regime and $I_D^{sat}=(\mu_{FE}WC_0/2L)(V_G-V_T)^2$, at saturation regime, respectively. Here, we use 1.0×10^{-8} F/cm^2 as the capacitance per area of gate insulator SiO_2 (C_0), estimated from dielectric constant and thickness of SiO_2. The μ_{FE}, V_T, current on-off ratios, $I_D(V_G=80\ \text{V})/I_D(V_G=0\ \text{V})$, and subthreshold swing S are summarized in Table I. All devices qualitatively show the same characteristics, and their device parameters are close to those of the best ones fabricated by conventional methods,[4] except for the device with $L=2.5$ μm. Saturation behavior in output characteristics was not observed for the device with $L=2.5$ μm because of the short channel effect. Now, we will mainly discuss data obtained from devices with $L=5$–25 μm.

Temperature dependences of resistance at linear region ($V_{DS}=10$ V) and $1/I_D^{sat}$ ($V_{DS}=80$ V) for the various V_G are depicted with Arrhenius plots in Figs. 2(a) and 2(b), respectively. Here, resistance was estimated from the steepest slope at the linear region in I_D versus V_{DS} plots.[11,12] In both cases, the temperature dependence is activation type. V_G dependence of E_a for devices with $L=5$ and 25 μm is plotted in Fig. 3(a). E_a values were estimated from R versus T plots [Fig. 2(a)] for linear region and $1/I_D^{sat}$ versus T plots [Fig. 2(b)] for saturation region. An exponential-like decrease of E_a with increasing V_G was observed for all cases, as reported in Refs. 15 and 16. Here, it should be noted that three features are found in V_G dependence of E_a [Fig. 3(a)]. First, the E_a shows larger value for device with larger L, which can be confirmed by the L dependence of E_a, as shown in Fig. 3(b). Second, for the device with $L=5$ μm, the E_a values are different in the linear and saturation regions [Fig. 3(a)]. Third, for the device with $L=25$ μm, the E_a for linear and saturation regions at the same V_G show almost the same value [Fig. 3(a)].

L dependence of E_a originates from different contributions of R_S, R_D and R_{ch} to $R_t(T)[=R_S(T)+R_{ch}(T)+R_D(T)]$. For $L\rightarrow0$, the E_a corresponds only to potential barriers at the contacts, i.e., $R_t(T)=R_S(T)+R_D(T)$. Taking into account the double Schottky barrier model,[13,14] the main contribution at the contact is R_S, namely, $R_t(T)\approx R_S(T)$, because the reverse bias operation at the drain electrode is the dominant source of resistance. Here, it should be noticed that $R_S(T)$ does not directly affect I_D at the saturation region, because of pinch-off regime. However, voltage drop at source electrode,

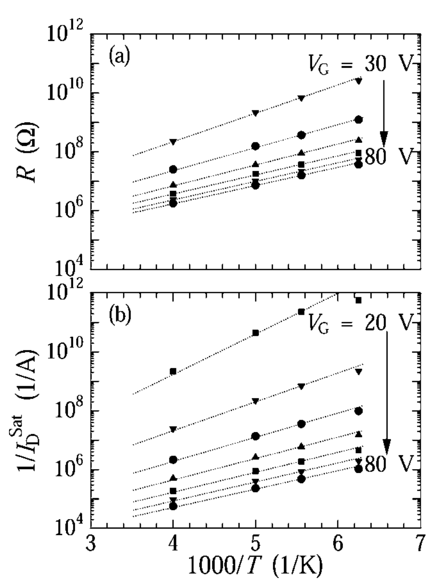

FIG. 2. Arrhenius plots of (a) resistance at linear region, and (b) $1/I_D^{sat}$ at saturation region for C_{60} FET with $L=25$ μm, for various V_G in 10 V steps.

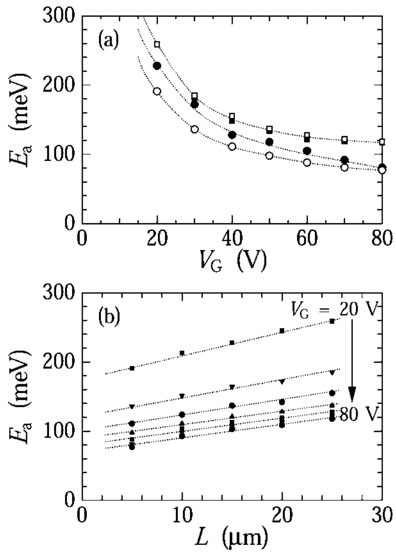

FIG. 3. (a) E_a vs V_G plots at V_{DS}=10 V (closed marks) and 80 V (open marks) for devices with L=5 μm (circle) and 25 μm (square). (b) L dependence of E_a estimated from saturation region for various V_G in 10 V steps. Lines are guides for the eye.

$V_S = R_S I_D$, can reduce the effective gate voltage from V_G to $V_G - V_S$, resulting in the reduction of I_D even at the saturation region. Consequently, for smaller L, the E_a is mainly governed by R_S (carrier injection barrier) for whole V_{DS} region. On the other hand, for $L \rightarrow \infty$, the E_a corresponds only to potential barriers at the channel region, i.e., $R_t(T) \approx R_{ch}(T)$.

First, we discuss the E_a values for the device with L=5 μm, which are mostly consist of R_S. The E_a values (230–80 meV) for the device with L=5 μm are smaller than those (260–110 meV) for the device with L=25 μm [Fig. 3(a)], showing that the carrier injection barrier height is smaller than potential barriers between trap sites in the channel of C_{60} thin film. In addition, the E_a values are smaller than those expected from Mott–Schottky relation. This suggests that a thermionic emission through Schottky barrier lowered by interface states dominates transport at the contact. Furthermore, different E_a values in the linear and saturation regions originate from the mirror-charge effect on Schottky barrier, namely, barrier height decreases with increasing V_{DS} due to the mirror-charge effect.[13] Thus, V_{DS} dependence of E_a is a specific phenomenon originating from the Schottky barrier.

Finally, we discuss the E_a values for the device with L=25 μm. They should be hardly affected by R_S, because of large L, as is supported by the fact that E_a for linear and saturation regions at the same V_G show almost the same value, i.e., the E_a is independent of V_{DS}. Indeed, the E_a values are consistent with the density of states of charge carrier traps at the channel.[16] Consequently, it is concluded that E_a values of 260–110 meV for the device with L=25 μm directly reflect the barrier heights to carrier hopping between trap states in the channel of C_{60}. The reduction of E_a by application of V_G can be explained by filling the trap states of C_{60} thin film.[16]

In conclusion, we estimated three different series of E_a in C_{60} FET from temperature dependence of device characteristics for various V_G and channel lengths L. Small E_a values of 230–80 meV were ascribed to carrier injection barrier at contact between source electrode and C_{60} channel. Here, it has been found that barrier at the source contact is slightly reduced by application of V_{DS}, due to the mirror-charge effect. The barrier height to carrier hopping between trap states in the channel of C_{60} thin film has been found to vary from 260 to 110 meV depending on V_G. The relative relationship and approximate values for potential barrier heights have been clarified, although E_a values at the contact and channel could not be completely separated in this study. This information can contribute to understanding the detailed transport mechanism of OFETs.

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