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Description	

Fabrication of ambipolar field-effect transistor device with heterostructure of C₆₀ and pentacene

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Ambipolar field-effect transistor (FET) device was fabricated with heterostructure of thin films of C₆₀ and pentacene. Three types of device structures in the C₆₀/pentacene heterostructure FET device were studied in order to realize the best ambipolar properties. In the middle-contact type FET device of C₆₀ and pentacene, the mobility μ in *p*-channel operation was estimated to be $6.8 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, while the μ in *n*-channel operation was $1.3 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This ambipolar FET device is available for a practical building-block to form CMOS integrated circuits with low-power consumption, good-noise margins, and ease of design. © 2004 American Institute of Physics. [DOI: 10.1063/1.1818336]

Field-effect transistor (FET) devices with thin films of organic molecules have attracted special attention from viewpoints of structural flexibility, low-temperature/low-cost processing, and large-area coverage.^{1,2} Most of organic thin-film FETs show either *n*- or *p*-channel characteristics, i.e., unipolar properties. The C₆₀ thin-film FET showed *n*-channel enhancement-type properties with the highest mobility, μ , of $0.1\text{--}0.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ among *n*-channel FETs with organic thin films.³⁻⁵ On the other hand, the FET with thin films of pentacene showed *p*-channel enhancement-type properties with the highest μ value ($\sim 1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) among all known FETs with organic thin films.⁶

CMOS integrated circuits have extensively been used to develop various types of chips such as memories and micro-processors because of low-power consumption, good-noise margins, and ease of design.⁷ Some CMOS integrated circuits have been fabricated with multiple organic unipolar devices.^{5,8-11} On the other hand, the use of ambipolar FET devices, which shows both *n*- and *p*-channel properties, can lead to simplification in design of CMOS integrated circuits. Very recently, the CMOS inverter circuits were fabricated with ambipolar FET devices of [6,6]-phenyl C₆₁-butyric acid methyl ester (PCBM) /poly[2-methoxy-5-(3',7'-dimethyloctyloxy)]-*p*-phenylene vinylene (OC₁C₁₀-PPV) blend structure, and poly(3,9-di-*t*-butylindeno[1,2-b]fluorene) (PIF);¹² the PIF functioned as *n*- and *p*-channel FETs by itself. The ambipolar FET devices were also fabricated with heterostructure of C₆₀ and α -hexathienylene (α -6T), and heterostructure of 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA) and α,ω dihexyl hexathienylene (H6T).^{13,14} Further the FET device with titanylphthalocyanine showed ambipolar properties by changing the nature of the active layer.¹⁵ However, the μ 's of these ambipolar devices were quite low ($10^{-6}\text{--}10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)¹²⁻¹⁵ though the C₆₀/ α -6T FET de-

vice showed relatively high μ of $\sim 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

In the present study we have fabricated high-performance ambipolar FET devices with heterostructure of thin films of C₆₀ and pentacene. C₆₀ and pentacene are expected to be promising materials for the high-performance ambipolar FET devices, since the individual devices with C₆₀ and pentacene showed the highest μ value among *n*- and *p*-channel organic FETs, respectively.³⁻⁶ Three types of device structures were investigated in order to realize high-performance ambipolar FET properties.

The device structures fabricated in the present study are schematically shown in Fig. 1. Commercially available C₆₀ (99.98%) and pentacene (99.9%) were used for the fabrication of thin films as active layers. The commercially available SiO₂/Si(100) wafer was used as a substrate after clean-

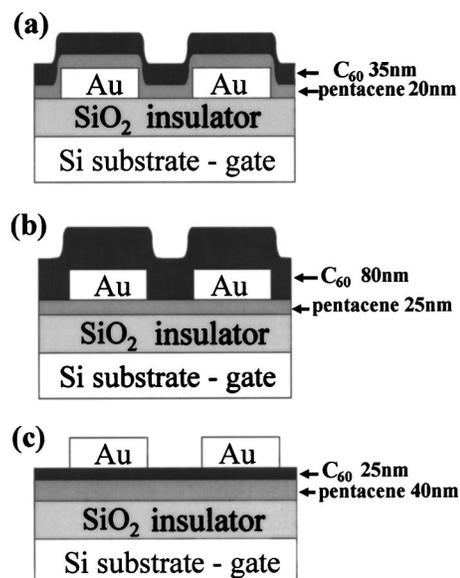


FIG. 1. Device structures of C₆₀/pentacene thin-film FET. (a) Bottom-contact type, (b) middle-contact type and (c) top-contact type devices.

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ing and hydrophobic treatments of the surface reported elsewhere.⁵ The thin films of pentacene and the C₆₀ were formed by a thermal deposition under 10⁻⁸ Torr. Thickness of SiO₂ layers was 420 nm. Gold electrodes of 50 nm thickness were attached on different places in three types of devices (Fig. 1). The thicknesses of C₆₀ and pentacene are shown in Fig. 1. The channel length, *L*, and the channel width, *W*, of these devices were 20–30 and 2000–6000 μm, respectively. The characteristics of these FET devices were measured under vacuum of 10⁻⁶ Torr.

The plots of the drain current *I_D* versus the source-drain voltage *V_{DS}* of the C₆₀/pentacene FET device fabricated in bottom-contact type [Fig. 1(a)] showed only *p*-channel FET properties before annealing the device. This result implies that pentacene operates as an active layer. On the other hand, this device showed only *n*-channel FET properties, after annealing at 120°C for 24 h under vacuum of 10⁻⁶ Torr. This implies that C₆₀ operates as *n*-channel active layer by removing impurity gases from the C₆₀ thin film. Thus no ambipolar FET properties could be observed in the bottom-contact device [Fig. 1(a)]. The disappearance of the *p*-channel operation after annealing remains to be clarified. Here it should be noted that the pentacene layer remains to be sublimed even at 120°C because the layer is covered with C₆₀. Therefore we cannot assign the disappearance of *p*-channel performance to that of the pentacene layer. The *I_D* of the pentacene FET in the bottom-contact device before annealing was lower by three orders of magnitude than that [see Fig. 2(a)] in the middle-contact device, i.e., the top contact for the pentacene layer, implying that the *p*-channel FET performance is poor in the bottom-contact configuration. Therefore, the disappearance of the *p*-channel FET performance when the C₆₀ FET operates after annealing may be associated with such an unstable *p*-channel performance. However, a clear explanation for the disappearance of the *p*-channel performance cannot be shown at the present stage.

The C₆₀/pentacene FET device fabricated in the middle-contact structure [Fig. 1(b)] showed only *p*-channel properties before annealing the device under vacuum, while both FET properties of *n* and *p* channels were observed after annealing at 80°C for 24 h under 10⁻⁶ Torr. The *I_D*–*V_{DS}* plots measured in the *p*-channel mode showed typical *p*-channel FET properties, while those in the *n*-channel mode showed unusual FET properties, as described later. The magnitude of *I_D* in the *n*-channel mode was smaller by two orders of magnitude than that in the *p*-channel mode. Here the increase in the annealing time at 80°C could not lead to a significant enhancement of the *I_D* in the *n*-channel mode. On the other hand, the raising of the annealing temperature at 10°C step from 80 to 120°C resulted in a linear increase in the *I_D* where the annealing time was 24 h at all the annealing temperatures. Finally, annealing the device at 120°C increased the *I_D* in the *n*-channel mode by one order of magnitude in comparison with the case of annealing at 80°C for 24 h. The raising of the annealing temperature did not lead to the lowering of the *p*-channel conduction.

As shown in Fig. 2, the *I_D*–*V_{DS}* plots of the C₆₀/pentacene device with middle-contact structure [Fig. 1(b)] showed clear ambipolar FET properties after annealing the device at 120°C. The plots in the *p*-channel mode showed typical *p*-channel FET properties [Fig. 2(a)]. In the *n*-channel mode the *I_D* increased supralinearly with increasing *V_{DS}* at low values of *V_G* [Fig. 2(b)]. The magnitude of *I_D*

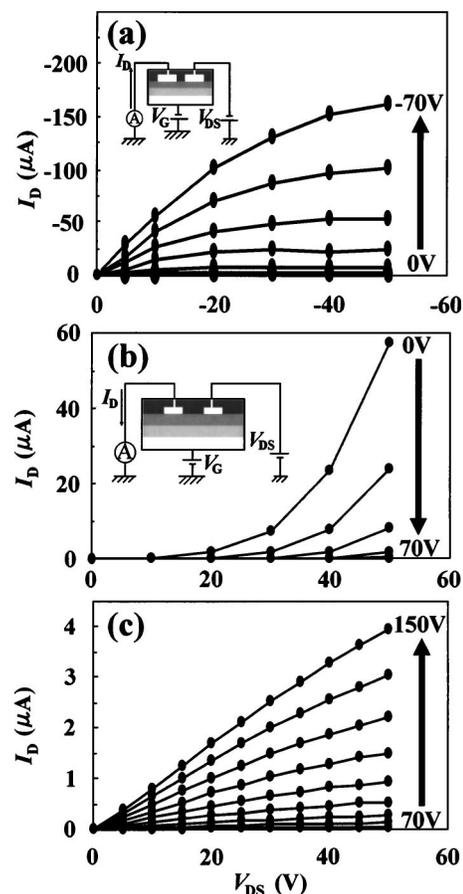


FIG. 2. *I_D*–*V_{DS}* plots of C₆₀/pentacene FET with middle-contact device structure at 295 K. This device was annealed at 120°C for 24 h before the measurement of FET properties. *I_D*–*V_{DS}* plots in (a) *p*-channel mode, (b) *n*-channel mode from *V_G*=0 to 70 V, and (c) *n*-channel mode from *V_G*=70 to 150 V. Closed circles refer to the points measured. Variation of *V_G* applied to devices is shown by arrows. Measurement circuits in *p*- and *n*-channel modes are shown in (a) and (b), respectively.

decreased when increasing *V_G*, and reached the minimum value around *V_G*=60 V. Further increase in *V_G* could lead to the enhancement of *I_D*, and the *I_D*–*V_{DS}* plots showed normal *n*-channel properties [Fig. 2(c)]. Here it should be noted that the electric field at *V_{DS}*=50 V and *V_G*=0 V in *n*-channel circuit is the same as that at *V_{DS}*=–50 V and *V_G*=–50 V in the *p*-channel circuit, and that the parallel shift of –50 V in *V_G* occurs between the *n*- and *p*-channel circuits. The holes are still induced into the thin film of pentacene at *V_{DS}*=50 V and *V_G*=0 V (*n*-channel circuit). Therefore, the decrease in the *I_D* observed in the *n*-channel mode when increasing *V_G* from 0 to 60 V implies that the hole conduction is depleted in the thin film of pentacene. The electron conduction in the thin film of C₆₀ is not observed below 60 V. After complete depletion of hole conduction, the electron conduction was observed with an increase in *V_G*, as shown in Fig. 2(c).

The μ and the threshold voltage *V_T* in the *p*-channel operation for this C₆₀/pentacene device after the annealing at 120°C was estimated to be $6.8 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and –15 V, respectively. The μ value is larger by one to two orders of magnitude than those of the *p*-channel operation in the C₆₀/α-6T heterostructure ($\mu=4 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and PCBM/OC₁C₁₀-PPV blend ($\mu=7 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) FET devices,^{12–14} while $|V_T|$ is somewhat larger than that, ~0 V, in the *p*-channel mode of the C₆₀/α-6T FET device. The μ

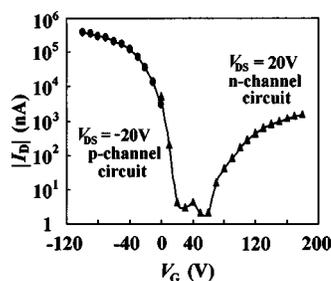


FIG. 3. $|I_D|$ - V_G plot at $|V_{DS}|=20$ V for C_{60} /pentacene FET with middle-contact device structure at 295 K. This device was annealed at 120°C for 24 h before the measurement of FET properties. Closed circles and closed triangles refer to the points measured in p - and n -channel circuits, respectively.

and V_T of the n -channel operation in the C_{60} /pentacene device were estimated to be $1.3 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 98 V, respectively. This μ value is larger by two orders of magnitude than that, $3 \times 10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, in the PCBM/ OC_1C_{10} -PPV blend FET devices,¹² while the μ value is somewhat smaller than, $5 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, in the n -channel operation of the C_{60}/α -6T FET.^{13,14} To sum up, the ambipolar device with C_{60} /pentacene heterostructure showed the highest μ in p -channel operation among ambipolar devices with thin films of organic materials and the μ value comparable to the maximum value ($\mu=5 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in C_{60}/α -6T FET) in n -channel operation.

The plots of $|I_D|$ versus V_G for the C_{60} /pentacene FET are shown in Fig. 3. The maximum on-off ratios in p - and n -channel operations of the C_{60} /pentacene FET device after the annealing at 120°C were estimated to be 1.3×10^5 and 7.6×10^2 from the $|I_D|$ versus V_G plot (Fig. 3). It has been found that the C_{60} /pentacene heterostructure FET device with middle-contact structure shows very good ambipolar FET properties. The middle-contact device structure corresponds to the top-contact and bottom-contact structures for pentacene and C_{60} , respectively. The top-contact FET device of pentacene shows higher FET properties than those of the bottom-contact pentacene FET because of the difference in morphology of crystals in the thin films,¹⁶ while such a tendency has not been reported so far for C_{60} FET. These facts may lead to the high ambipolar FET properties in the middle-contact device, i.e., the best p -channel properties for pentacene as active layer among ambipolar devices and the good n -channel properties for C_{60} as active layer.

It is expected that this ambipolar FET device is available for a practical building-block to form CMOS integrated circuits with low-power consumption, good-noise margins, and ease of design. Further this FET device was annealed up to 130°C to examine the annealing effect on the FET properties. However, the μ values in both p - and n -channel operations decreased slightly in comparison with those measured after the annealing at 120°C . Finally the C_{60} /pentacene FET with top-contact device structure shown in Fig. 1(c) was fabricated. However, neither n - nor p -channel properties were observed in this device. These results show that the middle-contact structure is the best device structure for the ambipolar FET properties in the C_{60} /pentacene heterostructure FET devices.

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