Output properties of C_{60} field-effect transistor device with Eu source/drain electrodes

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Field-effect transistor (FET) device with thin films of C_{60} has been fabricated with Eu electrodes exhibiting small work function. The C_{60} FET device shows *n*-channel FET properties with high field-effect mobility, 0.50 $cm^2\ V^{-1}\ s^{-1}$. Furthermore, nonvanishing drain current, i.e., normally on, is observed in this FET device. This originates from small energy barrier for electron from Eu source electrode to lowest unoccupied molecular orbital of C_{60}. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2337990]

Field-effect transistor (FET) devices with thin films of organic molecules have attracted special attention because of structural flexibility, low-temperature/low-cost processing, and large-area coverage.[1,2] The highest field-effect mobility μ value is 1.5 $cm^2\ V^{-1}\ s^{-1}$ for the pentacene thin-film FET among FETs with organic thin films, and this device showed *p*-channel normally off properties.[3] On the other hand, the C_{60} and *N*,*N*′-dialkyl-3,4,9,10-perylene tetracalboxylic diimide derivative thin-film FET devices showed *n*-channel normally off FET properties with the high μ values of 0.56–0.65 and 0.6 $cm^2\ V^{-1}\ s^{-1}$, respectively.[4–6]

Very high μ values of 1–20 $cm^2\ V^{-1}\ s^{-1}$ were reported for the FET devices with single crystals of rubrene and pentacene.[7–10] Furthermore, *p*-channel, *n*-channel, and ambipolar FET devices with single crystals of rubrene and dibenzothiatetrathiafulvalene-tetracyanoquinodimethane were successfully fabricated by tuning the Fermi level of electrodes.[11,12] Thus, recent progress of organic single crystal FETs is dramatic and rapid. Nevertheless, it is indispensable to develop the thin-film FETs exhibiting excellent performance for practical applications of organic FETs. Especially, *n*-channel FET devices exhibiting high μ values are required for design of complementary metal oxide semiconductor logic gate circuits because of the worse output properties for *n*-channel thin-film FETs than those for *p*-channel FETs.

Recently, *n*-channel FET properties in the pentacene thin-film FET device were observed by using Ca metal for source/drain electrodes in the device; the μ value was quite low (2.7×10^{-5} $cm^2\ V^{-1}\ s^{-1}$).[13] No energy barrier for electron exists from Ca electrodes (Fermi energy[14] $E_F=-\phi=-2.87$ eV) to the lowest unoccupied molecular orbital (LUMO) of pentacene (energy level of LUMO, $E_{LUMO}=-3.2$ eV).[13] This is probably the origin for the *n*-channel operation of the pentacene FET. Furthermore, the *p*-channel operation was realized in the C_{60} thin-film FET by modifying Au electrodes with self-assembly monolayers.[15] These results show that the FET operation in the thin-film FET devices can also be controlled by using metal electrodes with various ϕ, as in the single crystals FET.[11,12] In this letter, we have studied the output properties of C_{60} thin-film FET devices fabricated with metal electrodes exhibiting the ϕ value of 2.5–5.65 eV. The C_{60} FET device with Eu source/drain electrodes[14] ($\phi=2.5$ eV) showed the μ value of 0.50 $cm^2\ V^{-1}\ s^{-1}$.

The C_{60} molecule and the top-contact-type device structure are shown in Fig. 1(a); this device structure is adopted for Eu, while the bottom-contact-type device structure (not shown) is adopted for Cu and Pt. Commercially available C_{60} (99.98%) and SiO_2/Si(100) wafer were used for the formation of the active layers (thickness of 70–150 nm) and for a substrate, respectively. The SiO_2 surface was treated with hexamethyldisilazane. During thermal deposition of C_{60} under 10^{-8} Torr, the temperature of the substrate was maintained at room temperature. Thickness of SiO_2 layers was 400 nm, and the capacitance per unit area, C_0, was determined by *LCR* meter to be 7.3×10^{-9}–8.2×10^{-9} F cm^{-2}. The metal electrodes of 30–50 nm thickness were attached as source/drain electrodes. The channel length *L* and the

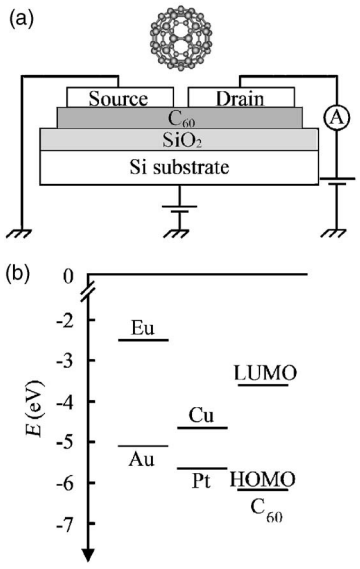

FIG. 1. (a) Molecular structure of C_{60} and device structure of C_{60} thin-film FET. (b) Energy diagram of metals and LUMO and HOMO of C_{60}.

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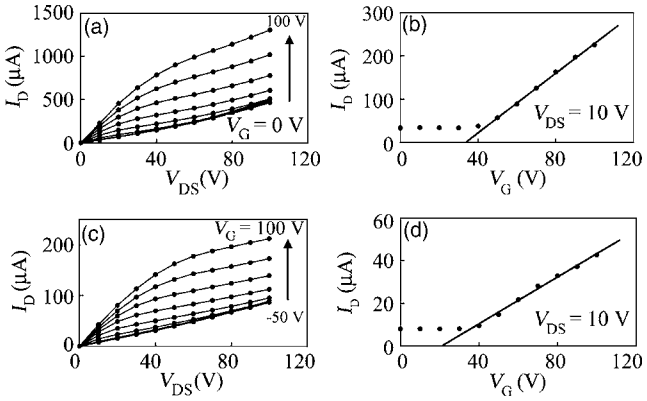

FIG. 2. (a) I_D-V_{DS} plots and (b) I_D-V_G plot for C_{60} FET device with Eu electrodes measured at 294 K just after annealing the device. (c) I_D-V_{DS} plots and (d) I_D-V_G plot for C_{60} FET devices with Eu electrodes measured at 294 K after keeping the device at 294 K for 12 h.

channel width W of these devices were 50 and 4800 μm for Eu, respectively, and 30 and 2700 μm for Cu and Pt. The characteristics of the FET devices were measured in n-channel measurement mode [Fig. 1(a)] under vacuum of 10^{-7} Torr (Eu) or 10^{-6} Torr (Cu and Pt).

The plots of the drain current I_D versus the drain-source voltage V_{DS} in the C_{60} FET device with Eu source/drain electrodes show n-channel normally on properties [Fig. 2(a)]; the C_{60} FET with Au source/drain electrodes showed n-channel normally off properties.[4,16–18] The E_F for metals and the energy levels for LUMO and highest occupied molecular orbital (HOMO) (E_{LUMO} and E_{HOMO}) are shown in Fig. 1(b); the E_F values of metals, E_{LUMO}, and E_{HOMO} are taken from Refs. 8, 19, and 20. As the E_F of Eu is higher than E_{LUMO}, no energy barrier, i.e., Ohmic contact, for electron can be expected between Eu electrode and LUMO. Actually, the interface dipole is known to be induced between metal electrodes and organic layers.[21] In this case, the dipole shifts the vacuum level by the shift value Δ. The Δ value for Eu may be positive since the Δ generally goes towards positive from negative with decreasing ϕ. The positive Δ may break Ohmic contact between the Eu electrodes and C_{60} thin films because the E_F of Eu metal lowers by the Δ. However, as the maximum Δ is at most $\sim$1 eV, the E_F of Eu will become $\sim$−3.5 eV (=−2.5−Δ) even if Δ=1 eV. Namely, the energy barrier between the Eu and C_{60} should be small even if the Schottky barrier is formed between Eu and LUMO level (E_{LUMO}=−3.6 eV) of C_{60}. Consequently, nonvanishing I_D observed at gate voltage V_G of 0 V may be explained by no or small Schottky barrier when the C_{60} thin films contact to the Eu electrode.[22]

The μ and threshold voltage V_T were determined to be 0.50 $cm^2\ V^{-1}\ s^{-1}$ and 34 V, respectively, from the I_D-V_G plot [Fig. 2(b)] at V_{DS}=10 V (linear region). The μ value is comparable to that, 0.56–0.65 $cm^2\ V^{-1}\ s^{-1}$, reported previously for the C_{60} FET device with Au electrodes.[4,6] The μ value of 0.56 $cm^2\ V^{-1}\ s^{-1}$ was observed for the FET device tested under 10^{-9} Torr without exposure to air after formation of C_{60} thin films,[4] while the μ of 0.65 $cm^2\ V^{-1}\ s^{-1}$ was observed for the device tested under N_2 atmosphere (O_2, H_2O<0.1 ppm) without exposure to air.[6] The FET device with Eu electrodes fabricated in this study was exposed to air after formation of thin films of C_{60} and annealed at 363 K for 4 h under vacuum of 10^{-7} Torr before formation of source/drain electrodes. Here it should be noted that the μ values observed for the C_{60} FET devices with Au electrodes after exposure to air could never get over 0.3 $cm^2\ V^{-1}\ s^{-1}$ even when annealing them for $\sim$12 h at 363–393 K under vacuum of 10^{-6}–10^{-8} Torr, since deep trap states are formed in the channel region by adsorbed O_2, and the transport of electrons are suppressed.[16–18] Therefore, the μ value of 0.50 $cm^2\ V^{-1}\ s^{-1}$ for the C_{60} FET device exposed once to air can be closely related to the high injection efficiency of electrons from source electrode to LUMO achieved using Eu electrodes.

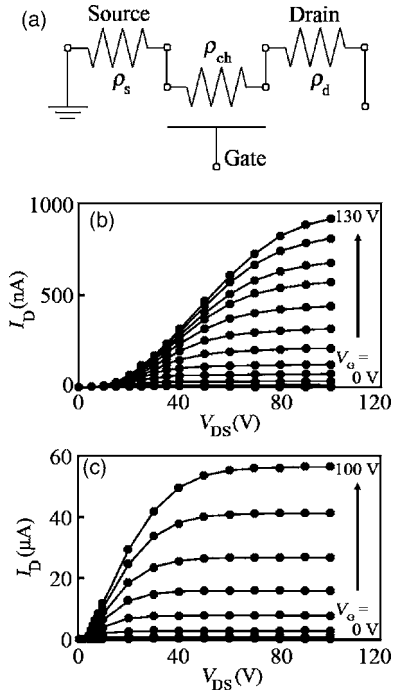

FIG. 3. (a) Circuit model for the FET device. I_D-V_{DS} plots for C_{60} FET devices with (b) Cu and (c) Pt electrodes measured at 294 K.

Here it is significant to say that the μ values are not independent of injected carrier concentration. As seen from Fig. 3(a), the total resistivity ρ_t of the C_{60} FET device can be expressed with the resistivity ρ_{ch} of C_{60} thin films and the resistivity ρ_c between source/drain electrodes and C_{60} thin films as follows:

$$\rho_t = \rho_{ch} + \rho_c = 1/en\mu_{ch} + \rho_c = 1/en\mu. \quad (1)$$

Here, e and n refer to the charge and carrier concentration. The ρ_{ch} corresponds to the intrinsic mobility of thin films of C_{60}. The ρ_c ($=\rho_s+\rho_d$) can be associated with the Schottky barrier between the electrodes and thin films; ρ_s and ρ_d correspond to resistivity between source electrode and C_{60} thin films and resistivity between drain electrode and C_{60} thin films, respectively. As seen from Eq. (1), the μ value increases with a decrease in ρ_c, showing that the μ value reflects strongly the injection efficiency from electrodes to C_{60} thin films. Such an increase in μ value linked with injection efficiency is also found in the perylene FET device.[23]

Furthermore, it should be noted that the V_T is positive despite of nonvanishing I_D at V_G=0 V. Generally, nonvanishing I_D produces negative V_T for n-channel operation. As seen from Fig. 2(b), the I_D is constant at $\sim$40 μA below V_G of 40 V. This result implies that the I_D of 40 μA does not correspond to channel current but bulk current which flows

through the whole region of thin films. Namely, this device shows apparent normally on FET properties produced by high bulk current, and the bulk current originates from no or small energy barrier from source electrode to LUMO.

The I_D vs V_{DS} plots measured after keeping the device at 294 K for 12 h under vacuum of 10^{-8} Torr is shown in Fig. 2(c). The I_D decreases by one order of magnitude, and the μ value was determined from the I_D-V_G plots (linear region) shown in Fig. 2(d) to be 7.9×10^{-2} cm^2 V^{-1} s^{-1} whose value is 1/6 of the μ value, 0.50 cm^2 V^{-1} s^{-1}, measured at 294 K just after annealing. The reduction of μ may be due to the oxidation of Eu electrodes. However, as the Eu electrode is top contacted to C_{60} thin films, further study is required to clarify whether the interface between the Eu electrodes and C_{60} thin films is influenced by small amounts of O_2.

The I_D-V_{DS} plots for the C_{60} FET devices with Cu and Pt are shown in Figs. 3(b) and 3(c), respectively. These plots show *n*-channel normally off FET properties. As seen from Fig. 1(b), the energy barrier exists for electron between source electrode and LUMO level. This should lead to vanishing I_D at V_G of 0 V since carriers cannot be injected because of the impediment by the Schottky barrier. The μ values for the C_{60} FETs with Cu and Pt were determined from the $I_D^{1/2}$-V_G plots (saturation region) to be 2.3×10^{-4} and 2.4×10^{-2} cm^2 V^{-1} s^{-1}, respectively. The values for the C_{60} FETs with Cu and Pt electrodes are smaller by one to three orders of magnitude than that of the C_{60} FET device with Eu. The device structure is different between C_{60} FETs with Eu and Cu/Pt. Though it is reported that the interface structure drastically changes between the pentacene thin films on metal electrodes and metal electrodes on pentacene thin films,[24] the difference in output properties for the C_{60} FETs with Eu and Cu/Pt can be reasonably explained only by considering the difference in energy barrier between source electrode and C_{60} thin films.

The I_D for the C_{60} FET with Cu electrodes [Fig. 3(b)] is lower than that with Pt [Fig. 3(c)] regardless of the smaller energy barrier between Cu and LUMO of C_{60} than that between Pt and LUMO. Furthermore, the I_D-V_{DS} plots for the C_{60} FET with Cu electrodes show nonlinear behavior at low V_{DS}, suggesting the existence of large Schottky barrier. These results present the possibility that the factors such as charge transfer and $d-\pi$ interaction between metal and C_{60} considerably change the net ϕ values of Cu and Pt metals.

In conclusion, the high μ value of 0.50 cm^2 V^{-1} s^{-1} has been obtained in the C_{60} FET device with Eu electrodes. The μ value is comparable to the best record obtained for the C_{60} FET device with Au electrodes fabricated without exposure to air.[4,6] The I_D-V_{DS} plots for the C_{60} FET device with Eu electrodes show *n*-channel normally on property. These results are realized by high injection efficiency in electrons produced by no or small energy barrier for electron from source electrode to LUMO of C_{60}.

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